Guest Editorial

Behind this special issue on VLSI Testing

Sunil R. Das
Guest Editor

With advances in the technology of electronic digital circuits through the introduction of very large scale integrated (VLSI) circuits, the problem of fault detection, fault analysis, and test generation has become a prime issue in the domain of VLSI design. The overwhelming response to the Call For Papers for this Special Issue on VLSI Testing from various parts of the world is a brilliant testimony to the profound interest and ever-increasing activities of the researchers in this important discipline.

All of the papers in this inaugural issue of *VLSI Design* are from recognized experts in the field of VLSI testing. Our first article, by Swartzlander and Malek, discusses a test approach suitable for repetitive structures like cellular arrays. The approach is directly applicable to most arithmetic circuits, which are generally quite regular, and is based on exhaustive testing of overlapping segments of the array. The approach further detects bridging faults besides stuck faults, and its high fault coverage makes it rather suitable for testing current VLSI and future WSI arrays.

Next, Sharma and Saluja propose a built-in concurrent self-test (BICST) technique for testing combinational logic circuits concurrently with their normal operation. The authors utilize the concept of sharing the test hardware among identical circuits to reduce the overall area overhead. The proposed technique was implemented in the design of an ALU with on-line test capability in CMOS technology. The authors also discuss the performance evaluation of their BICST technique and its possible use in the detection of intermittent faults and in computing transient fault coverage.

The paper by Savir and Bardell describes the progress in built-in self-testing or BIST since its very inception, and presents the important problems that still remain to be solved to make the technique widely acceptable. The article provides an extensive bibliography on the subject and is expected to be of great value to researchers in the field.

Bryan, Devadas and Keutzer consider analysis and the problem of synthesis of regular structures such as adders, arithmetic logic units, comparators, multipliers, and parity generators to determine whether they are testable for dynamic faults, or how they can be modified for testability for dynamic faults, at the same time maintaining good area and performance characteristics. In design modification to produce fully robustly testable structures, the authors derive a number of new composition rules that allow cascading of the individual modules, while maintaining robust testability under dynamic fault models. Methods for obtaining circuits that are fully testable in weaker fault models like transistor stuck-open fault and robust gate-delay fault are also analyzed.

Najjar and Srimani use a new probabilistic measure of network fault tolerance expressed as the disconnection probability to study the robustness of star graphs. The authors derive analytical approximation for the disconnection probability of star graphs and verify it with Monte Carlo simulation. The measure of network resilience and relative network resilience to evaluate the effects of disconnection probability on the reliability of star graphs are presented as well.

Debany presents a method to determine the coverage of shorts or bridging failures by internal access techniques that provide node observability. The method requires only good circuit simulation and does not involve creation of the universe of bridging failures.

Finally, Mourad discusses criteria for selecting benchmark circuits. These criteria are partly based on results of experiments carried out to characterize computer-aided testing systems (CATS). He also examines practical considerations involved in benchmarking. The author's emphasis is specifically on automatic test pattern generators (ATPGs).

In conclusion, I would like to express my sincerest gratitude to those friends and colleagues who helped make this Special Issue a reality. First, Professor George W. Zobrist, the Editor-in-Chief of this journal, who has been a constant source of encouragement, help, and guidance. His immense help and valued

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