Preface

Many VLSI CAD problems are constrained optimization problems, and almost all nontrivial versions of these problems are computationally intractable (NP-hard). Developing effective techniques for solving these optimization problems therefore plays an essential role in VLSI research. The VLSI optimization problems have attracted extensive attention in the past, and will continually be a major focus in the future. In recent years, many new techniques for solving NP-hard problems have been introduced. Examples include simulated annealing, neuralnet approach, generic algorithms, randomized algorithms, pseudopolynomial algorithms, parallel computing, etc. The development and application of new VLSI optimization techniques has become one of the most exciting and active areas in VLSI CAD research. Such efforts require deep mathematical insight into these VLSI problems, and extensive experimental verifications.

Optimization in VLSI synthesis and layout is the focus of this special issue. VLSI synthesis is a task that takes the behavior specification of a VLSI system or circuit, and a set of constraints to be satisfied and objective functions to be optimized, constructs a circuit implementation that satisfies the constraints and optimizes the objectives. Basically, there are two types of synthesis, high-level synthesis and logic synthesis. VLSI layout is a classical problem. It consists of subproblems as circuit partitioning, placement and floor-planning, global and detailed routing, and compaction. The objective of synthesis and layout is to optimize the performance of the circuit and to minimize its layout area.

This special issue contains seven articles. The topics covered include encoding of multi-level finite state machines and technology mapping for FPGAs (Field Programmable Gate Arrays) in logic synthesis, and placement, floor-planning, global routing, and detailed routing in VLSI layout. The optimization techniques used in the proposed methods include problem decomposition, problem transformation, branch and bound, evolution programming, randomization, iterative improvement with generalized moves, and force-directed heuristics. Each method is shown effective by theoretical analysis and experimental results for the particular problem considered. The articles in this special issue provide a good sample of current research in the area of optimization in VLSI synthesis and layout.

Si-Qing Zheng
Dian Zhou

Guest Editors' Biographical Information

Si-Qing Zheng received the B.S. Degree in Electrical Engineering from Jilin University, China, in 1973. From 1976 to 1980, he was a research engineer at Chinese Academy of Sciences, Beijing, China. He received the M.S. degree in Mathematical Sciences from the University of Texas at Dallas in 1982, and the Ph.D. degree in Computer Science from the University of California, Santa Barbara, in 1987. In August 1987, he joined the faculty of Department of Computer Science, Louisiana State University, where he is currently an associate professor. Dr. Zheng's research interests include VLSI, parallel and distributed computing, computer networks, and computational geometry. He has published 70 refereed research articles in these and related research areas.

Dian Zhou received the B.S. degree in Physics and the M.S. degree in Electrical Engineering from the Fudan University, Shanghai, China in 1982 and 1985, respectively, and the Ph.D. degree in Electrical and Computer Engineering from the University of Illinois at Urbana-Champaign, Illinois in 1990. His research interests include VLSI design, CAD systems and tools, circuit design and simulation, algorithms, and multichip module systems. He was a research assistant with the Applied Computation Theory Group at the Coordinated Science Laboratory, the University of Illinois. He is currently an assistant professor with the Department of Electrical Engineering, University of North Carolina at Charlotte. Dr. Zhou is a member of Tau Beta Pi. He received the National Science Foundation Research Initiation Award in 1991. He received the IEEE Circuit and System Society Darlington Award in 1993.