Guest Editorial

Field-Programmable Gate Arrays

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Field-Programmable Gate Arrays (FPGAs) are becoming increasingly popular for *rapid prototyping* of *Application Specific Integrated Circuits* (ASICs), implementing hardware emulation systems, and custom computing. Rapid turnaround time for high density integrated circuits is one major advantage that FPGAs offer. FPGAs are among the fastest growing arenas in the semiconductor industry. Some of the designs using FPGAs have exploited programmability very heavily and the resulting systems have matched near supercomputer performance at extremely low costs. All these examples have proven vast applications of FPGAs, much beyond the earlier thought applications like a technology to provide "glue logic" or a technology to support rapid prototyping at low costs.

New fields have emerged with the advent of FPGAs. User programmability with high density devices has started research in the areas of FPGA architecture, computer aided design (CAD) tools, special purpose computing, hardware emulation/simulation, programming environments, and dynamically reconfigurable computer architecture. Various architectural studies have appeared in the recent past and associated CAD tools have been heavily investigated. Most of the work related to the FPGA architecture has addressed the commercially available FPGAs and the

research in CAD tools has been mostly targeted towards logic synthesis. Incremental changes in FPGA architecture and associated CAD tools have been suggested from time to time.

This special issue contains five papers that are representative of some of the innovations that have led to the development of better FPGA architectures and supporting CAD tools for mapping applications on FPGAs.

The first paper by Cherepacha and Lewis describes a new FPGA architecture that is suitable for datapath oriented circuits. This is an important area as most existing architectures do not handle very regular circuits efficiently. Also, as large applications are synthesized for FPGAs, the ratio of the regular datapath to the random control logic will increase substantially. Thus architectures like DP-FPGA are very much sought. The second paper authored by Roy and Sechen addresses a very important problem related to design partitioning. For very large applications, it becomes essential to partition the design into multiple number of segments such that each segment can be accommodated in one physical device. The partitioning has to be done under very severe area and pin constraints. While trying to satisfy these fundamental constraints, it is likely that the overall performance of the design may degrade due to signal paths traversing

back and forth between various physical devices. In order to have minimum degradation, the partitioning has to be done very carefully and this second paper addresses one such way of performing timing driven partitioning for multiple FPGAs. The third and fourth papers address the timing driven placement for mapping designs on FPGAs. The third paper by Raman and Liu uses force-directed method to obtain a timing driven placement for FPGAs. The fourth paper by Roy, Guan and Sechen uses simulated annealing to accomplish timing driven placement for FPGAs. Finally, the last paper addresses the routing problem in FPGAs. The SEGA router developed by Brown, Khellah and Lemieux is capable of routing placed circuits by taking both performance and routability into account. Various research results important for better understanding of routing architecture of FPGAs are also presented in this last paper.

Author Biography

Dinesh Bhatia received a Bachelors in Electrical Engineering from Regional Engineering College, Suratkal, India and Masters and a Ph.D. in Computer Science from University of Texas at Dallas. Currently he is an Assistant Professor in the department of Electrical and Computer Engineering and Computer Science at the University of Cincinnati. He also directs the Design Automation Laboratory within the same department. Prior to his current position he was a visiting Assistant Professor of Computer Science and Engineering at the Southern Methodist University in Dallas. His research interests include the architecture and CAD for field-programmable gate arrays, interconnection problems in VLSI, physical design of MCMs and large ICs and, graph theory and its application in VLSI design.