Linking Behavioral, Structural, and Physical Models of Hardware

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The explosion in complexity of VLSI chips has made it increasingly difficult for designers to manually carry out the chip and systems design. Automated synthesis from behavioral specifications is emerging as a most promising approach to the implementation of large scale systems. Current behavioral level design models lack the capability of capturing important physical design effects such as wiring and floor-planning which are first order factors in layout area and performance (especially for large scale designs). Relying on such incomplete and abstract models when performing early design decisions could therefore adversely affect the quality of the final solution. Unfortunately, the exact physical attributes of a design are not known until the design process is carried out in full. Since design steps are quite expensive, it is not feasible to go through a full design iteration step every time a high level decision is made. Thus, in order to approximate a realistic layout model of hardware, the designer must rely on efficient but accurate estimates of the various design metrics throughout the design process. This way, the physical effects can be properly accounted for without incurring an unacceptable penalty in runtime.

In order to develop such models of layout, it is clear that there is a need to address research problems both in synthesis and physical design. Specifically,

the topics covered in the papers presented in this special issue include the following:

- Synthesis and incorporating physical design information into the synthesis tasks.
- Modeling of layout and the physical design process.
- Predicting design quality metrics, such as: area, performance, power, and reliability.
- Linking synthesis tasks and physical design tasks together.
- Physical design driven technology mapping.

We start with a paper by Pedram, Bhatt and Kuh which describes a technique for integrating technology mapping with layout by performing the two processes in lock-step. This results in circuits of smaller area and higher performance.

The next paper by Chandrasekhar, McCharles, and Wallace present three aspects of coupling logic synthesis with layout. These aspects are: exploiting logic equivalence, net-weighting, and resynthesis.

The third paper by Tyagi describes methods techniques to estimate the area and delay of RT level modules. These techniques are based on statistical models.

The fourth paper by Dutt and Jha discusses describes work that defines, evaluates and demonstrates

the use of a canonical RT component set to support design refinement, reuse and automatic model generation.

The fifth paper by Harris and Orailoglu looks at techniques for selecting a module set for implementing an RT level design from behavioral specification. These techniques successfully explore the different module tradeoffs to satisfy an overall area and/or time constraint.

The sixth paper by Weng and Parker describe design strategies for relieving potential thermal problems. These design strategies are applied during high level synthesis, and help eliminate hot-spots on a chip.

The seventh paper by Wu presents an extensive experimental study on the relationship between traditional high level area models and actual layouts. The author concludes that these models lack *fidelity*, which is shown to be important for producing high quality designs.

The eighth paper by Tsai and Hsu describes a design methodology for linking high level synthesis and layout. They use a two level layout model to help explore the design space in an interactive manner.

In conclusion, I would like to acknowledge the help and encouragement of Prof. George Zobrist in organizing and processing the papers of this special issue. I would also like to thank the many reviewers who refereed the papers for their diligence and timeliness. Finally, thanks go to my assistant, Ms. Louise Karkoutli whose help was invaluable in organizing the review process of this issue.

ican University of Beirut, Lebanon in 1981, and the M.S. and Ph.D. degrees in Computer Engineering from the University of Southern California in Los Angeles, CA, in 1982 and 1987, respectively.

Since 1987, he has been a faculty at the Department of Electrical & Computer Engineering at the University of California, Irvine, where he is currently an Associate Professor. His research interests are in the areas of Computer-Aided Design of VLSI circuits, high-level synthesis, and design methodology of large scale systems. His research addresses the issues of linking High Level Synthesis to subsequent levels of design, namely logic and physical levels. He has published papers dealing with various aspects of chip and system synthesis at international conferences and journals. He has organized and participated in tutorials on high level synthesis at international conferences such as the Design Automation Conference in 1990. Prof. Kurdahi was Associate Editor for IEEE Transactions on Circuits and Systems II in 1993–95. He was Organization chairman of the Sixth International High Level Synthesis Workshop, and served on the Program committees of several conferences and workshops such as: the International High Level Synthesis Workshop, the International Symposium on System Level Synthesis, and the European Design and Test Conference. He received the Research Initiation Award from the National Science Foundation in 1989, and the ACM/SIGDA Fellowship in 1991 and 1992. Dr. Kurdahi is a member of IEEE and ACM.

Authors' Biography

Fadi J. Kurdahi received the Bachelor of Engineering degree in Electrical Engineering from the Amer-