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On Ensuring Multilayer Wirability by Stretching Layouts*

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Every knock-knee layout is four-layer wirable. However, there are knock-knee layouts that cannot be wired in less than four layers. While it is easy to determine whether a knock-knee layout is one-layer wirable or two-layer wirable, the problem of determining three-layer wirability of knock-knee layouts is NP-complete. A knock-knee layout may be stretched vertically (horizontally) by introducing empty rows (columns) so that it can be wired in fewer than four layers. In this paper we discuss two different types of stretching schemes. It is known that under these two stretching schemes, any knock-knee layout is three-layer wirable by stretching it up to (4/3) of the knock-knee layout area (upper bound). We show that there are knock-knee layouts that when stretched and wired in three layers under scheme I (II) require at least 1.2 (1.07563) of the original layout area. Our lower bound for the area increase factor can be used to guide the search for effective stretching-based dynamic programming three-layer wiring algorithms similar to the one presented in [8].

Keywords: Knock-knee layouts, three-layer wirable, stretching schemes, three-dimensional layouts, layer assignment, detailed routing

1. INTRODUCTION

The *rectangle routing problem* (*RRP*), which is also referred to as the *switch-box routing problem*, is a fundamental problem in computer-aided VLSI physical design. The input to this problem is a rectangular *grid* R determined by the horizontal lines with y-coordinate values i, $0 \le i \le h+1$ and the vertical lines with x-coordinate values j, $0 \le j \le w+1$. The horizontal lines with y-coordinate values 0 and $h+1$ and the vertical lines with x-coordinate values 0 and $w+1$ form the *boundary* of R. Let $N = \{N_1, N_2, \ldots, N_p\}$, where each N_i is a subset of grid points on the boundary of R (excluding the corners of R), such that $N_i \cap N_j = \emptyset$ for all $i \neq j$. Each set N_i is called a *net* and its grid points are called *terminals*. A special case of RRP is the *channel routing problem* (*CRP*), in

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which all terminals are located on two opposite sides of R.

Traditionally, the RRP has two conducting layers available for routing. Recent advances in VLSI fabrication technology have made it practical to use three or more layers for the interconnection of the nets. A typical knock-knee multi-layer RRP routing algorithm consists of two phases. In the first phase, a knock-knee wire layout $W=\{W_1,W_2,\ldots,W_p\}$ is constructed, where each W_i is a subgraph of the grid R connecting all terminals in N_i such that W_i does not share any grid edge with W_j for all $j\neq i$. In the second phase, each wire segment in W is assigned to a layer in such a way that no two wire segments from distinct wires share a grid point in any layer. For example, this approach is used by the routing algorithm for the two-terminal-net CRP (each net has exactly two terminals) by Preparata and Lipski [18]. Their algorithm guarantees an optimal three-layer wiring. Several other routing algorithms are also based on this approach (e.g., see [13, 16, 17, 19]). Brady and Brown [2] showed that every knock-knee layout can be transformed into a four-layer wiring with dimensions identical to those of the knock-knee layout. By using the reduction given in Theorem 2.1 (refer to the next section), Lipski [14] showed that the problem of deciding whether a given knock-knee layout is three-layer wirable is an NP-complete problem. Only restricted classes of knock-knee layouts are known to be three-layer wirable (e.g. [13, 20, 17, 19]).

A knock-knee layout may be *stretched vertically* (*horizontally*) by introducing between a pair of adjacent rows (columns) an empty row (column) [see Fig. 6]. Clearly, stretching a knock-knee layout increases its area; however, if a knock-knee layout is stretched in appropriate places it can be wired in fewer than four layers. This approach has been considered in [4, 8, 9, 10, 11, 12, 16, 21]. It is important to investigate the trade-off between the routing area and the number of layers needed for wiring a knock-knee layout. Let $A(W)$ denote the area of knock-knee layout W. The simple stretching algorithm described in 16 generates a two-layer wiring with area at most $2A(W)$, by vertically stretching it between every pair of adjacent rows. Gonzalez and Zheng [9] showed that there are knock-knee layouts that need to be stretched by this factor of two even when more general stretching schemes are allowed. Algorithms that construct minimum area two-layer wirings by vertically stretching the knock-knee layout are given in [4, 12]. Algorithms that construct area-efficient three-layer wirings by vertically stretching the knock-knee layout are given in [4, 8]. When there are more than four layers available for wiring, a routing solution is rather complicated and thus harder to generate due to its 3-dimensional structure. In such a situation, the partition approach of [1, 5, 7] can be used. In this approach, an RRP can be decomposed into several RRP's, each consists of a collection of subnets of the original RRP. Then, each of these new RRP's is solved using a fixed number of layers. One possible partition method is to ensure that each generated RRP to be routable in knock-knee mode. The routability can be guaranteed by using the conditions given in [3, 6] and algorithms in [3, 6, 16]. Once the knock-knee layouts for these RRP's are generated by some knock-knee routing algorithms, the multilayer wiring can be constructed by stretching and wiring each of these knock-knee layouts.

In this paper we discuss two different types of stretching schemes, scheme I and scheme II, for three-layer wiring knock-knee layouts. Scheme I allows layout stretching only in one dimension, whereas scheme II allows layout stretching in both dimensions. A stretched three-layer wiring is optimal if the resulting layout area is minimum. By the results of [14], the problem of finding an optimal stretching is NP-hard. We investigate the lower-bounds of the ratios of the stretched 3-layer wirable layout and the original layout under these two schemes. This problem is important since it provides a measurement for evaluating the performance of stretching and 3-layer wirability. It is known that under scheme I, any knock-knee

layout may be stretched and wired using three layers in no more than (4/3) the knock-knee layout area (upper bound) [4, 8]. In section 4(5), we show that there are knock-knee layouts that when stretched and wired in three layers under scheme I (II) require at least 1.2 (1.07563) of the knock-knee layout area. Our lower bound for the area increase factor can be used to guide the search for effective stretching-based dynamic programming three-layer wiring algorithms similar to the one presented in [8].

2. PRELIMINARIES

In this section, we review some of the fundamental concepts and the main theorem in the theory of wiring knock-knee layouts [15]. A *tessellation T of the plane* is a partition of the plane into regular polygons, called *tiles*, such that each partitioning line segment is shared by exactly two tiles. The sides of the tiles are called *tile edges*, and the endpoints of the tile edges are called *tile vertices*. The dual graph of a given tessellation T of the plane (called the *grid of* T and denoted by $R(T)$) is defined by grid points (vertices) located at the center of each tile and the grid edges that join grid points located on adjacent tiles. We say that a grid of T is *uniform* if each grid point has an even degree, i.e. each tile in its corresponding tessellation T has an even number of sides. There are exactly four different uniform grids: square, hexagonal, octo-square and dodeco-hexo-square [15]. In this paper, we only consider the uniform square grid. A *layout domain* D is a collection of tiles of T. The definition of the grid of D, which is denoted by $R(D)$, is similar to that of $R(T)$. I.e., the grid edges of $R(D)$ are the grid edges in $R(T)$ that intersect a tile edge of a tile in D, and the grid points of $R(D)$ are the grid points in $R(T)$ incident to a grid edge in $R(D)$. The grid points in $R(D)$ outside the tiles in D are called *terminals*. Whenever there is no ambiguity, we will draw terminal points at the intersection of its corresponding grid edge and the boundary of D. A *wire* w in D is a connected subgraph of $R(D)$ such that no grid point of D has exactly one wire edge (each edge in w is called a *wire edge*), except for the grid points called terminals.

A *knock-knee layout* (or simply *layout*) in D is a collection $W=\{W_1,W_2,\ldots,W_p\}$ of mutually edge-disjoint wires in D. In a knock-knee layout, two distinct wires can share a grid point only by crossing or forming a *knock knee*, as shown in Figure 1. We say that a layout W contains a *loop* if a subset of wire edges in wire $W_i \in W$ is of the form $\{(v_{k+1}, v_{k+2}), (v_{k+2}, v_{k+3}), \ldots, (v_{k+l-1}, v_{k+l})\}$ for some $l > 4$ and $v_{k+1} = v_{k+l}$, where $v_{k+1}, v_{k+2}, \ldots, v_{k+l}$ represent grid points of $R(D)$. A layout W in D is called a *full layout* if every grid edge of $R(D)$ is covered by a wire edge of a wire in W. If a grid point p of D is not included in wire edges belonging to more than wire, then p is called a *trivial grid point*. Accordingly, a tile of D is called *a trivial tile* if its corresponding grid point is trivial. Let D^* be the set of nontrivial tiles in D. The *core* of W, denoted by W^*, is the portion of W restricted to D^*, i.e., W^* is obtained by deleting from W all trivial grid points and all wire edges joining trivial grid points. A tile vertex that is shared by fewer than four tiles in D^* is called a *boundary vertex* of D^*, and a tile edge that is a side of only one tile is called a *boundary edge* of D^*. All other tile vertices and tile edges of D^* are called *internal*. The boundary vertices and boundary edges define the *boundary* of D^*, which is a set of vertex disjoint cycles. Note that a layout domain D can have any rectilinear polygonal shape, and D^* is a set of rectilinear polygons, each may contain a set of rectilinear polygonal holes. Hereafter we assume that all layout domains D will have a rectangular boundary, since the results on such domains can be trivially generalized to more general cases.

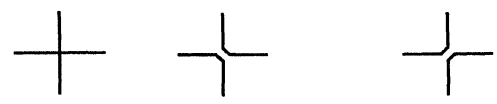

FIGURE 1 Crossings and knock-knees.

A tile in D which contains half wire edges belonging to two distinct wires W_i and W_j that form a knock-knee is called a *knock-knee tile*. The arrangement of diagonals bisecting both wires in each knock-knee tile is called the *diagonal diagram* D_d of W in D. We say that an internal tile vertex u of D_d is of *degree* k if there are k diagonals incident to u. Note that by the definition of D, there may be more than one layout sharing the same diagonal diagram. However, corresponding to each distinct diagonal diagram D_d in D there is a unique full layout W' such that each wire $W_i \in W'$ has no terminals or exactly two terminals. We call such a full layout as the *standard full layout* corresponding to D_d in D.

A (*conducting*) *layer* L_i, $1 \leq i \leq v$, is a copy of the grid $R(D)$. The v layers are considered laid one upon the other, in their indexed vertical order, with L_1 and L_v being the bottom-most and the top-most layers. A *v-layer wiring* of layout W in D is an assignment of each wire edge to a layer in such a way that if wire edges e_1 and e_2 of W_a incident to a grid point p of D are assigned to layers L_i and L_j, $i \leq j$, respectively, then for every edge e of W_b, $a \neq b$, incident to p, e is not assigned to a layer L_k, for $i \leq k \leq j$. The following theorem is fundamental in the theory of multi-layer wiring.

THEOREM 2.1([15]) *An arbitrary knock-knee layout W in layout domain D is three-layer wirable if and only if there exists a set P^* of internal tile edges in D^* corresponding to W^* such that*

(*a*) *every internal tile vertex of D^* is incident with an even number of segments of $P^* \cup D_d^*$;*
(*b*) *for each connected component of the boundary of D^*, the total number of incidences of segments of $P^* \cup D_d^*$ with vertices along this component is even; and*
(*c*) *all segments in $P^* \cup D_d^*$ incident at any vertex of D^* does not contain any of the eight forbidden patterns shown in Figure 2, where diagonals drawn as dashed segments are not present.*

We call the set P^* of line segments satisfying the conditions given in this theorem a *legal partition* of the diagonal diagram D_d^* in D^*. When the layout domain is understood we just omit it and say that a set of edges is a legal partition of a diagonal diagram. Theorem 2.1 shows that the existence of a legal partition of D_d^* in D^* is a necessary and sufficient condition for the layout W in D to be three-layer wirable. What can be said about the existence of a legal partition of D_d in D? Since $D_d^* \subseteq D_d$ and $D^* \subseteq D$, we know that the existence of a legal partition P for D_d in D implies the existence of a legal partition P^* for D_d^* in D^*. It is simple to prove that the reverse is not true. Therefore, the existence of a legal partition P of D_d in D can only be used as a sufficient condition for three-layer wiring of knock-knee layouts. This well known result is captured in the following corollary.

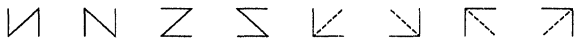

FIGURE 2 Forbidden Patterns. Dashed diagonals are not present.

COROLLARY 2.1 *An arbitrary knock-knee layout W in layout domain D is three-layer wirable if there exists a legal partition P of D_d in D.*

A legal partition divides $D^* \cup D_d^*(D \cup D_d)$ into regions that are two-colorable, i.e. using two colors one can color its regions in such a way that every two adjacent regions (regions sharing a line segment as their common boundary) can be assigned distinct colors. Given a legal partition $P^*(P)$ of a diagonal diagram $D_d^*(D_d)$ in $D^*(D)$ corresponding to $W^*(W)$, the process of transforming layout W into a three-layer wiring is simple. Interested readers may refer to [18] for details of this transformation. Using the reduction given in Theorem 2.1, Lipski [14] gave an example showing that there exists a 19-row wire layout that is not three-layer wirable. Using this layout structure he showed that the problem of deciding whether a knock-knee layout is three-layer wirable is NP-complete.

Consider the layout domain D and a layout W defined in D as shown in Figure 3(a). The

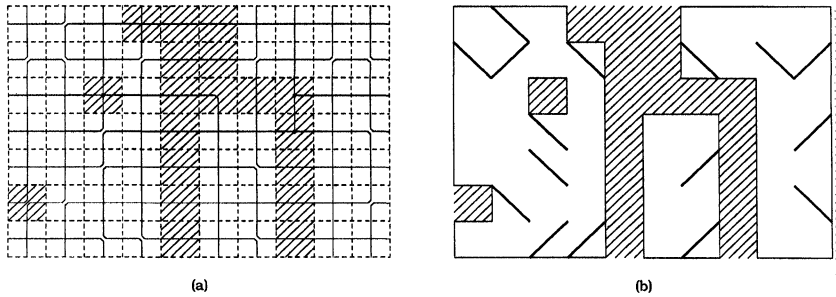

FIGURE 3 (a) Knock-knee layout. Layout domain D (all tiles), layout W (solid lines, dark dots are connections), trivial tiles (shadowed tiles), W^* (the portion of W in the non-trivial tiles), and domain D^* (unshadowed tiles). (b) Diagonal Diagram D_d^* on D^*. Shadowed area are trivial tiles.

shadowed tiles are trivial tiles and the portion of the wires defined in the non-trivial tiles is W^* and the non-trivial tiles constitute the layout domain D^*. Note that in this case D^* consists of three rectilinear polygons, and one of them contains a hole. Figure 3(b) shows the diagonal diagram D_d^* corresponding to W^*. A legal partition of the diagonal diagram given in Figure 3(b) is shown in Figure 4(a). A three-layer wiring constructed from the legal partition (Figure 4(a)) is shown in Figure 4(b). For the RRP problem the layout domain D is an h-row by w-column rectangular subdivision of T. If W is a loop-free full layout in a layout domain D such that every wire W_i of W has two terminals, then W^* is identical to W and D^* is identical to D. Therefore, to derive new results on three-layer wirability of knock-knee layouts, it is sufficient to consider only two-terminal net loop-free full layouts. We are particularly interested in the layouts in a rectangular domain D. In section 6, we discuss some results concerning three-layer wiring based on the conditions given in Corollary 2.1.

3. LAYOUT STRETCHING SCHEMES

Since the problem of determining whether a knock-knee layout is three-layer wirable is NP-complete, we investigate the problem of stretching and then wiring a knock-knee layout. This approach has been considered in [4, 8, 9, 10, 11, 12, 16, 21]. Stretching a layout vertically (horizontally) is equivalent to dividing the layout horizontally (vertically) between two adjacent rows (columns) into two sublayouts, then inserting an empty horizontal (vertical) grid line between these two sublayouts and merging the vertical (horizontal)

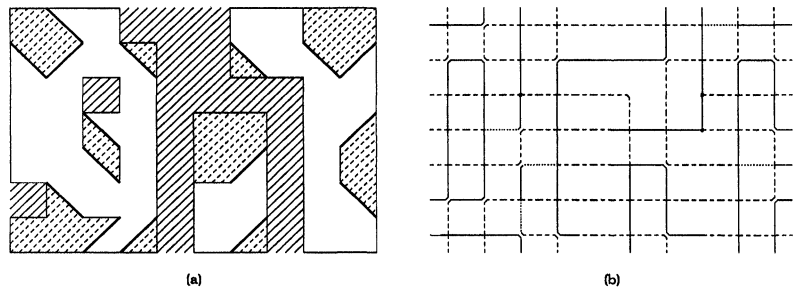

FIGURE 4 (a) Legal partition of D_d^* in D^*. The colors are blank and dashed. (b) Three-layer wiring of W obtained from the legal partition. Solid lines (top layer), dotted lines (middle layer), and dashed lines (bottom layer).

wires in these two sublayouts at the newly introduced grid line. The following layer assignment scheme is a direct generalization of the layer assignment algorithm given in [16].

(1) Divide W horizontally and/or vertically, into sublayouts $W^1,\ldots,W^s$, such that $W^i, 1 \leq i \leq s$, is three-layer wirable.
(2) Find a three-layer wiring for each sublayout W^i of W.
(3) Extend the grid R to form grid R' by inserting a horizontal (vertical) empty grid line between sublayouts separated by a horizontal (vertical) dividing line introduced in step (1).
(4) Merge two adjacent sublayouts at the newly inserted grid line and introduce vias at the grid points on the new grid line if it is necessary.

Depending on the type of additional grid lines introduced, we make a distinction between the following two stretching schemes:

Scheme I Wirings are obtained by only introducing either additional horizontal or vertical grid lines.
Scheme II Wirings are obtained by introducing additional horizontal and vertical grid lines.

Let h and w be the height and width for grid R, respectively. We use W' to denote the layout corresponding to the wiring obtained by the above algorithm. Clearly, for scheme I we have

$$A(W') = \left(1 + \frac{t}{h}\right) \cdot A(W),$$
$$(\text{or } A(W') = \left(1 + \frac{t}{w}\right) \cdot A(W)),$$

where t is the number of additional horizontal (or vertical) grid lines. For scheme II we have

$$A(W') = \left(1 + \frac{t}{h}\right) \cdot \left(1 + \frac{u}{w}\right) \cdot A(W),$$

where t and u are the number of additional horizontal and vertical division lines introduced, respectively. Examples of stretched layouts under scheme I and II for the layout in Figure 5 are given in Figure 6.

Consider any full layout W defined in a rectangular layout domain D without holes. If every wire W_i in W has two terminals and the segments of each W_i does not form a loop, then (as we mentioned before) W^* and D^* are identical to W and D, respectively. Then, finding a three-layer wiring of W by the above stretching and wiring schemes can be restated as follows.

(1) Construct the diagram D_d corresponding to W.
(2) Divide D_d into legally partitionable blocks $D^1,\ldots,D^s$, by introducing horizontal and/or vertical partitioning lines along the tile edges of D (accordingly layout W on D is partitioned into three-layer wirable sublayouts $W^1,\ldots, W^s$).
(3) Find legal partition P^i for each D^i and construct a three-layer wiring A^i for the sublayout W^i from P^i of D^i.
(4) Extend the grid R to form grid R' by inserting a horizontal (vertical) empty grid line between every two adjacent sublayouts separated by a horizontal (vertical) division line introduced in step (2).
(5) Obtain a stretched layout W' and its wiring by merging every two adjacent sublayouts in the

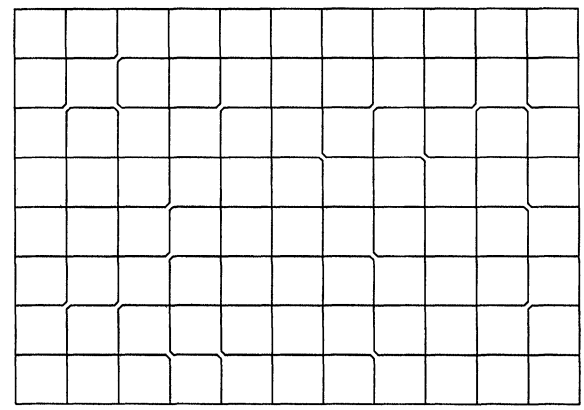

FIGURE 5 Standard full Layout for the knock-knee layout given in Figure 3(a).

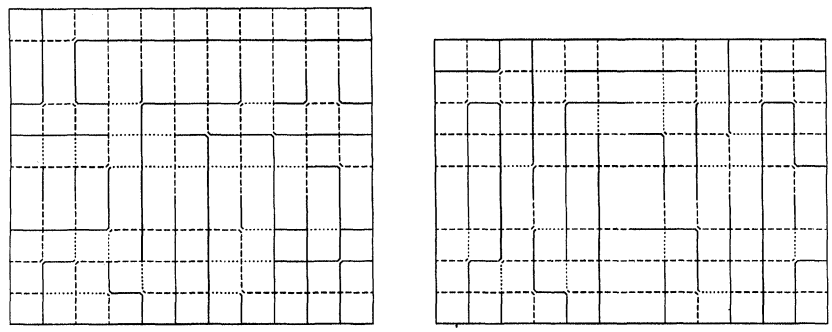

FIGURE 6 Layouts obtained by stretching the layout in Figure 5 using scheme I and II.

division at the newly inserted grid lines and introduce vias at the grid points on the new grid line whenever necessary.

We call the ratio $A(W')/A(W)$ the *area increase factor* of the stretching scheme. This abstraction of stretching and wiring schemes allows us to simplify the investigations on the area increase factor in two different but related aspects. We elaborate this point by considering only scheme I, because similar arguments can be applied to scheme II. Since the existence of a legal partition of D_d is a sufficient condition for the three-layer wirability of all layouts sharing the same D_d (see Corollary 2.1), if we know that for any k-row diagonal diagram there exists a legal partition, then we can conclude that any layout W can be wired with three layers in area no greater than $((k+1)/k)\,A(W$. Here, $(k+1)/k$ is an upper bound for the area increase factor under scheme I. Therefore, the problem of finding a computationally attainable smaller upper bound is equivalent to finding an efficient algorithm that guarantees a three-layer wiring for any k-row layout such that k is as large as possible. On the other hand, if we know that there exists at least one two-terminal loop-free full layout W with diagonal diagram D_d such that all its subdiagrams formed by its k adjacent rows and all its subdiagrams formed by its k adjacent columns do not admit legal partitions, then by Theorem 2.1 we can conclude that not all layouts W can be wired with three layers in area less than $((k+1)/k)$ $A(W)$. That is, one cannot design an algorithm which guarantees three-layer wirings with area less than $(k+1)/k\,A(W)$ for all layouts W. Here, $(k+1)/k$ is an existential lower bound (or simply lower bound) for the area increase factor under scheme I. The lower bound for the area increase factor can be used to guide the search for effective stretching-based three-layer wiring algorithms.

4. A LOWER BOUND FOR THE AREA INCREASE FACTOR UNDER SCHEME I

To establish a lower bound for the area increase factor under scheme I, we construct a knock-knee full layout and show that (a) it is a two-terminal loop-free knock-knee layout (Lemma 4.4), and (b) when stretched and three-layer wired under scheme I it requires at least a number of grid lines proportional to either the height or the width of the layout constructed in (a) [Theorem 4.1]. To show that this layout is not three-layer wirable in an area 1.2 times the knock-knee layout area we show that any adjacent six rows or columns in the diagonal diagram D_d corresponding to the layout cannot be legally partitioned. This diagonal diagram consists of copies of a strip subdiagram arranged as shown in Figure 11. First we show that the strip subdiagram cannot be legally partitioned (Lemma 4.1) and then we show that it corresponds to a two-terminal-net loop-free full knock-knee layout (Lemma 4.2).

We now establish that the diagonal diagram, called the *strip subdiagram*, shown in Figure 7 does not admit any legal partition.

LEMMA 4.1 *The diagonal diagram given in Figure 7 does not admit any legal partition.*

Proof Since the proof is mechanical and has too many details, it is presented in the Appendix. □

LEMMA 4.2 *The standard full layout corresponding to the diagonal diagram given in Figure 7 is not wirable in three layers.*

Proof The standard full layout corresponding to the diagonal diagram given in Figure 7 is shown in Figure 8. Clearly, there is no loop in this layout. By Theorem 2.1 and Lemma 4.1, this layout is not three-layer wirable. □

Let us consider the standard loop-free full layout W given in Figure 8. We call a net in W a *rising net* if its two terminals (x_1,y_1) and (x_2,y_2) are not located on the same boundary and $x_1 < x_2$ and $y_1 < y_2$; a *falling net* if its two terminals (x_1,y_1) and (x_2,y_2) are not located on the same boundary and $x_1 < x_2$ and $y_1 > y_2$; a *through net* if its two terminals (x_1, y_1) and (x_2, y_2) are located on the two opposite boundaries and $x_1 = x_2$ or $y_1 = y_2$; a *local net* if for its two terminals (x_1, y_1) and (x_2, y_2) are located on the same boundary. Clearly, each net in the layout is of (exactly) one of these four types. We label each terminal with *r*, *f*, *t* or *l* depending on the type of net the terminal belongs to. For the two terminals belonging to the same local net and located at a horizontal boundary, we call the one with the smaller x-coordinate value the *left terminal of the net* and the other the *right terminal of the net*. We use *ll* and *lr* to distinguish left terminals and right terminals of local nets with terminals located on the top or bottom boundary. The layout has the following properties:

(i) Every wire (for a net) is vertically monotone, i.e. a vertical line located between any given two adjacent columns does not intersect the wire of any net more than once.

(ii) There does not exist a net whose two terminals are located on the same vertical boundary of the layout.

(iii) The terminal located at the left end of the i-th row and the terminal located at the right end of $((i \bmod 6)+1)$-th row, $1 \leq i \leq 6$, are either both labeled *r* or labeled *f*.

(iv) If a terminal labeled *f* or *ll* is located at the intersection of column c and the top boundary, then the terminal located at the intersection of column c and the bottom boundary is labeled *f* or *lr*.

(v) If a terminal labeled *r* or *lr* is located at the intersection of column c and the top boundary, then the terminal located at the intersection of column c and the bottom boundary is labeled *r* or *ll*, except for the pairing *lr* on the

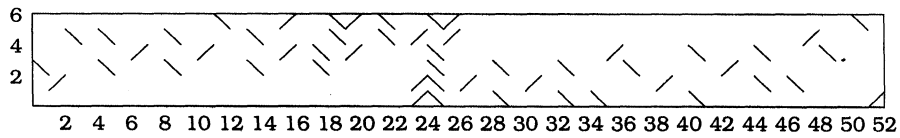

FIGURE 7 Strip Subdiagram.

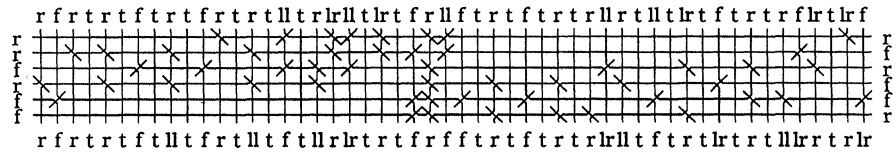

FIGURE 8 Labeled standard full layout for the diagonal diagram in Figure 7.

top boundary and *ll* on the bottom boundary which is not possible.

To simplify our notation we use t, b, l and r to label the top, bottom, left and right boundaries of the standard full layout corresponding to the strip subdiagram given in Figure 7. We say a terminal in the standard full layout corresponding to the strip subdiagram in Figure 7 is of type p_q if it is labeled $p \in \{r, f, ll, lr\}$ and it is located on the boundary labeled $q \in \{t, b, l, r\}$, of the layout. For example, a terminal is of type f_r if it is a terminal of a falling net located on the right boundary of the layout. Note that we totally ignore through nets and their terminals. The reasons for this will be addressed shortly. By fact (ii) we know that there are 12 different types of terminals in the layout corresponding to the strip subdiagram given in Figure 7 named r_t, r_b, r_l, r_r, f_t, f_b, f_l, f_r, ll_t, ll_b, lr_t and lr_b.

Let the lower left corner point of the layout domain D be (0,0). By placing a 6-row by 52-column strip subdiagram in D such that the lower left corner point of the strip subdiagram is $(52 \cdot i, i + 6 \cdot j)$, where $0 \le i \le 5$ and $j \ge 0$, we obtain a subdiagram arrangement shown in Figure 9. We call this arrangement the *strip subdiagram arrangement* A_{11}. The standard full layout corresponding to A_{11} is divided into sublayouts shown in Figure 8 by the division lines, which are the boundaries of subdiagrams, in subdiagram arrangement A_{11}. Thus a horizontal (resp. vertical) division line can be treated as the top (resp. left) boundary of one sublayout and the bottom (resp. right) boundary of another sublayout. Consequently, the crossing point of a wire and a division line in A_{11} can be treated as a terminal of both adjacent sublayouts along the division line. We may call such a crossing point a *pseudo terminal*. Obviously, a vertical wire of a through net in a sublayout corresponding to a subdiagram in A_{11} is a wire segment of a vertical wire going through the standard full layout corresponding to A_{11}. We can ignore these vertical wires since they never form loops.

Let us define a directed graph G (Fig. 10) as follows. There are 12 nodes in G, each corresponding to a distinct terminal type. There are two type of arcs, type-1 (solid lines) and type-2 (dashed lines). The type-1 arcs are labeled either L or R. A type-1 arc from node A to node B with label L (resp. R) indicates that in a strip subdiagram there is a net with terminals type A and B such that the wire that starts at the terminal represented by node A moves to the left (resp. right) until it reaches a terminal represented by node B. The type-2 arcs

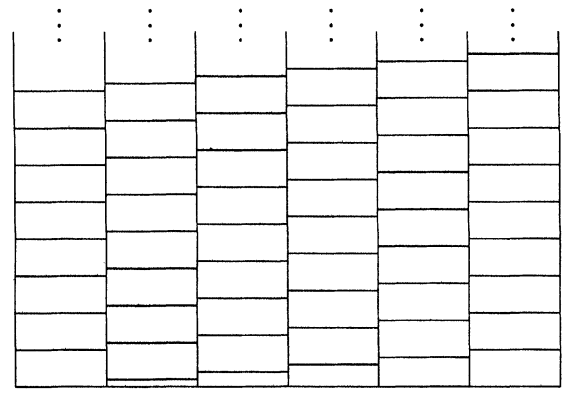

FIGURE 9 Strip subdiagram arrangement A_{11}.

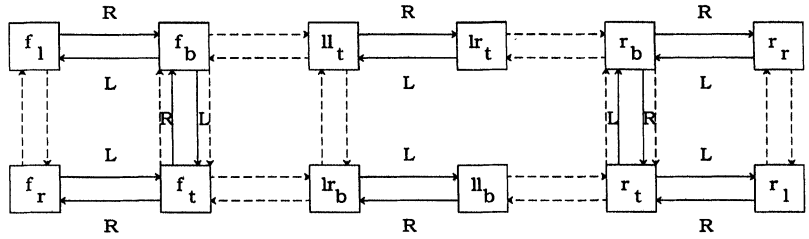

FIGURE 10 Type-1 arcs (solid arcs) and type-2 arcs (dashed arcs).

relate nets on adjacent strip subdiagrams. There is a type-2 arc from node A to node B if a pseudo terminal at a division line can be of type A for one sublayout and it can also be of type B for the adjacent sublayout along the division line. Note that type-2 arcs are symmetric.

Checking whether there is a loop in the standard full layout corresponding to A_{11} can be determined by tracing all wires in the layout. With graph G at hand, the verification is simpler. Let us trace any wire in the standard full layout corresponding to A_{11} starting from any pseudo terminal in it. In parallel to this tracing, we traverse the graph G through a directed path. It is easy to see that tracing a wire in the standard full layout corresponding to A_{11} is equivalent to traversing a directed path of arcs of type-1 and type-2 in an alternating order on graph G. If all type-1 arcs in an alternating path are labeled L (resp. R), then when we trace a wire in the layout corresponding to A_{11} we always move to the left (resp. right) from subdiagram to subdiagram. Taking fact (i) into account, we know that every wire in the standard full layout corresponding to A_{11} is vertically monotone. Therefore, there are no loops.

LEMMA 4.3 *The standard full layout corresponding to the subdiagram arrangement A_{11} given in Figure 9 is loop-free.*

Proof From the above observations it is simple to prove that it is only required to show that every alternating directed path in G has all type-1 arcs either labeled L or R. Since the proof of this fact is straight forward, it will be omitted. □

Using the subdiagram arrangement A_{11}, let us construct a subdiagram arrangement A_{12} as shown in Figure 11. The shadowed area in this subdiagram arrangement does not contain diagonals.

LEMMA 4.4 *The standard full layout corresponding to the subdiagram arrangement A_{12} constructed from the strip subdiagram given in Figure 7 is loop-free.*

Proof The proof follows from Lemma 4.3. □

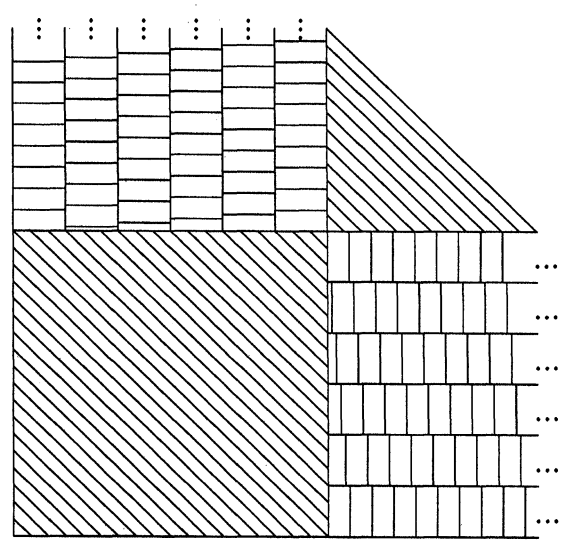

FIGURE 11 Strip subdiagram arrangement A_{12}.

THEOREM 4.1 *For any small $\varepsilon > 0$ there exists a knock-knee layout W such that under stretching scheme I any of its three-layer wirings W' has area $A(W') > (c_1-\varepsilon)\cdot A(W)$, where $c_1 = (6/5)$.*

Proof Consider the standard full layout corresponding to the subdiagram arrangement A_{12} of Figure 11. By Lemma 4.2 we know that it is loop-free. In this layout, except for 6·52 rows and 6·52 columns, every six adjacent rows and columns contains a sublayout that is not three-layer wirable (Theorem 2.1 and Lemma 4.2). Since the dimension of this layout can be arbitrarily large, we conclude that for any small $\varepsilon > 0$ there exists a knock-knee layout W such that under scheme I any three layer wiring W' for it has area $A(W') > ((6/5) - \varepsilon) \cdot A(W)$. This completes the proof for the theorem. □

5. A LOWER BOUND FOR THE AREA INCREASE FACTOR UNDER SCHEME II

To derive lower bounds for the area increase factor under stretching Scheme II, we need to find layouts with small dimensions for which legal

partitions do not exist and then use these layouts to construct a larger layout with certain structure. Consider an n-row by n-column diagonal diagram satisfying that (a) both of its upper left corner tile and lower right corner tile either do not contain diagonal or contain diagonals of the same type, (b) it does not admit any legal partition, and (c) its corresponding standard full layout is loop-free. We call such a diagonal diagram a *square subdiagram*. Let us arrange identical n-row by n-column square subdiagrams in such a way that the lower left corner of every subdiagram has x-coordinate $i \cdot n + j$ and y-coordinate $j \cdot n + i$, where i and j are integers. The arrangement restricted to the rectangle formed by the horizontal lines of y-coordinate value 0 and h and vertical lines of x-coordinate values 0 and w is shown in Figure 12. We call the arrangement restricted to this rectangle the *square subdiagram arrangement* A_2. By (a), we know that A_2 is a diagonal diagram of some full knock-knee layout. If the standard full layout corresponding to diagonal diagram A_2 is loop-free, then from (b) we know that this layout is not three-layer wirable. Note that condition (c) does not imply that the standard full layout corresponding to diagonal diagram A_2 is loop-free.

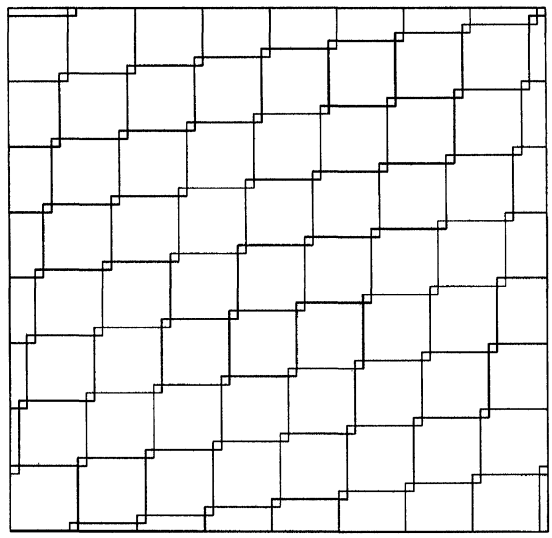

FIGURE 12 Square subdiagram arrangement A_2.

Suppose that the standard full layout corresponding to diagonal diagram A_2 is loop-free. We define a *window* in the arrangement A_2 as a rectangular region with boundary lines formed by tile edges of D. We define $t(u,n)$, for $u \geq n$, as the smallest integer v such that in the arrangement A_2 any u row by v column window contains at least one square subdiagram. By symmetry, the computation of $t(u,n)$ can be performed by only considering those windows whose lower left corners are located at tile vertices $(0, y)$, where $0 \leq y \leq n^2$. Therefore,

$$t(u,n) = \max_{0 \leq y \leq n^2} \left\{ \min_x \{x | \text{the window defined by } (0,y), (0,y+u), (x,y) \text{ and } (x,y+u) \text{ in } A_2 \text{ contains at least one } n\text{-row by } n\text{-column square subdiagram}\} \right\}$$

In any (wirable) division by Scheme II, if there is a sublayout with u rows there must be at least $\lceil (h/u) \rceil - 1$ horizontal division lines and there must be at least $\lceil w/(t(u,n)-1) \rceil - 1$ vertical division lines. Without loss of generality assume that $w = h$ and these values are large. Then, the area of the stretched wirable layout is about

$$\left(1 + \frac{1}{u}\right) \cdot \left(1 + \frac{1}{(t(u,n)-1)}\right) \cdot A(W),$$

and a lower bound for the area of the stretched wirable layout is given by

$$\min\left\{ \left[1 + \frac{1}{u}\right] \cdot \left[1 + \frac{1}{(t(u,n)-1)}\right] | u \geq n \right\} \cdot A(W).$$

To obtain a larger lower bound, a smaller $t(u,n)$ value is required; and a smaller $t(u,n)$ value can be derived only from a smaller value for n. Let us consider the square subdiagram shown in Figure 13, where $n = 10$.

LEMMA 5.1 *There is no legal partition for the diagonal diagram given in Figure* 13.

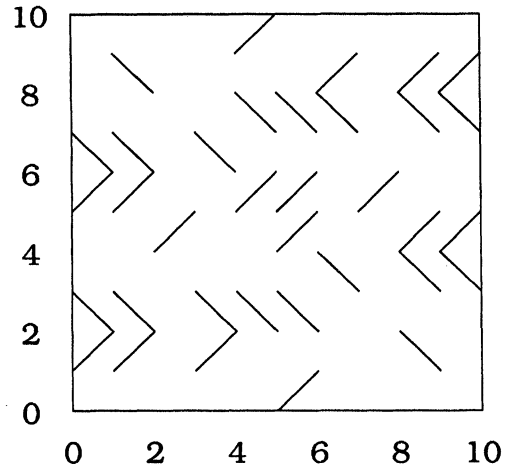

FIGURE 13 Square Subdiagram.

Proof The proof has similar structure as the one for Lemma 4.1. Since the proof includes too many details, it is given in the Appendix. □

LEMMA 5.2 *The standard full layout corresponding to the square subdiagram shown in Figure* 13 *is three-layer unwirable.*

Proof The standard full layout corresponding to the square subdiagram of Figure 13 is shown in Figure 14. Clearly there is no loop in this layout. By Lemma 5.1 and Theorem 2.1, this layout is not three-layer wirable. □

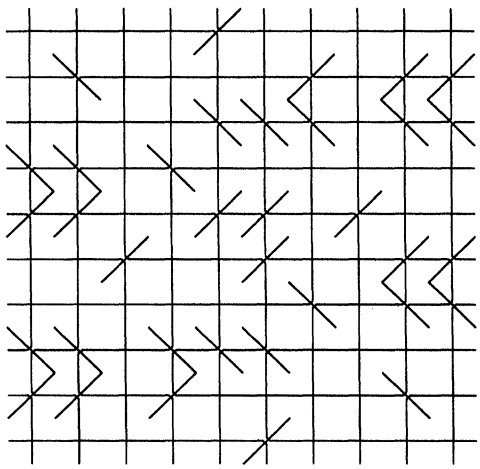

FIGURE 14 Standard full layout corresponding to the diagram in Figure 13.

Based on the above discussions, we establish the following Theorem.

THEOREM 5.1 *There exists a knock-knee layout W such that under stretching scheme II any of its three-layer wirings W' has area $A(W') \geq c_2 \cdot A(W)$, where c_2 is* 1.075630.

Proof Consider the subdiagram arrangement A_2. If we use the diagonal diagram of Figure 13 as the component subdiagrams, there are wire loops in the standard full layout corresponding to the arrangement. To eliminate loops we extend this 10-row by 10-column square subdiagram to a 11-row by 11-column square subdiagram shown in Figure 15. The standard full layout corresponding to this square subdiagram is shown in Figure 15. This layout does not contain any loop. From Theorem 2.1 and Lemma 5.2, we know that to complete the proof of the theorem we only need to show that there is no loop in the standard full layout corresponding to this subdiagram arrangement. The proof is not obvious. First let us show that there are no loops. In Figure 15, we label the wires in the layout corresponding to the square subdiagram. Let us now consider the wires in A_2.

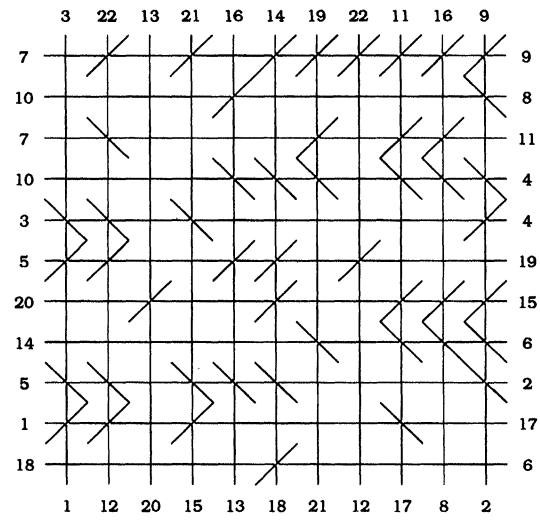

FIGURE 15 Extended diagonal diagram and its standard full layout.

We claim that there is only one type of global wires (see Fig. 16). These wires are formed by the repeated sequence of the wires

$$\ldots - 1 - 2 - \ldots - 21 - 22 - 1 - 2 - \ldots$$
$$-21 - 22 - 1 - 2 - \ldots$$

without any loop (Fig. 16). Therefore, no wire in A_2 has a loop. One can also modify the top row and right column of the diagonal diagram in Figure 15 to obtain a loopless A_2 diagram with two, three or even four different types of wires. We used the one in Figure 15 for convenience. The t values for the subdiagram arrangement are given in Table I. Therefore, $c_2 = 1.075630$ (the minimum is achieved for $u = 17$ and $t(u, n) = 64$).

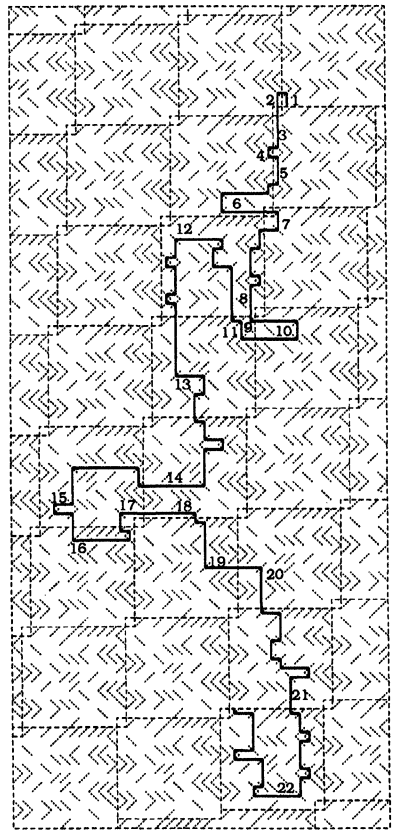

FIGURE 16 Global wire.

6. DISCUSSIONS

We considered two different layout stretching schemes for three-layer wiring knock-knee layouts. We showed the lower bounds 1.20 and 1.075630 for the area increase factor under stretching schemes I and II, respectively. The upper bound 4/3 for the approximation factors under scheme I by using the algorithms given in [4] and [8] is close to the lower bound 1.20 developed in this paper. The lower bound we found for the approximation factors under scheme II is much smaller than that for the scheme I. This provides "evidence" that smaller upper bounds for the stretched layout area may be obtained under scheme II. Several techniques for stretching and three-layer wiring are proposed in [8]. We believe that the combination of the two stretching schemes considered in this paper and some wiring techniques proposed in [8] may result in better wiring area upper bounds.

Let us now define the following four classes of knock-knee layouts

(a) Knock-knee layouts whose diagonal diagrams D_d are of degree greater than two.
(b) Knock-knee layouts whose diagonal diagrams D_d are of degree two.
(c) Knock-knee layouts whose diagonal diagrams. D_d are of degree two and the standard full layouts of the diagonal diagrams are loop-free.

TABLE I u and $t(u,11)$

u	11	12	13	14	15	16	17	18	19	20	21	≥ 22
$t(u, 11)$	130	119	108	97	86	75	64	53	42	31	20	≤ 20
$(1+(1/u))(1+(1/t(u,11)-1))$	1.1	1.09	1.09	1.08	1.08	1.08	1.0756	1.08	1.08	1.09	1.1	> 1.08

TABLE II Upper and lower bounds for stretching and three-layer wiring

	Scheme I		Scheme II	
Class	upper bound	lower bound	upper bound	lower bound
a	1.33	1.33	1.33	1.173
b	1.33	1.25	1.33	1.134
c	1.33	1.20*	1.33	1.075*
d	1.25	1.167*	1.25	1.060

(d) Knock-knee layouts whose diagonal diagrams D_d are of degree one.

In Table II we summarize the lower and upper bounds for stretching and wiring knock-knee layouts in these four classes. The upper bounds are derived in [4] and [8]. The lower bounds are derived [9], [10], and in this paper (for class (c)). An entry marked with a "*" means that the lower bound is with respect to any algorithm that obtains the wiring by partitioning the corresponding diagonal diagram of D_d^* and not D_d (see Corollary 2.1 in Section 2). It is worthwhile to note that the lower bounds for the wiring area under scheme II are much smaller than those for scheme I.

Acknowledgments

We wish to thank Donna J. Brown, Franco P. Preparata, Majid Sarrafzadeh and Ioannis Tollis for their comments and suggestions to earlier versions of this paper. The extended diagonal diagram given in Figure 15 was generated by a program running on UCSB's MEIKO CS-2.

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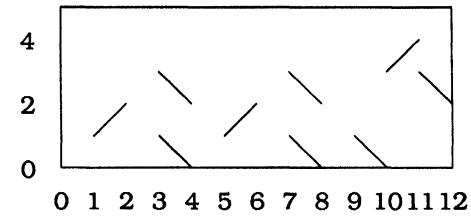

FIGURE 17 Basic component.

APPENDIX

To simplify our proofs of Lemma 4.1 and Lemma 5.1, we use the following conventions. We use the ordered pair (x, y) to refer to the tile vertex in D with coordinate values x, y. A horizontal line connecting two tile vertices (x_1, y_1) and (x_2, y_1) is referred to by $[(x_1, y_1), (x_2, y_1)]$. Similarly, a vertical line connecting two tile vertices (x_1, y_1) and (x_1, y_2) is referred to by $[(x_1, y_1),(x_1, y_2)]$. We use the notation "$S_1 \rightarrow S_2 \rightarrow \ldots \rightarrow S_k$" to mean that "statement S_1 holds; since S_1 holds, then S_2 holds; since S_1 and S_2 hold, then S_3 holds; ...; since statements $S_1,\ldots,S_{k-1}$ hold, then statement S_k holds". Let D_d be a diagonal diagram in layout domain D and let P' be a set of tile edges of D. We say that a tile vertex v in D is legally connected by P' if the number of segments from $D_d \cup P'$ incident at v is even, and there are no forbidden patterns that include v. Clearly, if P' is a legal partition of D_d in D, then all vertices in D must be legally connected by P'.

The proof of that there exists no legal partition for the strip subdiagram shown in Figure 7 is based on the proof that a basic component in it cannot be legally partitioned when some key partitioning lines are present (Lemma A).

LEMMA A *The diagonal diagram given in Figure 17 does not admit any legal partition which contains a horizontal partitioning line with vertex* (11,4) *as its right end point.*

Proof The proof is by contradiction. Suppose it has a legal partition P which contains a horizontal partitioning line with vertex (11,4) as its right end point. Depending how vertex (10,3) is legally connected in P there are two cases need to be considered.

Case 1 Vertex (10,3) is the right end point of a horizontal partitioning line, b, in P (Figs. 18 and 19).

Since vertex (7,3) is of degree one in the diagonal diagram, it must be the left end point of this horizontal line. There are two subcases, depending on how vertex (8,2) is legally connected in P.

Subcase 1.1 Vertex (8,2) is the left end point of a horizontal line, c, in P (Fig. 18).

$a = [(0,4),(11,4)]$, $b = [(7,3),(10,3)]$, and $c = [(8,2),(12,2)]$ are in $P \rightarrow$vertex (11,3) cannot be legally connected in P (Fig. 18). This contradicts the assumption that P is a legal partition.

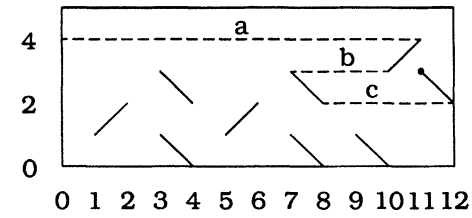

FIGURE 18 Subcase 1.1.

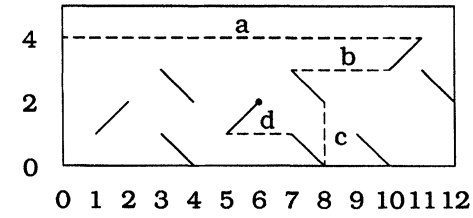

FIGURE 19 Subcase 1.2.

Subcase 1.2 Vertex (8,2) is the top end point of a vertical partitioning line, b, in P (Fig. 19).

$a=[(0,4),(11,4)]$, $b=[(7,3),(10,3)]$ and $c=[(8,0),(8,2)]$ are in $P\rightarrow d=[(5,1),(7,1)]$ is in $P\rightarrow$ vertex (6,2) cannot be legally connected in P (Fig. 19). This contradicts the assumption that P is a legal partition.

Case 2 Vertex (10,3) is the top end point of a vertical partitioning line, b, in P (Fig. 20).

$a=[(0,4),(11,4)]$, and $b=[(10,0),(10,3)]$ are in $P\rightarrow c=[(7,1),(9,1)]$ is in $P\rightarrow d=[(6,2),(8,2)]\rightarrow e=[(3,3),(7,3)]$ are in $P\rightarrow f=[(4,0),(4,2)]$ is in $P\rightarrow g=[(1,1),(3,1)]$ is in $P\rightarrow$ vertex (2,2) cannot be legally connected in P (Fig. 20). This contradicts the assumption that P is a legal partition.

In either case there is a contradiction. Therefore, the diagonal diagram given in Figure 17 has no legal partition which contains a horizontal partitioning line with vertex (11,4) as its right end point. □

Proof of Lemma 4.1 The proof is by contradiction and follows similar arguments as the one for Lemma A. For convenience, we divide the diagonal diagram given in Figure 7 into five sections by dotted lines shown in Figure 21 to 28. The rightmost section, which consists of two columns, is meaningless in the proof of Lemma 4.1. However, proofs of other lemmas in Section 4 are greatly simplified because of these additional columns. Three of these five sections are similar to the diagonal diagram shown in Figure 17. With the aid of figures and labels we shall give the skeleton of the proof and leave it to interested readers to verify correctness. Suppose it has a legal partition P. Since vertex (25,4) is of degree one in the diagonal diagram, there must be a partitioning line in P with vertex (25,4) as its end point. The possible partitioning line segments incident to vertex (25,4) are labeled a and shown in Figures 21, 22–26 , 27 or 28. Let us now consider these four different cases.

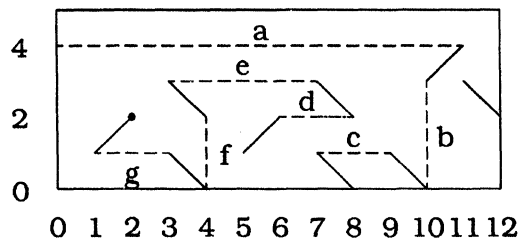

FIGURE 20 Case 2.

Case 1 Line segment a in Figure 21 with vertex (25,4) as its bottom end point is in P. The line segment a implies line segment b which in turns implies the conditions of Lemma A (Fig. 21). This contradicts the assumption that P is a legal partition.

Case 2 Line segment a in Figure 23–27 with vertex (25,4) as its top end point is in P. Now, vertex (24,3) can be legally connected in P by the line segment b in Figure 22 or in Figure 23–26.

Subcase 2.1 Line segment b in Figure 22 with vertex (24,3) as its top end point is in P.

This line segment implies line c which in turns implies the conditions of Lemma A (Fig. 22). This contradicts the assumption that P is a legal partition.

Subcase 2.2 Line segment b in Figures 23–26 with vertex (24,3) as its right end point is in P.

Now, vertex (20,4) can be legally connected in P by the line segment c in Figures 23–25 or in Figure 26.

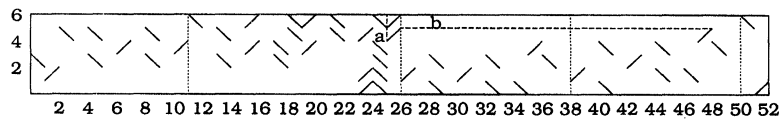

FIGURE 21 Case 1.

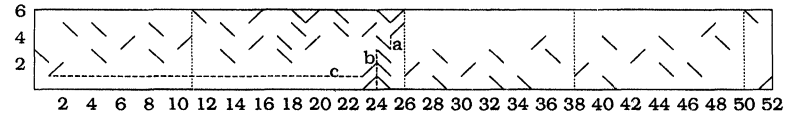

FIGURE 22 Subcase 2.1.

Subcase 2.2.1 Line segment c in Figures 23–25 with vertex (20,4) as its left end point is in P.

Now, vertex (21,5) can be legally connected in P by the line segment d in Figure 23, 24, or 25.

Subcase 2.2.1.1 Line segment d in Figure 23 with vertex (21,5) as its bottom end point is in P.

This line segment implies the line segment e (Figure 23). This in turn implies that vertex (23,4) cannot be legally connected in P (Figure 23). This contradicts the assumption that P is a legal partition.

Subcase 2.2.1.2 Line segment d in Figure 24 with vertex (21,5) as its right end point and left end point (18,5) is in P.

This line segment implies that vertex (19,4) cannot be legally connected in P (Fig. 24). This contradicts the assumption that P is a legal partition.

Subcase 2.2.1.3 Line segment d in Figure 25 with vertex (21,5) as its right end point and left end point (19,5) is in P.

This line segment implies the line segments e, f, g, h, i, j, k, l, and m (Fig. 25). These in turn imply that vertex (12,5) cannot be legally connected in P (Fig. 25). This contradicts the assumption that P is a legal partition.

Subcase 2.2.2 Line segment c in Figure 26 with vertex (20,4) as its bottom end point is in P.

This line segment implies the line segment d (Fig. 26). Arguments similar to the ones in Subcase 2.2.1.3 can be used to obtain a contradiction (Fig. 26).

Case 3 Line segment a in Figure 27 with vertex (25,4) as its right end point is in P.

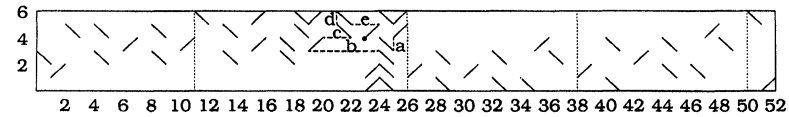

FIGURE 23 Subcase 2.2.1.1.

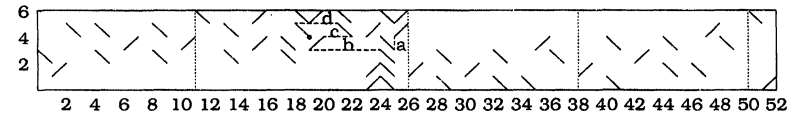

FIGURE 24 Subcase 2.2.1.2.

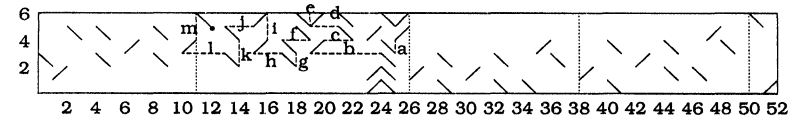

FIGURE 25 Subcase 2.2.1.3.

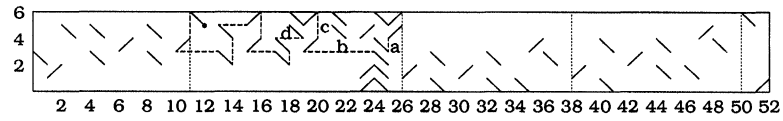

FIGURE 26 Subcase 2.2.2.

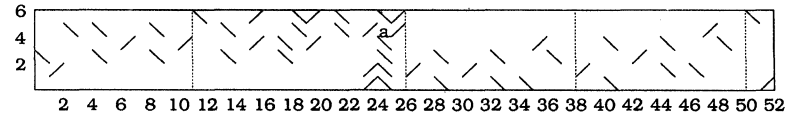

FIGURE 27 Case 3.

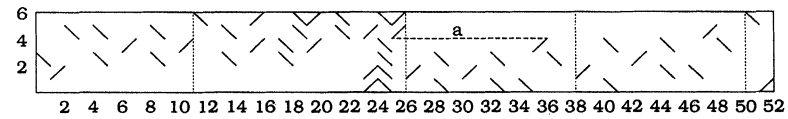

FIGURE 28 Case 4.

The remaining part of the proof follows similar arguments to the ones in case starting with the degree one vertex (24,3).

Case 4 Line segment a in Figure 28 with vertex (25,4) as its left end point is in P. This line segment implies the conditions for Lemma A (Fig. 28). By Lemma A, P is not a legal partition. This contradicts the assumption that P is a legal partition.

Since P does not satisfy any of the cases, it must be that there is no legal partition for the diagonal diagram D_d given in Figure 1. □

Proof of Lemma 5.1 The proof is by contradiction. Suppose it has a legal partition P. Since vertex (5,5) is of degree one, there must be a partitioning line in P with vertex (5,5) as its end point. Since the diagonal diagram is symmetric, it is sufficient to consider only the case when there is a vertical line, a, in P with vertex (5,5) as its left end point. Since vertex (6,4) is of degree one, there must be a partitioning line in P with vertex (6,4) as its end point. There are two cases, depending on how vertex (6,4) is legally connected in P.

Case 1 Vertex (6,4) is the left end point of a horizontal line, b, in P (Fig. 29). The right end point of this horizontal line is (10,4) as

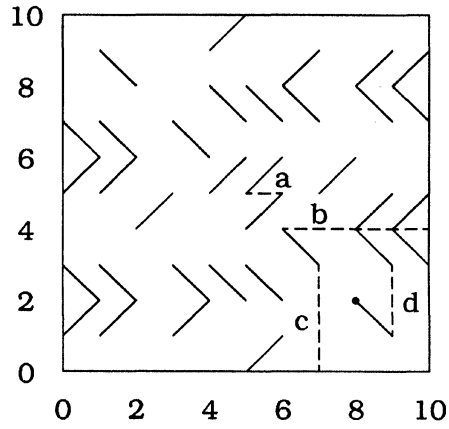

FIGURE 29 Case 1.

otherwise there is a forbidden pattern. $b=[(6,4),(10,4)]$ is in $P \rightarrow c=[(7,0),(7,3)]$ is in $P \rightarrow d=[(9,1),(9,3)]$ is in $P \rightarrow$ vertex (8, 2) cannot be legally connected in P (Fig. 29). This contradicts the assumption that P is a legal partition.

Case 2 Vertex (6,4) is the top end point of a vertical line, b, in P (Figs. 30 and 31). Since vertex (6,2) is of degree one, it must be the bottom end point of this vertical line. There are two subcases, depending on how vertex (5,2) is legally connected in P.

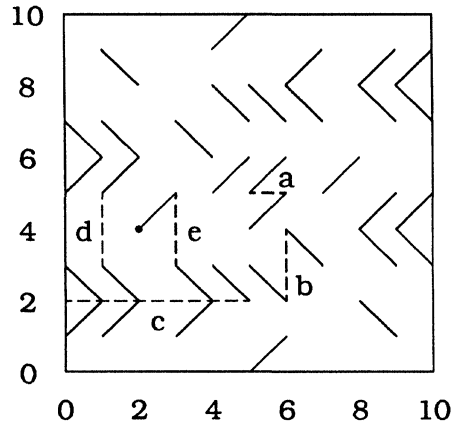

FIGURE 30 Subcase 2.1.

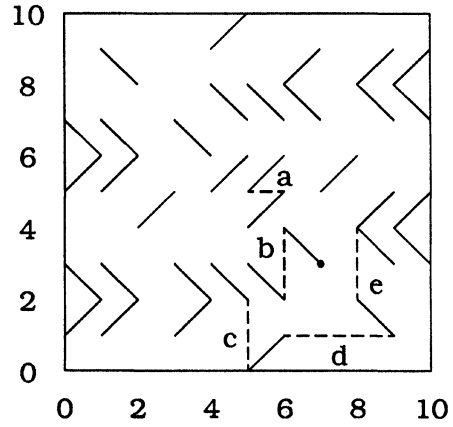

FIGURE 31 Subcase 2.2.

Subcase 2.1 Vertex (5,2) is the right end point of a horizontal line, c, in P (Fig. 30).

The left end point of this horizontal line must be (0,2) as otherwise there is a forbidden pattern. $c=[(0,2),(5,2)]$ is in $P \rightarrow d=[(1,3),(1,5)]$ is in $P \rightarrow e=[(3,3),(3,5)]$ is in $P \rightarrow$vertex (2,4) cannot be legally connected in P (Fig. 30). This contradicts the assumption that P is a legal partition.

Subcase 2.2 Vertex (5,2) is the top end point of a vertical line, c, in P (Fig. 31). $b=[(6,2),(6,4)]$ and $c=[(5,0),(5,2)]$ are in $P \rightarrow d=[(6,1),(9,1)]$ is in $P \rightarrow e=[(8,2),(8,4)]$ is in $P \rightarrow$vertex (7,3) cannot be legally connected in P (Figure 31). This contradicts the assumption that P is a legal partition.

Since in all cases there is a contradiction we conclude that the diagonal diagram given in Figure 13 has no legal partition.

Authors' Biographies

Teofilo F. Gonzalez was born in Monterrey, Mexico in 1948. He received the B.S., degree in Computer Science from the Instituto Tecnologico de Monterrey (1972) and the Ph.D., degree in Computer Science from the University of Minnesota, Minneapolis, (1975). Currently, he is Professor of Computer Science at the University of California, Santa Barbara. His major research interests are in the design and analysis of algorithms, computational aspects of computer aided design, and scheduling theory.

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