

Transient Phenomena in High Speed Bipolar Devices

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A new numerical method is applied to the analysis of the charge partitioning in the quasi-neutral base of a BJT. The results show that the conventional, 1:2 collector/emitter partitioning is not valid in general. High level injection increases the collector fraction, whilst fast switching decreases it.

Keywords: BJT capacitance, transient semiconductor device simulation

1. INTRODUCTION

As shown in [1], the charge partitioning may significantly affect device delay times. Non-Quasi-Static (NQS) BJT modeling [2] also demonstrates the practical importance of such effects in modern devices. The ever increasing speed of microelectronic devices [3, 4, 7] requires the development of more accurate models to describe transient behavior.

Papers [1, 2] are based on "first order" NQS corrections. Although the latter approaches are significantly different, they are similar in their use of the quasi-static approximation for the charge partitioning factor in the quasi-neutral base (QNB). The accuracy of the NQS method [2] is higher since it takes into account a delay in the QNB charge, not only in the collector current.

In the present paper we use an exact, 2D numerical technique, for the evaluation of the charge partitioning in semiconductor devices [5]. It is applied here to study the partitioning of the QNB charge (related to the diffusion capacitances of a BJT). The numerical method allows the separation of the charges into quasi-neutral and space charge components, and the extraction of the transient components of terminal currents, responsible for changes in the device internal charge.

Previous results, obtained for a 1D *pn*-diode [5], demonstrated a dramatic change of the charge partitioning of the charge injected into the quasi-neutral region depending on the ramp speed. It was shown that the injection level strongly influenced the charge partitioning which could exceed 0.6 of the net base charge in very high level

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injection. In contrast, in low level injection, a partitioning of 0.33 is obtained which agrees well with the conventional diffusion theory. A similar trend was noticed in [2] where small-signal 1D analysis of a BJT was performed (α_m parameter in Fig. 4, [2]). Charge-based models e.g., those stemming from [8, 9] are preferred to describe transient device behavior and there has been renewed interest in charge partitioning [1, 10–21].

The majority of authors [1, 10–21] have addressed the partitioning problem using simplified analytic methods. Analytic models, such as those proposed for MOSFETs [10, 11] and BJTs [12, 13, 15, 16, 18, 19] provide charge conserving, partitioned charge descriptions. Analytic models, based on first or higher order, non-quasi-static, solutions of the continuity and transport equations have also been proposed [12, 17, 20, 21]. To obtain closed form expressions, useful for device models, such analysis requires a significant number of simplifying assumptions.

A numerical techniques needed to extract the various charge/current components, necessary to accurately characterize the charge partitioning, have been developed recently [5]. These techniques were implemented in TRASIM [22] which provides an accurate, stable, and rapidly convergent, time-dependent, numerical solution of the two-dimensional Poisson and continuity equations, for specified, time dependent boundary conditions. The numerical results show that there are significant differences between the exact charge partitioning and the predictions of the analytic models.

Both the present and previous analytic models are based on the conventional, drift-diffusion model for carrier transport. The numerical analysis confirms the validity of this approach in BJTs, since the electric fields (or Fermi-level gradients) remain modest, at even the highest switching speeds.

Non-the-less, the Ohmic electric fields, associated with the removal of the neutralizing, majority carriers, are large enough to cause major changes in the minority carrier partitioning. Such effects are completely omitted in analytic models.

2. DEPLETION AND DIFFUSION CHARGES

Conventional device models associate the motion of the space-charge region boundaries with charge storage in a “depletion capacitance”, and the storage of minority carriers in quasi-neutral regions with a “diffusion” capacitance. A conventional numerical model provides no such distinction. The total charge for each carrier type must be split into a) a space-charge part, corresponding to a depletion capacitance and b) a quasi-neutral part, corresponding to a diffusion capacitance.

The extraction of the space charge and quasi-neutral charge have been described in detail earlier [5]. Following the methods described in [5] the depletion and diffusion charges are found from

$$Q_{n,p}^{\text{dep}} = \int_{\Omega} \rho_{n,p}^{\text{sc}} dx dy, \quad Q_{n,p}^{\text{dif}} = \int_{\Omega} \rho_{n,p}^{\text{qn}} dx dy \quad (1)$$

where Ω is the computational domain. The charges defined in Eq. (1) represent only the changes in the device charges/carrier concentrations that occur as a result of the applied switching ramp.

3. THE PASS-THROUGH CURRENT

It is necessary to compute the “pass-through” current [5], defined as the current that would flow across the device if the instantaneous bias and the instantaneous, transient internal potential distribution were held constant (c.f. “convective current” in [23]). The time dependent pass-through current must be subtracted from the terminal currents since it does not contribute to changes in the stored charges.

The “pass-through” current J_n^{pt} and J_p^{pt} are computed in a separate series of iterations, solving only the steady state, non-linear continuity equations

$$\nabla J_n^{pt} = qR; \quad \nabla J_p^{pt} = -qR. \quad (2)$$

During a fast transient, or as a result of high level injection, the electrostatic and majority carrier

quasi-Fermi potential distributions $\psi(x, y)$ and $\varphi_p(x, y)$ change during the transition. It is insufficient to merely interrupt the changes in terminal voltages and to then compute the conventional steady-state current.

For even a very slow transient errors arise: Although the change in the potential distribution will be smaller, the integration time is increasing and still leads to an erroneous calculation of the partitioning. Unfortunately the effects of internal potential variation, imply also that the conventional “steady-state” part of a circuit model is no longer adequate to predict the corresponding terminal currents.

Integration of the solutions of Eq. (2) over the device contacts, gives $\sum_{k=1}^{N_c} J_k^{pt} = 0$. The total charge, arriving at the k -th terminal is defined as $Q_k(t) = \int_0^t (J_{c,k}(t') - J_{e,k}^{pt}(t')) dt'$.

4. SIMULATION RESULTS

The modifications described above were implemented in TRASIM [22], and the modified version of TRASIM used for transient 2D numerical simulation of a CML BJT [4]. Depending on the functional purpose of the transistor and the desire to increase speed of the ECL circuit, the transistor may operate in a high current mode, causing high level injection. Rather few papers have been published on the high injection behavior of the BJT (e.g. [6]). We believe that only thorough numerical investigation will shed light on the highly nonlinear, transient problem.

4.1. Device Structure

The transistor structure is shown in Figure 1 (we follow the data and SEM photograph from [4]). Only one half of the transistor is simulated to reduce the computational burden. The depth of the buried layer was $0.575 \mu\text{m}$, having Gaussian impurity distribution with exponent of $0.1 \mu\text{m}$ and peak concentration of 10^{19}cm^{-3} . The selectively epitaxially grown active collector has impurity

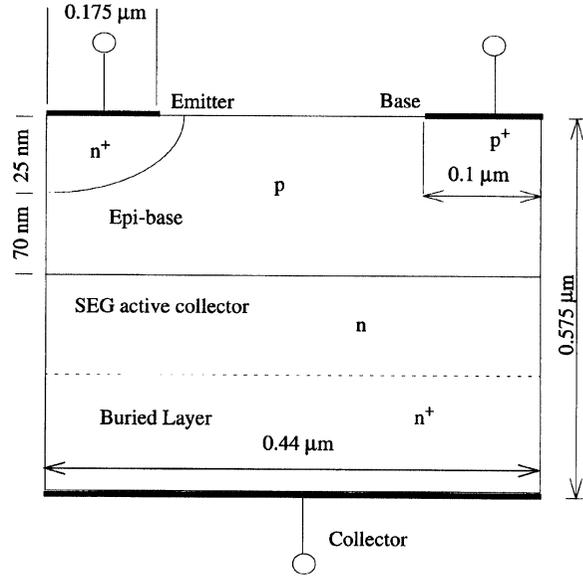


FIGURE 1 Simulated BJT structure.

concentration of $1.8 \cdot 10^{17} \text{cm}^{-3}$. The epitaxial base layer has a concentration of $2.5 \cdot 10^{18} \text{cm}^{-3}$ and width of 70nm . The polysilicon emitter was modeled by a surface recombination 10^4cm/s , effective p - n junction depth of 25nm and a half emitter with an area of $0.175 \mu\text{m}$ and $0.35 \times 2.6 \mu\text{m}^2$ respectively. SRH, Auger and high doping effects were taken into account. This device shows β about 95 and I_C of 1mA at $V_{EB}^0 = -0.92$ and $V_{CB} = 2 \text{V}$ which matches the experimental data [4].

4.2. Charge Partitioning for Different Injection Levels

The transients were simulated at $V_{CB} = 2 \text{V}$ with V_{EB} switched from V_{EB}^0 to 0V with a linear ramp of duration τ_r seconds. The collector charge fraction P_C was calculated from $P_C = Q_C(t) / (Q_C(t) + Q_E(t))$, where $Q_E(t)$ and $Q_C(t)$ are charges recaptured at the emitter and collector terminals respectively after time t . Figure 2 shows the time evolution of the dynamical charge partitioning of the QNB charge. As we see, increasing the injection level leads to a bigger

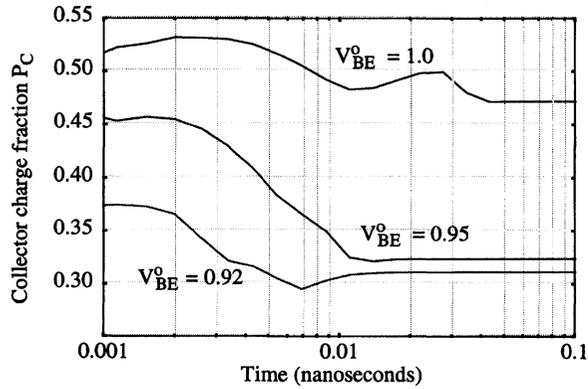


FIGURE 2 Charge partitioning for different injection levels $\tau_r = 0.01$ ns.

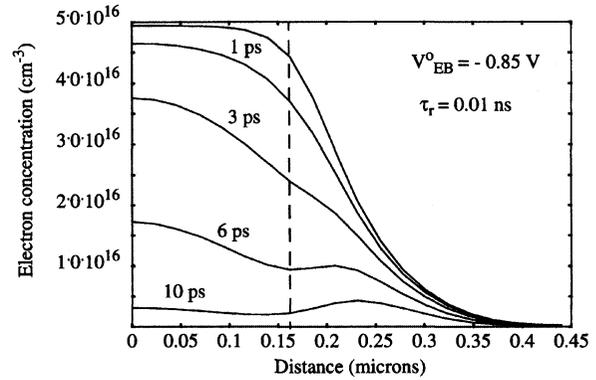


FIGURE 3 Electron density profile across the current flow in the QNB.

collector charge fraction. This effect is due to the built-in electric field in the QNB associated with the high injection level and the extraction of the compensating majority carriers.

Figure 3 shows 2D effects present when discharging the base of the transistor, in low injection. The vertical dashed line in the Figure 3 shows the “current channel boundary”. Electrons injected outside this channel are diverted to the collector rather than to the emitter. After switching-off the transistor they are collected by the collector effectively increasing the collector fraction.

4.3. Charge Partitioning for Different Ramp Speeds

Figure 4 shows the dynamical charge partitioning of the QNB charge for different ramp speeds at $V_{EB}^0 = -0.95$ V. Increasing ramp speed leads to smaller collector charge fraction which is consistent with the earlier results for a *p-n* diode [5]. This effect is due to the transient electric field in the QNB caused by the hole current.

Figure 5 shows the vertical component of the electron current density during transient for a slow and fast ramps under high level injection. The lateral electric field, caused by the fast base discharge, pinches the electron current flowing from the emitter to the collector, leading to a non-

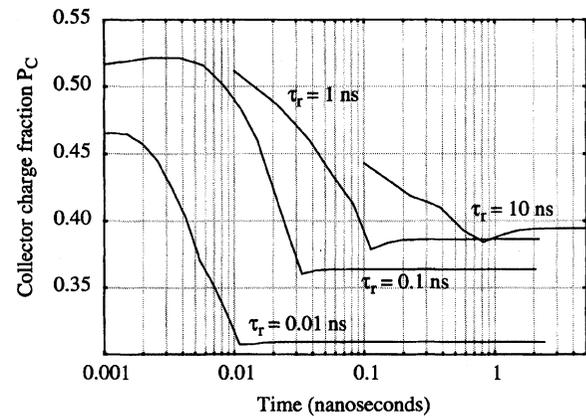


FIGURE 4 Charge partitioning for different ramps, $V_{EB}^0 = -0.95$ V.

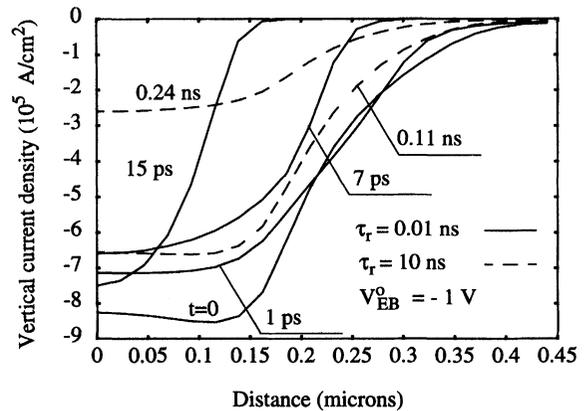


FIGURE 5 Vertical current density component for a slow and fast transient.

monotonic dependence of the electron current density underneath the center of the emitter. For the slow transients the current density profiles retain their shape during the transient.

CONCLUSIONS

A number of different BJT operating conditions were simulated. Some results depend on the device structure, nevertheless a few general conclusions seem to be possible at this point:

- i) At low level injection charge partitioning deviates from the theoretical 1:2 collector:base partition due to the 2D effects.
- ii) In a high current mode, when high injection occurs, the resulting electric built-in field the QNB leads to a collector charge partition that grows with V_{BE} .
- iii) The ramp speed affects charge partitioning in both high and low injection level by effectively reducing the collector charge fraction at faster ramps.

It is not possible draw comparisons with [6] which models a device of base width 200 microns and zero recombination.

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Michael S. Obrecht received his M.Sc. (Physics and Applied Mathematics, 1975) and Ph.D. (Theoretical Physics, 1983) degrees from the Novosibirsk State University, Russia. He has worked in the area of semiconductor device numerical modeling for the last 14 years. In 1991 he joined Electrical and Computer Engineering Department of the University of Waterloo as a Research Associate Professor. Since 1994 he is also with Siborg Systems Inc. He has authored and coauthored over 20 papers and developed software tools for two-dimensional process-simulation which are used worldwide. Recently Dr. Obrecht is developing numerical algorithms and software tools for steady-state and transient, 2D/3D semiconductor device simulation.

Professor Heasell graduated in Physics (BSc.) and Electrical Engineering (Ph.D.), from Imperial College, London. As a research associate at AEI, Rugby he studied high current silicon rectifiers, before returning the EE.Dept. at Imperial College. His early research was directed to the study of 3–5 materials and especially InSb. On joining Waterloo the latter interest gave way to silicon device processing and modeling. His interests remain the analytical and numerical study of silicon devices.

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