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On Self-Checking Design of CMOS Circuits for Multiple Faults

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A technique for designing totally self-checking (TSC) FCMOS (Fully Complementary MOS) designs for multiple faults is presented in this paper. The existing techniques for self checking design consider only single faults, and suffer from high silicon area overhead. The multiple faults considered in this paper are multiple breaks, multiple transistors stuck-offs and multiple transistors stuck-ons. Starting from FCMOS design, small modifications (addition of two-weak transistors) make the original circuit totally self-checking. Experiemntal results show the overhead, delay and power consumption for the proposed technique. This paper also presents a technique for designing multistage TSC FCMOS circuits.

Keywords: Self-checking, on-line detection, stuck-off and stuck-on transistor faults, CMOS

1. INTRODUCTION

The increasing complexity of VLSI circuits has made it expremely difficult to detect faults in such circuits. The large transistor count in present day circuits also makes the presence of multiple faults more probable. Off-line testing methods like Built In Self Test (BIST), add significant overhead to the functional circuit. Also test time is increased. Totally Self Checking (TSC) circuits are very desirable for implementing highly reliable VLSI systems. Such circuits can indicate the presence of a fault during their normal operation [7].

The design of TSC systems is currently aimed at detection of single stuck-at faults. This may be sufficient at the gate level where most of the TSC and BIST techniques are used. Relistic modeling of defects in VLSI circuits, can be done only at the transistor level, since only at this level is the complete circuit structure known [2, 14]. This make it necessary for TSC design techniques to be developed for circuits at the transistor level.

Currently, CMOS is the dominant circuit technology for implementing VLSI systems. A FCMOS gate, shown in Figure 1, consists of complementary P and N networks. It has been established that breaks, stuck-on transistor faults constitute a significant portion of the faults occuring in CMOS circuits [2]. This work is aimed at the detection of such faults.

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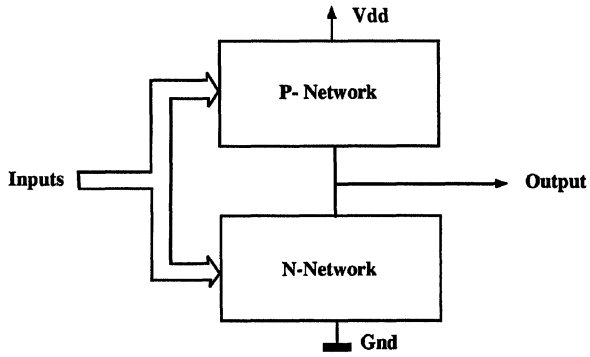

FIGURE 1 FCMOS gate structure.

Break faults are caused by missing conducting material [3]. Break defects in CMOS circuits can be of two kinds e.g., intra-gate breaks and signal line breaks. Figure 2 shows possible break defects in a typical FCMOS circuit. Intra-gate breaks occur internal to a gate e.g., break between source and drain, break in metal contacts to drain, breaks in diffusion region etc. Signal line breaks occur in the gate of the transistor. A signal line break can also cause a transistor to behave as a stuck-on transistor [3]. Thus, successful detection of break faults requires the detection of stuck-on transistor faults as well. An intra-gate break may cause the output to either float or to remain at an incorrect value. Capacitive coupling between adjacent nodes may further complicate the situation [13]. A floating node, being ambiguous, should not be allowed to occur in any circuit. Stuck-on transistors in a FCMOS circuit can cause a direct conducting path between Vdd and GND. This will results in abnormal bus currents and may cause a total failure of the circuit. Stuck-offs are very similar to breaks in that in either case the transistor network becomes incapable of creating a conduction path between the supply and the output node for certain input conditions.

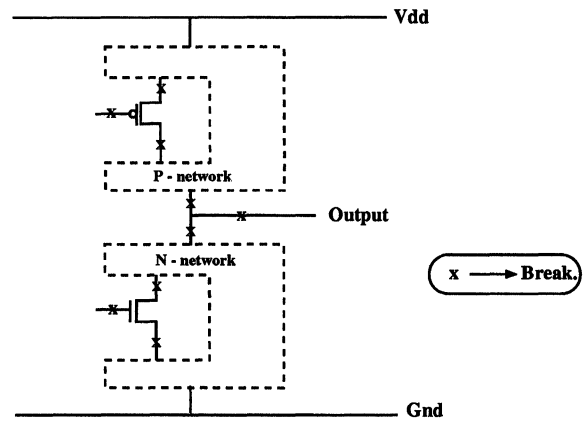

FIGURE 2 Typical breaks in a FCMOS circuit.

2. CONCEPTS OF SELF-CHECKING CIRCUITS

Self-checking circuits provide a very cost effective method of fault detection [7]. Such circuits are designed so that for valid inputs they either provide correct outputs or indicate the presence of a fault by producing non-codewords. The outputs of self checking circuits are encoded such that any fault affecting the outputs will produce an invalid code word.

The following definitions are important in the context of this work [7].

Fault Secure: A circuit is said to be fault secure for a given set of faults, if for any fault in the set, the circuit never produces an incorrect code word at the output for the input code space.

Self Testing: A circuit is self testing, if for every fault from a given set of faults, the circuit produces a non-code word at the output for at least one input code word.

Totally Self Checking: A circuit is said to be totally self checking if it satifies both the above properties. i.e., it is both fault secure and self testing.

3. SELF CHECKING FCMOS CIRCUIT DESIGN

Most of the published work in FCMOS testability considers only gate level designs. Some amount of

work on testability has also been reported at the transistor level [4, 6, 10–12]. Relatively little work has been done on self-checking CMOS circuit design [1, 5, 8]. Cheema *et al.* presented a technique for TSC FCMOS circuits for single transistor stuck-on and stuck-off faults [1]. It considers only single stuck-on and stuck-off transistor faults, and requires up to six test transistors per complex gate as well as an extra clock input. Thus, there exists a need for a more efficient TSC FCMOS circuit design technique at the transistor level.

A TSC design technique should be capable of detecting a significant proportion of faults occurring in practical circuits. The invalid output generated due to a fault should also propagate to the final output in case of multistage FCMOS circuits. This enables the detection of multiple faults in the composite circuit. It is also possible that a fault may cause both the networks of a FCMOS gate to turn on simultaneously. Therefore, the circuit has to be designed such that the creation of a low resistance path between the supply nodes is avoided. Other important criteria of a good TSC FCMOS design technique include minor modification of the original circuit with small number of extra transistors, limited degradation in performance (time delay), and full testability for the extra transistors. The design technique proposed in this paper satisfies all the above mentioned criteria.

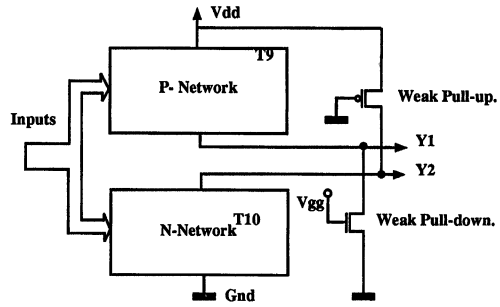

FIGURE 3 A TSC FCMOS gate structure.

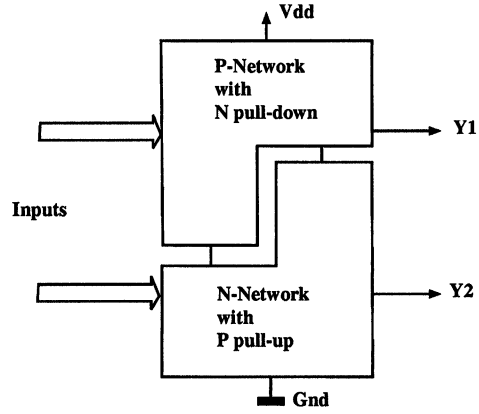

FIGURE 4 Block diagram of a TSC FCMOS gate.

4. PROPOSED DESIGN TECHNIQUE

The augmentation of a normal FCMOS complex gate to obtain a TSC version involves the addition of two test transistors. The general structure of the modified gate is shown in Figure 3. The two networks of the complex gate have been separated to generate the two outputs Y1 and Y2. The outputs Y1 and Y2 will always be at the same logic value for a fault-free circuit. If the outputs Y1 and Y2 have complementary values, the circuit is assumed faulty. Figure 4 shows the general block diagram of a TSC FCMOS gate. As each output (Y1 and Y2) should have the ability to take on both logic values (1 or 0), the P-network (N-network) should have a corresponding pull-down (pull-up) part. This requires the addition of two weak transistors which remain permanently on, as shown in Figure 3. The weak pull down transistor is fed with a gate voltage of 2 V to 2.5 V. This ensures that the voltage levels are proper at output Y1. This voltage (Vgg) can be generated internal to the chip. A weak transistor affects the output only if the network associated with it is turned off. Weak transistors are formed by fabricating a transistor with a high L/W (length to width) ratio [9], or by using high resistivity semiconductor material for the channel.

The proposed technique covers the following three fault sets:

1. All single breaks or struck-ons or struck-offs in any transistor in the circuit.
2. All multiple breaks and stuck-offs transistor in the functional circuit i.e., multiple break or stuck-off faults which include the weak transistors are not included.
3. All multiple stuck-on transistors.

The phrase 'fault set' will apply to any of the above three sets. However, faults from only one of the sets will be assumed to be present at any time.

5. EXAMPLE : A TSC FCMOS COMPLEX GATE

A FCMOS complex gate (Fig. 5a) has been modified to incorporate TSC capabilities and is shown in Figure 5b. Transistors T9 and T10 are weak transistors. T9 is a weak PMOSFET and T10 is a weak NMOSFET. The gate of T10 is maintained at Vgg = 2.5 V. The W/L ratios of the weak transistors are determined by taking into consideration the effective W/L ratios of the P and N networks. The weak transistors T9 and T10

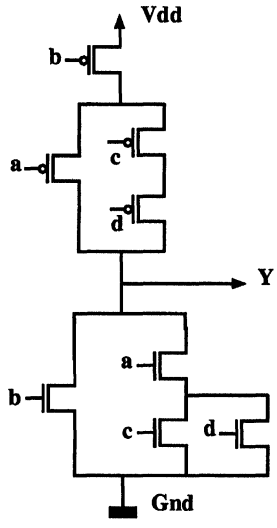

FIGURE 5a A FCMOS complex gate.

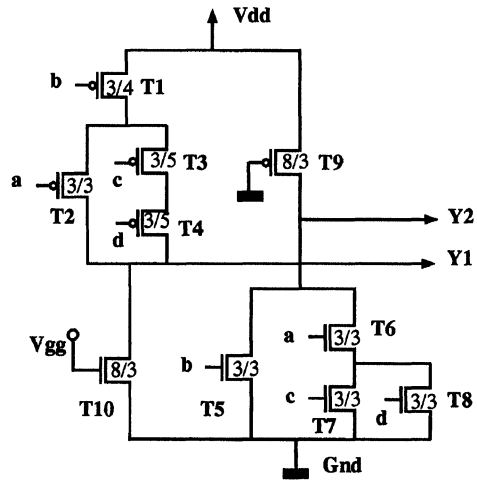

FIGURE 5b The TSC version of Figure 5a.

affect the outputs Y2 and Y1 respectively, only when the networks associated with them (N and P respectively) are off. The worst case delay input patters i.e., input patterns which turn on the maximum number of transistors in series, has to be considered to determine the L/W values of the weak transistors [9]. For the circuit shown in Figure 5b the worst case input patterns are **abcd = 1000** and **abcd = 1010**, for the N and P weak transistor respectively. If T10 and T9 transistors are made very weak, the fall time and the rise time of outputs Y1 and Y2 will be unacceptably high. On the other hand, T10 and T9 have to be weak enough (large on-resistance) to make high voltage of Y1 acceptable (greater than 3.7 V) and low voltage of Y2 acceptable (less than 0.5 V). The L/W ratio for each transistor is chosen as shown in Figure 5b.

It is assumed here that the complex gate shown is the first stage of composite circuit. The inputs to the P and N networks have therefore been connected together. They would have been separated if the complex gate was used as an intermediate stage.

THEOREM I *A fault-free FCMOS circuit, augmented as shown in Figure* 3, *will always produce correct outputs* (11 *or* 00) *for any input pattern.*

Proof The networks of a FCMOS gate are designed such that any input pattern will always turn on only one of the networks [9]. We consider the following two cases.

Case I Input combination that turns on the *P*-network. The *N*-network will obviously be off in this case. The *P*-network being on, causes the Y1 to be connected to Vdd. The *P*-network is also able to overcome the pull-down effect of weak transistor T10. The *N*-network being off, does not affect Y2. Weak transistor T9 is able to pull up Y2 to a logic 1. Thus, we get a value Y1Y2 = 11. For example, **abcd = 0011** turns on the *P*-network through T1 and T2. The *N*-network is off and Y1Y2 = 11.

Case II Input combination that turns on the N-networks. The *N*-network pulls Y2 down to 0 overcoming the weak pull-up offered by T9. The P-network being off, allows weak transistor T10 to pull down Y1 to a logic 0. The output value of Y1Y2 = 00 is obtained in this case. For example, **abcd = 0100** causes the *N*-network to turn on via T5. The *P*-network is off due to T1 being off, and hence Y1 Y2 = 00. Thus, a fault-free TSC gate always produces valid outputs (11 or 00). QED.

THEOREM II *A FCMOS circuit, augmented as shown in Figure* 3, *will always produce either a correct output* (00 *or* 11) *or an invalid output* (01 *or* 10), *when faults from the given sets, are presented in the circuit.*

Proof A path between a supply node and an output is said to be activated by an input pattern, iff all the transistors in that path are turned on. A break or a stuck-off fault is sensitized when the input patterns attempts to activate the path (from a supply node through the fault to an output), and de-activate all other paths to that particular output. In other words, the output will be pulled down or up only through the activated path. A stuck-on transistor fault is sensitized when an input pattern attempts to turn on all the transistors in a path (from a supplied node through the stuck-on transistor to an output) except the stuck-on transistor itself and de-activate all other paths in the same network. A fault affects an output iff it is sensitized by an input pattern. It is assumed that the circuit is irredundant i.e., for every fault there exists at least one input pattern which can sensitize it.

The proposed technique considers three different types of faults e.g. breaks, stuck-on transistors and stuck-off transistors. Each fault set (Section 4) will be considered individually by first proving the fault secure property then the self-testing property.

Case I: All single breaks/stuck-ons/stuck-offs Outputs Y1Y2 being equal implies one network being on and the other network off. For a single fault to cause the outputs to change from 11 to 00 or vice versa, the off-network has to be turned on and the on-network has to be turned off simultaneously, thereby affecting both outputs Y1 and Y2. A break or struck-off fault in the functional circuit can only turn a network off. A stuck-on fault in the functional circuit can only cause a network to turn on. Thus, no single fault in the functional circuit can affect both networks outputs since the two sections are disjoint as shown in Figure 3. Thus, the modified FCMOS gate is fault secure for single faults in the circuit.

To prove the self-testing property, each type of fault is considered separately. Let us consider first single break or stuck-off faults. Since the circuit is irredundant, there exists an input pattern that sensitizes a single break or stuck-off. For such an input, both networks will be off, causing Y1Y2 = 01. Therefore, the proposed circuit is self-testing for single break and transistor stuck-off fault.

Let us now consider the case where a single transistor is stuck-on. An input pattern which sensitizes this fault will cause the network containing it to turn on instead of turning it off. The other network is also turned. Thus, we have a case with both the networks remaining on causing an output Y1Y2 = 10. In other words, the circuit is also self-testing for transistor stuck-on faults. It may also be possible for either one or both of the weak transistors to get disconected from the circuit due to a break or a stuck-off fault. When this occurs,

the output node associated with the faulty weak transistor does not get a path to discharge. This causes that particular node Y1 or Y2 to be stuck at a value of 1 or 0 respectively. Any pattern which causes the network associated with the faulty weak transistor to turn off, will result in an invalid output of Y1Y2 = 10 or 01. The weak transistors are permanently on. Hence, a stuck-on fault does not affect them. Thus the circuit is self-testing for all single faults. Since the circuit is both fault secure and self-testing, it is TSC for this case.

Case II: All multiple breaks and stuck-offs in the functional circuit No multiple break or stuck-off transistor can cause the output of the circuit to change from 11 to 00 vice versa. To do so, the fault must turn on one network and turn off the other simultaneously. No breaks or stuck-off faults can cause an off-network to turn on. In other words, multiple break faults and stuck off transistor faults cannot cause incorrect outputs. Thus, the circuit is fault secure.

A given input pattern can only turn on one of the networks. The input pattern may sensitize more than one break or stuck-off fault (along the same path). This has the same effect as a single break or stuck-off fault in that path. We have already proved (case I) that for a single break or stuck-off fault in a path the circuit is TSC. Multiple breaks and stuck-off transistor faults are detected by an input pattern, if any one of them is on the activated path. Hence, the circuit is self testing. Thus, the circuit is TSC for case II.

Case III: All multiple stuck-ons No multiple stuck-on transistor fault can cause the output of the circuit to change from 11 to 00 or vice versa. To do so, the fault must turn on one network and turn off the other simultaneously. No stuck-on fault can cause an on-network to turn off. In other words, multiple stuck-on transistors cannot cause incorrect outputs. Thus, the circuits is fault secure for this case.

A given input pattern can only turn on one of the networks. The input pattern may sensitize more than one stuck-on transistor fault (along the same path). This has the same effect as a single stuck-on transistor fault in that path. We have already seen in case I that a single stuck-on transistor in a path is detected. Multiple stuck-on transistor faults in the same path are sensitized and detected by an input pattern if the pattern turns on all transistors in that path except the faulty ones. The circuit is thus, self testing for this case. Thus, the circuit is TSC for case III. QED.

6. SIMULATION RESULTS

The layout of the original circuit, created using MAGIC (VLSI layout editor), was modified to obtain the layout for the TSC circuit of Figure 5b. The two transistors were appended to the circuit with minimal modifications to the original layout. The transient simulation of the original and the modified circuit were carried out using CaZm (circuit analyzer and timing simulator). The plots of the input and output waveforms are shown in Figure 6. The inputs in Figure 6 are given for the worst case time delays and logic levels for the outputs. For example, as discussed before, the worst case for logic level '1' on output Y1 is when ABCD = 1000. i.e., input pattern which turns on the maximum number of transistors in series. For this input, and for the selected size of transistor T10, the voltage at Y1 is 3.97 V (Fig. 6). The results reported in Table III are derived from the timing diagrams of the outputs in Figure 6. In addition, the TSC circuit was simulated for various comibinations of faults from the fault sets. Some of the results are tabulated in Table I and Table II. Table I shows the simulation results for breaks and stuck-off transistors; the breaks were introduced at the source, drain or gate of the transistor. Table II shows the simulation results for stuck-on transistors. Magic layout tool is used to layout the original circuit and the modified TSC circuit. The circuits layouts are 2912 sq. units for the original circuit and 3432 sq. units for the modified TSC circuit; thus a percentage increase of 17.86%.

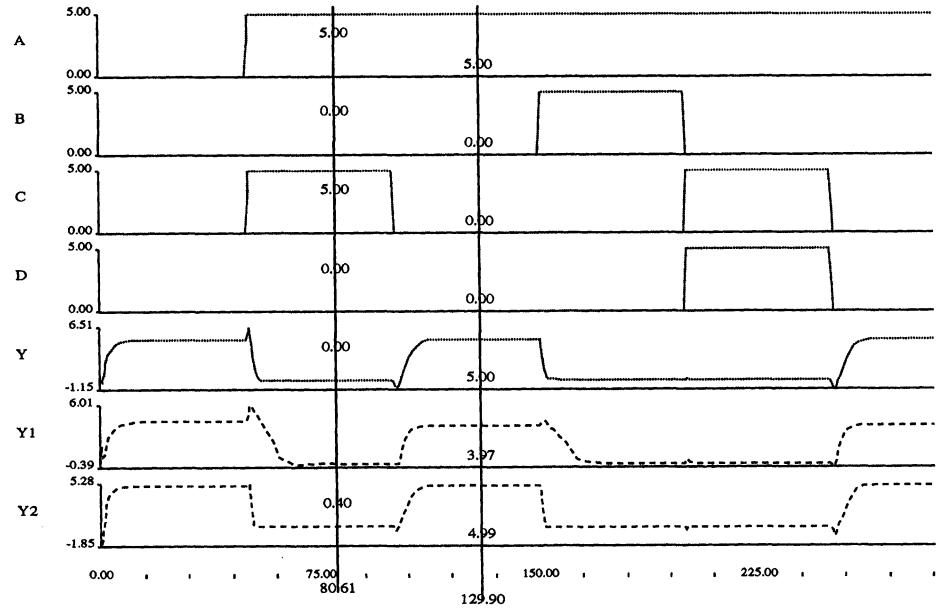

FIGURE 6 Input-output waveforms for circuits of Figure 5.

TABLE I Breaks or Stuck-off faults

Transistor(s)	Inputs				Fault-free		Faulty	
affected	a	b	c	d	Y1	Y2	Y1	Y2
T5	0	1	0	0	0	0	0	1
T4	1	0	0	0	1	1	0	1
T7	1	0	1	0	0	0	0	1
T9, T10	0	0	0	0	1	1	1	0
T2, T7, T8	1	0	1	1	0	0	0	1
T2, T3, T6, T7	0	0	1	1	1	1	0	1

TABLE II Stuck-on faults

Transistor(s)	Inputs				Fault-free		Faulty	
affected	a	b	c	d	Y1	Y2	Y1	Y2
T5	0	0	0	0	1	1	1	0
T4	1	0	0	1	0	0	1	0
T7	1	0	0	0	0	0	1	0
T9, T10	0	0	0	0	1	1	1	1
T2, T7, T8	0	0	1	1	1	1	1	0
T2, T3, T6, T7	1	0	1	0	0	0	1	0

The added voltage supply line (Vgg = 2.5 V) will be common to all the gates. This can be generated on-chip by using just two transistors in an inverter configuration, but with the output and input shorted. The results and the layout are indicative of two facts. First, the area overhead is not significant. Second, the modifications that have to be made to a CMOS layout are minor.

The modified TSC circuit has two outputs Y1 and Y2. The low voltage level at Y2 (=0.4V) and

TABLE III Timing results

Signal	Output High	Output Low	t_{phl}	t_{plh}	$td=(t_{phl}+t_{plh}/2)$
Y	5 volts	0 volts	1.86 ns	4.74 ns	3.3
Y1	3.97 volts	0 volts	8 ns	3.4 ns	5.7
Y2	5 volts	0.4 volts	0.98 ns	4.09 ns	2.54

t_{phl} is the propagation delay on the high to low transition.
t_{plh} is the propagation delay on the low to high transition.
td: average delay.

the high voltage level at Y1 (=3.97V) are acceptable low and high voltages for CMOS. The noise margins for the modified TSC circuit are lower than those for CMOS, but are comparable to those of nMOS circuits. The waveforms for Y, Y1, Y2 are shown in Figure 6. The input waveforms (A, B, C and D) have 0.8 ns fall times and rise times. Fall time is the time needed for an input to drop from 4V (90% of high voltage) to 1V (10% of the low voltage). The timing analysis shows that output Y1 is slower than output Y2. It also shows that Y2 is faster than Y, the output of the original circuit. Table III shows the timing results. The delay of Y1 could be further improved by choosing appropriate value for Vgg and by better transistor sizing. The waveform of Y2 has musch sharper edges and better voltage levels than Y1 or Y. This can be used as the output for driving any other circuit.

CMOS circuits usually have no static power consumption since there is no static path between Vdd and Gnd. On the other hand, the modified TSC FCMOS circuits have static paths between Vdd and GND when Y1 is pulled up or when Y2 is pulled down. Therefore, the power consumption for the TSC circuit is comparable to the power consumption in nMOS circuits. The power consumption for the modified, i.e., TSC, circuit was 0.13 mW compared to 0.02 mW for the original FCMOS circuit.

7. TSC MULTISTAGE FCMOS CIRCUITS

A general structure of a multistage TSC FCMOS circuit is shown in Figure 7. G1 and G2 are any complex gate whereas G3 is a two input gate (NAND or NOR). Note that inputs to the P and N networks of gates G1 and G2 have not been separated. The inputs of gate G3 have been split to individually feed into its P and N networks. This is because G1 and G2 are first stage gates whereas G3 is not. A TSC FCMOS gate produces a invalid code (10 or 01) at its outputs in the presence of a fault. The design procedure should ensure that this output propagates down to the final outputs of the composite circuit in order for the fault to be detected. For example, in Figure 7, a fault in G1 or G2 should affect the outputs of G3 also. This is ensured by connecting the output of the P-network (N-network) of one stage to the corresponding N-network (P-network) input of the following stage. When the input to any gate is an invalid code word, it may either turn on both the networks or turn them off, causing an invalid code to appear at its outputs as well. Thus, the invalid code word propagates from any stage to the final outpout, making the composite circuit self-testing. If the input to a stage

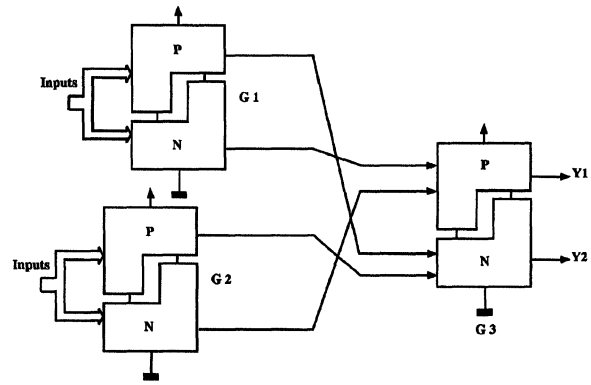

FIGURE 7 Multistage TSC FCMOS circuit structure.

is invalid (coming from a previous stage), then its output may still be correct if it has other inputs which are dominant. This means the circuit is also fault secure. Thus, the composite multistage FCMOS circuit is TSC. The proof verifying the validity of TSC Multistage circuits is given below.

THEOREM III *The proposed modification of a multistage FCMOS circuit will make it TSC for the fault sets mentioned in Section* 4.

Proof Let us consider the block diagram of a multistage FCMOS circuit as shown in Figure 8. The figure shows two successive stages, which may be part of a larger composite circuit. X1, X2 and Y1, Y2 are the outputs of stage S1 and S2 respectively. Stage S2 may have inputs besides X1 and X2 as shown in the figure. These inputs are assumed to be at values such that they sensitize the fault present in the circuit. The proof considers four possible cases:

I. S1 fault-free and S2 fault-free.
II. S1 fault-free and S2 faulty.
III. S1 faulty and S2 fault-free.
IV. S1 faulty and S2 fault.

Case I: S1 fault-free and S2 fault-free This case will be the similar to a normal circuit. For this case, X1 = X2 and Y1 = Y2 for all valid inputs. Theorem I and II can be applied to both S1 and S2 individually to prove this case.

Case II: S1 fault-free and S2 faulty This case is similar to a faulty single stage circuit. Theorem I and II can be applied to both S1 and S2 individually to prove this case.

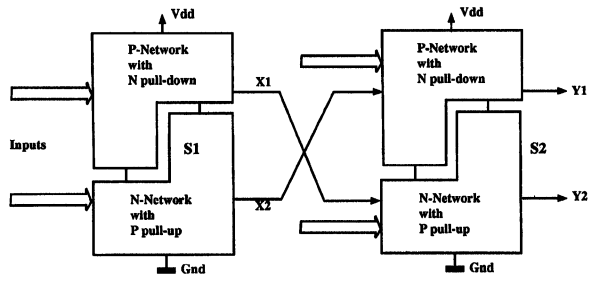

FIGURE 8 Two stages of a composite circuit.

Case III: S1 faulty and S2 fault-free There are two possible situations to be considered here. The outputs of S1 can be either 01 or 10.

Let us consider the case when outputs X1X2 are 01. Due to the crossover in the diagram, the P-network of S1 will get an input of 1 and the N-network will get an input of 0. This input will turn off a pair of transistors in S2. In a FCMOS circuit, every transistor in the P-network has a corresponding transistor in the N-network. At any time, in a fault-free FCMOS circuit, one of these two transistors will be on and the other will be off. The outputs of S1, thus, simulate the effect of a break or a stuck-off transistor in S2 by turning off two transistors in a pair. If the other inputs to S2 are such that they sensitize this 'fault', then both networks will be turned off, and the outputs Y1Y2 equal 01. Thus, the effect of a fault in S1 has propagated to the final output of the multistage circuit.

Next, let us consider the case where outputs X1X2 are 10. Due to the crossover in the diagram, the P-network of S1 will get an input of 0 and the N-network will get an input of 1. This input will turn on a pair of transistors in S2. The outputs of S1, thus, simulate the effect of a stuck-on transistor in S2 by turning on two transistors in a pair. If the other inputs to S2 are such that they sensitize this 'fault', then both networks will be turned on, and the outputs Y1Y2 equal 10. Thus, the effect of a fault in S1 has propagated to the final output of the multistage circuit. This proves the circuit to be TSC for Case III.

Case IV: S1 faulty and S2 faulty This case implies that the faults in S1 and S2 lie in fault set 2 or 3 (Section 4). We first consider fault set 2. Faults in this set, when sensitized cause the circuit to produce an output of 01. So X1X2 will be 01. This simulates a fault from set 2 in S2 as explained for Case III. Therefore, S2 can be considered to have multiple faults from the fault set 2. Case II of Theorem II proves this circuit to be TSC for the situation. If the faults lie in set 3, then the circuit will produce an output of 10 when sensitized. So X1X2 will be 10. This simulates a fault from set 3 in

S2 as explained for Case III. Therefore, S2 can be considered to have multiple faults from fault set 3. Case III of Theorem II proves this circuit to be TSC for this situation. Thus, the multistage circuit is TSC for the fault set mentioned in Section 4. QED.

8. CONCLUSION

The proposed technique enables the design of TSC FCMOS circuits for all relistic faults that may occur in VLSI circuits. The resulting overhead is very low. The technique is unable to detect multiple faults which include the weak transistors. This condition can be alleviated by adding more weak transistors in parallel to the existing ones. This redundancy does increase the overhead, but may be justifiable in certain cases. The technique introduces a delay in the circuit due to the addition of two weak transistors. This delay can be minimized by proper choice of the transistor sizes. The faults covered by this technique and the low overhead makes it practical for self checking VLSI circuit design.

Acknowledgment

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