Timing-Driven Circuit Implementation

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We consider the problem of selecting the proper implementation of each circuit module from a cell library to minimize the propagation delay along every path from any primary input to any primary output subject to an upper bound on the total area of the circuit. Different module implementations may have different areas and delays on the paths. We show that the latter problem is NP-hard even for directed acyclic graphs with two implementations per module and no restrictions on the overall area of the circuit. We present a novel retiming based heuristic for determining the minimum clock period on sequential circuits. Although our heuristics may handle a bound on the total area of the circuit, emphasis is given on the timing issue.

Keywords: Circuit implementation, technology mapping, delay minimization, NP-complete algorithms

1. INTRODUCTION

The circuit implementation problem studied here is related to the technology mapping problem studied earlier by Brayton et al. [1], Keutzer [7], Pedram et al. [13], Touati et al. [16, 17], Chaudhary et al. [3] and others. The authors above examine the problem of mapping a Boolean network using gates from a finite size cell library. However, in this paper, we consider Boolean networks that have already been mapped.

We examine the problem of selecting, from a cell library, an implementation for each module so that the propagation delay along any path from any primary input to any primary output is minimum. It is desirable that the total area of the circuit does not exceed a given bound. Every module implementation may have different delays along the paths connecting different pairs of input-output (I/O) terminals. Different implementations may also have different areas. In [2, 11], a similar problem was studied, the basic circuit implementation problem (BCI), where different implementations may have different areas, but the delays within each module are uniform.\textsuperscript{1}

The circuit implementation problem is very complex since many factors, i.e., delay, area, power, must be taken into consideration. How-

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\textsuperscript{1}Note that the authors in [11] insist that there is a path between every pair of input-output terminals. In this paper we relax the latter constraint which does not necessarily hold on mapped macro-based circuits where a module represents a macro in a specific technology.
ever, a recent trend in Computer Aided Design (CAD) focuses on timing driven applications, where priority is given to the maximum delay between any I/O path in a designed combinational circuit, or between any two flip-flops in a synchronous sequential circuit [15]. Thus, our primary goal is to select module implementations so that we minimize the maximum delay of a given circuit. For the sake of simplicity, we focus on the Timing-Driven General Circuit Implementation (TDGCI) model, where the module implementations are selected without considering the area of each implementation. However, the heuristic solutions presented in this paper can be easily extended to consider a bound on the total area of the implemented circuit.

We consider the pin-dependent MIS library delay model as was formulated in [3], where the arrival time $\text{arrival}(\cdot)$ at the output $g_o$ of some module $g$ is a complex function expressed as $\text{arrival}(g_o, C_{g_o}) = \max_{g_i \in \text{inputs}(g)}(r_{g_i, g_o} + R_{g_i, g_o}C_{g_o} + \text{arrival}(g_i, C_{g_i}))$, where $r_{g_i, g_o}$ is the intrinsic gate delay from input $g_i$ to output $g_o$ of $g$, $R_{g_i, g_o}$ is the drive resistance of $g$ corresponding to a signal transition at input $g_i$, $C_{g_o}$ is the load capacitance seen at $g_o$, and $\text{arrival}(g_i, C_{g_i})$ is the arrival time at input $g_i$ corresponding to load $C_{g_i}$ seen at that input [3]. The load capacitance $C_{g_o}$ depends on the input pin capacitances of the gates it is driving squared. Observe that if all pin capacitances of all module implementations are the same we result to a more simplified delay model, the simplified TDGCI problem where every module implementation has local delays on its various paths that do not depend on the delays on paths of other modules in the circuit. That way, the delay along a path can be computed by simply adding the delays on the module edges on the path.

Most of the previous work in the literature is on a simpler model, the BCI problem [2, 11, 10]. In this model the delay at each module output does not depend on module paths. For example, the rising transition of an $m$-input CMOS $NAND$ gate can be approximated as [18]: $t_r = \frac{R_p}{n} (m n C_d + C_f + k C_p)$, where $R_p$ is the effective resistance of $p$-device in a minimum-sized inverter, $n$ is the width multiplier for $p$-devices in this gate, $k$ is the fan-out, $m$ is the fan-in, $C_d$ is the gate capacitance of a minimum-sized inverter, $C_f$ is the source/drain capacitance of a minimum-sized inverter, and $C_p$ is the routing capacitance [18]. A similar approximation is given for the falling transition. Observe that due to the different capacitances, the delay of one module may depend on the delay of a neighboring module. However, the authors in [2, 11, 10] have considered a simplified BCI model so that the delay along a path can be computed by summing the delays on the modules on the path.

Chan [2] has shown that the simplified BCI problem is NP-hard for circuits with tree topology. Furthermore, for the simplified BCI model, Chan [2] has given a pseudo-polynomial time algorithm for trees, and a heuristic for basic circuits modeled by directed acyclic graphs (dags). Later, Li et al. [11] showed that the simplified BCI problem in NP-hard. They also developed a pseudo-polynomial time algorithm that obtains optimal solutions for basic series-parallel circuits [11]. In addition, they proposed six heuristics for basic combinational circuits under the simplified BCI model, without actually providing that the BCI problem on combinational circuits is NP-hard in the strong sense [11]. We have shown that the latter problem is indeed NP-hard by reducing from the One-In-Three 3SAT problem. The reduction is given in the Appendix. The latter was also recently, and independently, shown in [10] by reducing from the 3SAT problem. Both reductions hold for the restricted case of two implementations per module.

It appears that it is often the case in VLSI where parameters related to capacitances are ignored so that algorithmic solutions are obtained easier. This is for example the case in the clustering problem for delay minimization studied in [8, 12, 14], among others.

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2The latter recursive formula is slightly different from the one in [3] since we only consider Boolean Networks that have already been mapped.
In another context, the authors in [9] allow similar simplifications when they perform a retiming in a sequential circuit. Retiming is a technique that allows repositioning of the existing flip-flops of a sequential circuit so that its operation is not modified and the clock-period is minimized. This is equivalent to maintaining the same number of flip-flops at each cycle. Leiserson and Saxe have presented efficient retiming algorithms [9]. In fact, in this paper we modify one of the algorithms in [9] to solve the TDGCI problem efficiently for sequential circuits. Thus, the heuristics proposed in this paper are derived by initially considering the simplified TDGCI problem. At this point we decide the implementation for every module. Subsequently, we report the actual delay according to the pin-dependent MIS library delay model. That way we derive accurate solutions in a more efficient (in terms of time response) manner.

The paper is organized as follows. In Section 2, we solve an interesting open problem and we show that the TDGCI problem remains NP-hard on directed acyclic graphs (combinational circuits), where all the modules in the library have the same pin capacitances and there are only two possible implementations for each module. This is an improvement over the result in Li et al. [11].

In Section 3, we consider the TDGCI problem on general circuits and we given heuristics for both combinational and sequential circuits. In sequential circuits the goal is to minimize the clock period. We define the latter problem as that of selecting an implementation for each of the circuit modules, so that the clock-period of the circuit is minimized and the circuit function is preserved. As in [9], we assume delays on the combinational components only, and not on the flip-flops. In the first part of Section 3 we present a method for combinational circuits. This approach resembles the iterative improvement methodology, a popular approach for CAD, which needs to be modified so that it is more time efficient. We emphasize that iterative improvement turns out to be a very expensive (time consuming) operation, especially when one insists on working directly on the pin-dependent MIS library delay model, whereas our proposed method is much more efficient both in time response and surprisingly in quality of results when compared to iterative improvement. Then we present an $O(|V|^2|E|\log|V|)$ time approach that uses retiming techniques as well as the latter method to obtain efficient solutions for the circuit implementation problem on sequential circuits. Our proposed heuristics are then compared with two alternative approaches in Section 4.

Below we present some notation. A circuit is an interconnected set of modules. Each module has a number of input and output pins. A module with $p$ input pins and $q$ output pins is called a $(p, q)$-module. Some of the input pins of a $(p, q)$-module may be primary inputs and some output pins may be primary outputs.

## 2. THE COMPLEXITY OF THE TDGCI PROBLEM

We first show that the TDGCI decision problem is NP-complete on directed acyclic graphs with two implementations per module and uniform pin capacitances.

**TIMING-DRIVEN CIRCUIT IMPLEMENTATION PROBLEM (TDGCI)**

**Input:** A combinational logic circuit, two implementations for each module of the circuit, and a delay $D$.

**Output:** Is there an implementation, such that the delay of the given circuit is at most $D$?

We reduce from NP-complete problem in [5]:

**MAXIMUM 2-SATISFIABILITY (MAX-2SAT)**

**Input:** Set $U$ of variables, collection $C$ of clauses over $U$ such that each clause $c_k \in C$, $1 \leq k \leq |C|$ has $|c_k| = 2$, positive integer $K \leq |C|$.

**Question:** Is there a truth assignment for $U$ that simultaneously satisfies at least $K$ of the clauses in $C$?

**Theorem 2.1** The TDGCI decision problem is NP-complete in the strong sense even if the
maximum number of possible implementations for each module is two.

Proof The TDGGI decision problem is easily shown to be in NP. Next, we transform MAX-2SAT to TDGCI. Let \( U = \{u_1, u_2, \ldots, u_n\} \) be a set of variables and \( C = \{c_1, c_2, \ldots, c_m\} \) be a set of clauses making up an instance of MAX-2SAT. We shall construct an instance of TDGCI such that the MAX-2SAT instance is satisfiable if and only if the constructed TDGCI instance has an implementation with delay at most \( D \). We obtain the TDGCI instance as follows.

Let \( l_1^k, l_2^k \) be the first and the second literals of clause \( c_k, 1 \leq k \leq |C| \), respectively. Note that any literal \( l_1^k \) is either equal to some \( u_j \) or its complement \( u'_j \), where \( u_j \in U \). For every clause \( c_k, 1 \leq k \leq |C| \), we construct two modules called variable modules and a module called clause module. We call these three modules the \( k \)th block. The structure of the variables and clause modules is given below.

Each variable module is a (4, 4)-module and corresponds to a literal in the particular clause. For example, if \( l_1^k = u'_2 \) and \( l_2^k = u_3 \), we construct two variable modules which we label \( U_2^k \) and \( U_3^k \), respectively. The structure of module \( U_2^k \) and \( U_3^k \) is given in Figure 1a. The labeling of the module's inputs and outputs is also given in Figure 1a. The clause module \( C_k \) corresponding to clause \( c_k \) is a (2, 2)-module. Let the \( r \)th input and \( r \)th output of module \( C_k \) be labeled \( C_{r1}^k \) and \( C_{r2}^k \), respectively. The structure of module \( C_k \) is given in Figure 1b. Observe that it contains 2 internal nodes (this constraint can be removed but it simplifies the description of the reduction), and 5 internal edges, labeled \( e_i^k, 1 \leq i \leq 5 \), respectively.

The variable and clause modules are connected as follows: If \( l_1^k = u_i, u_i \in U \), then \( U_{i1}^k \) is connected to \( C_k \). If \( l_2^k = u'_i, u'_i \in U \), then \( U_{i2}^k \) is connected to \( C_k \). Similarly, if \( l_2^k = u_j, u_j \in U \), then \( U_{j1}^k \) is
We will now give two possible implementations for each variable and clause module, and an upper bound $D$ on the delay, so that we guarantee that at most $K$ clauses are satisfied if and only if the delay is at most $D$. This will be shown assuming a consistent assignment of true/false values on all appearance of each variable. This consistency will be guaranteed later via connections of the 3rd and 4th inputs and outputs of each variable module. Every variable module $U_k^j$ has two implementations: If $u_i$ is assigned the value true, then we assign delays 0, 1, 0, 1 along the edges connecting the $i$th input and output, $1 \leq i \leq 4$, respectively. If $u_i$ is assigned the value false, then we assign delays 1, 0, 1, 0 respectively. Similarly, each clause module $C_k$ has two implementations. The implementation of a clause module depends on the true/false evaluation of the first literal of the respective clause. If the first literal of a clause is true then we choose the implementation where $e_1^k = 1$, and $e_2^k = e_3^k = e_4^k = 0$. Otherwise, we choose the second implementation where $e_2^k = 1$, and $e_1^k = e_3^k = e_4^k = 0$. Finally, we set the delay $D$ to be $2m-K$. An example of the TDGCI instance corresponding to a MAX-2SAT instance is shown in Figure 1c.

We now show that the MAX-2SAT instance is satisfiable if and only if the constructed TDGCI instance has an implementation with delay $D'$ at most $D$. Let $c_k$ be a clause and consider the path from any of the first two inputs of the corresponding variable modules to any of the two outputs of the clause module $c_k$. If either one literal or both literals of $c_k$ are evaluated to be true, then both outputs of $c_k$ will have delay 1. If both literals are evaluated to be false, then both outputs will have delay 2. From the way we constructed the TDGCI instance, the delay up to the $i$th block is added to the delay up to the $i+1$th block. Thus, we ensure that every satisfied clause $c_k$ increments the delay up to the $k$th block. On the other hand, if $c_k$ is an nonsatisfied clause, the delay up to the $k$th block is increased by 2 units.
If the MAX-2SAT instance is satisfied, there at least \( K \) clauses satisfied and \( m-K \) clauses that are not satisfied. If there are exactly \( K \) clauses satisfied, then \( D'=2(m-K)+K=2m-K \). It is easy to see that in the constructed TDGCI instance of Figure 1c, \( D' \leq 2m-K \).

Conversely, suppose that the constructed TDGCI instance is satisfied. This implies that the delay along the longest path is at most \( 2m-K \), or equivalently, there are at least \( K \) blocks with delay 1. The latter implies that there are at least \( K \) clauses that are satisfied in the MAX-2SAT instance.

Up to now, we have assumed that we can ensure a consistent true/false assignment on all appearances of each variable. This can not be ensured necessarily with the up to now construction. However, we will enforce the latter by enlarging our construction as follows: For every variable \( u_i \) of the MAX-2SAT instance, we construct a (2, 2)-module which we call control module and we label it as \( C_{U_i} \). Let the \( r \)th input and \( r \)th output of Module \( C_{U_i} \) be labeled \( C_{U_i}^r \) and \( C_{U_i}^r \), respectively. The structure of such a module is given in Figure 1d. Note, that a variable \( u_i \) may appear in more than one clauses, and for each of its appearances we have created a new variable module. We connect these variable modules with their corresponding control modules as follows: We connect the 3rd and 4th outputs of the variable module corresponding to the \( k \)th appearance of variable \( u_i \), \( 1 \leq k \), with the 3rd and 4th inputs, respectively, of the variable module corresponding to the next \( (k+1) \)th appearance of variable \( u_i \). We continue in this manner and last we connect the 3rd and 4th outputs of the variable module corresponding to the last appearance of variable \( u_i \) with the 1st and 2nd inputs, respectively, of the control module \( C_{U_i} \). Let \( m_i \) be the number of clauses that contain either \( u_i \) or \( u_i' \). Every control module \( C_{U_i} \) has two implementations: If \( u_i \) is assigned the value true, then we choose the 2nd implementation where the latter edges have delays \( 2m-K-m_i \), \( 2m-K \), respectively. If \( u_i \) is assigned the value false, then we choose the 2nd implementation where the latter edges have delays \( 2m-K-m_i \), \( 2m-K \), respectively. Figure 1e shows the complete construction of the reduction of Figure 1c, and illustrates the latter construction.

We now show that the control modules guarantee a consistent true/false assignment to the variables. If the delay in the TDGCI instance is at most \( 2m-K \), then the delays up to \( C_{U_i}^1 \), \( C_{U_i}^1 \) of every control module \( C_{U_i} \) must be at most \( 2m-K \). However, our construction enforces that exactly one of the two internal edges of \( C_{U_i} \) is assigned delay of exactly \( 2m-K \) units. If the first internal edge of \( C_{U_i} \) is assigned delay \( 2m-K \), then the delay up to input \( C_{U_i}^1 \) is 0. This in turn implies that the delays on all edges connecting the 3rd input and output of every variable module corresponding to variable \( u_i \) must be 0. The latter enforces a consistent true assignment to all appearances of variable \( u_i \). Similarly, if the second internal edge of module \( C_{U_i} \) is assigned delay \( 2m-K \), then it means that we ensure a consistent false assignment to all appearances of variable \( u_i \).

3. HEURISTICS FOR THE TDGCI PROBLEM

3.1. Combinational Circuits

We propose a heuristic for solving the TDGCI problem on combinational circuits modeled by dags. For simplicity, we assume two implementations per module. We borrow ideas from the iterative improvement methodology. We first define the gain \( g(u) \) of a node \( u \) to be the difference between the delay of the longest path considering the node's current and complimentary implementation, respectively. Let the two delays be denoted \( D_1 \) and \( D_2 \). The gain of node \( u \) is \( g(u) = D_1 - D_2 \) i.e., the benefit resulting from the interchange on the module's implementation. In order to speed up operations however, we employ a technique that
calculates the gain of the modules approximately (based on local principles), in most cases provably correct. However, in order to be able to perform these local computations we must assume that all modules in the library have identical pin capacitances and therefore the load capacitance seen at each module output is the same. Note that this is where our approach is different from the straightforward iterative improvement. The major operation of our heuristic is to select the module with the biggest calculated gain, change its implementation has been found, and (b) it will not be changed in later iterations of the program. Finally, after all circuit modules have been assigned an implementation we perform an extra step (topological search) to enhance the quality of our results. We consider the modules actual pin capacitances and via a longest path computation we calculate precisely the (minimized) maximum delay of the circuit.

In a preprocessing step, we transform the input combinational circuit to an acyclic directed graph, $G=(V, E)$, by substituting every $(p, q)$-module by $(p+q)$ vertices. Figure 2 illustrates the transformation. Note that in the transformed graph, delays exist only on the edges that resemble edges internal to the modules in the original circuit.

Next we describe the procedure that calculates the gains. Each vertex $u$ contains two fields $lp-in(u)$ and $lp-in2(u)$. The former stores the maximum delay on the longest path from $S$ to $u$, and the latter the maximum delay on the longest path from $D$ to vertex $u$. We calculate the value of both fields via two longest path computations, one from $S$ to $D$, and one from $D$ to $S$.

Let $M_1$ be some $(p, q)$-module, selected for evaluation. The heuristic adds $lp-in1(p_i)$ to the $lp-in2(q_j)$, for every pair $(p_i, q_j)$ of $M_1$. It then adds the result to the weight of the internal edge from $p_i$ to $q_j$. Observe that this is the maximum delay on the longest path from $S$ to $D$ passing through vertices $p_i$ and $q_j$. Let's call this maximum delay $l_{1\max}$. Next, it compares the value of $l_{1\max}$ with the value of the maximum delay on the global longest path from $S$ to $D$, call it $l_{\max}$. If $l_{1\max} - l_{2\max} = 0$, then vertices $p_i, q_j$ are on the global longest path from $S$ to $D$. If $l_{1\max} - l_{2\max} > 0$, then vertices $p_i, q_j$ are not on the global longest path from $S$ to $D$. Either way, a flag is set to determine the status of each vertex. Let $l_{2\max} = lp-in1(p_i) + lp-in2(q_j) + d_2$, where $d_2$ is the delay of the second implementation of $M_1$ from $p_i$ to $q_j$.

The heuristic completes $g(M_1)$ as follows: If $l_{2\max} > l_{\max}$, then $g(M_1) = l_{\max} - l_{2\max}$. If $l_{2\max} < l_{\max}$ and vertices $p_i, q_j$ are not on global longest path, then $g(M_1) = 0$. If $l_{2\max} = l_{\max}$, then $g(M_1) = 0$. If $l_{2\max} < l_{\max}$ and vertices $p_i, q_j$ are on

\[3\] This process is in fact repeated a fixed number of times of unlocking all cells, in hope of further reducing the overall delay.
the global longest path, then $g(M_1) = l_{\text{max}} - l_{\text{max}}^2$. For every pair $(p_i, q_j) \in M_1$ there is a corresponding gain for $M_1$. The smallest of these gains is the one that our heuristic considers as $g(M_1)$. Let $|V|$ be the number of modules of the given circuit, and $|E|$ to the number of all edges of the graph. The heuristic requires $O(|V||E|)$ time. This is much less than the straightforward iterative improvement scenario (even for the simplified TDGCI model) where every time a module changes implementation we have to compute the gain exactly.

### 3.2. Sequential Circuits

A straightforward heuristic that obtains optimal solution to the TDGCI problem on sequential circuits is based on the idea of generating a combinational circuit by selecting flip-flops to break the cycles, and then apply the algorithm above. Figure 3 illustrates the process. Our proposed approach uses the concept of retiming.

Leiserson and Saxe [9] proposed algorithms for clock period minimization, for both circuits with uniform and nonuniform delays on the modules. We found the proposed algorithm for circuits with
nonuniform delays on the modules [9] to be complicated to implement. In this paper, we present an approach for the general model, which although asymptotically has the same time complexity with the respective algorithm in [9], is faster in practice and much easier to implement.

The formulation of our problem requires a retiming technique with some constraints on top of the ones in [9]. More precisely we perform retiming on a graph constructed as follows: Every module's input and output is represented by a node, and every internal edge is substituted by a node and two edges labeled as prohibitive. An edge is called prohibitive if it is not allowed to host any flip-flop. After this transformation, all nodes have uniform delays. (see also Fig. 4). Our problem is to do retiming on a cyclic graph $G=(V, E)$, constructed from the sequential circuit so that we minimize the clock period subject to a set of prohibitive edges $E_p$. It can be shown that the problem is equivalent to assigning weights $r(u)$ on the nodes $u \in V$, that satisfy the following conditions:

C1: $r(u) - r(v) \leq w(e)$, $\forall e = (u, v) \in E$.
C2: $r(u) - r(v) \leq W(u, v) - 1$, $\forall u, v \in V$ such that $D(u, v) > c$.
C3: $r(u) - r(v) = w(e)$, $\forall e = (u, v) \in E_p$, where $E_p$ is the set of prohibitive edges.

![Figure 4](image)

**FIGURE 4** The transformation using the prohibitive edge model. (a) A functional element with nonuniform delays. (b) The element of (a) after the transformation. The labels inside the circles indicate uniform delays on the respective nodes.
each unchanged module. The time complexity is
\( O(|V|^3|E| \log |V|) \).

4. EXPERIMENTAL RESULTS

We implemented both our approach and the straightforward iterative improvement for the combinational circuits in C and run on a Sun Sparc System 4/330. We experimented on several ISCAS'85 benchmarks. Since the ISCAS'85 circuits do not include a list of possible implementations for each module, we generated these randomly by using function rand() from the standard library. For simplicity reasons, we considered uniform pin capacitances and the simplified model. We applied mod 10 to all created numbers, so that the delays range from 0 to 9. We treat every cell from the library as a module. Table I, gives the experimental results for our heuristic, Comb1, and the straightforward iterative improvement approach Comb2. In Table I, “initial delay” denotes the initial delay of the circuit's longest path, “delay” the minimum delay obtained for the longest path, and “time” the time required for the particular heuristic to terminate. The time here is expressed in seconds.

When we constructed Comb1, we tried to stay as close to the gain computation as possible, expecting to get a little worse results than those of Comb2 (since the gains were computed approximately) but faster. We observed that in 80% of the gain selection Comb1 did indeed select the best actual gain. From Table I, observe that Comb1 is not only much faster than Comb2 as expected, but is also produces smaller delays. A possible explanation of this behavior is that the suboptimal gains helped escaping local minima.

We implemented our heuristics for the sequential circuits in C and run on a Sun Sparc System 2. We experimented on several ISCAS'89 benchmarks. For simplicity reasons, we run our three heuristics based on the assumption that all modules have uniform delays. We used the delays given by the ISCAS'89 circuit data as the delays of the first implementation. We generated the delays of the modules for the second implementation randomly using the function rand() from the standard library. In addition, we applied mod 10 to all generated numbers so the delays range from 0 to 9. As before, we treat each cell from the library as a module. Table II, presents the experimental results for the straightforward approach, Seq 1, our heuristic, Seq 2, and Seq 3. Under “initial delay”, we give the initial delay of the circuit's longest path. Under “delay”, we list the minimum delay obtained for the longest path. Under “time”, we give the time required for the particular heuristic to terminate. The time is expressed in seconds. Moreover, under “initial min.clock” we give the initial minimum clock period obtained by using retiming in Seq 2, Seq 3, before any module swaps have taken place. Although retiming appears to be relatively slow

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</tr>
</tbody>
</table>
TABLE II Results for Seq 1, Seq 2 and Seq 3

<table>
<thead>
<tr>
<th>Circuit ISCAS</th>
<th># of nodes</th>
<th>initial delay</th>
<th>Seq 1</th>
<th>Seq 2</th>
<th>Seq 3</th>
<th>initial min. clock</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>delay</td>
<td>time</td>
<td>delay</td>
<td>time</td>
</tr>
<tr>
<td>s208.1</td>
<td>122</td>
<td>114</td>
<td>52</td>
<td>0.62</td>
<td>22</td>
<td>78.2</td>
</tr>
<tr>
<td>s298</td>
<td>137</td>
<td>102</td>
<td>40</td>
<td>0.9</td>
<td>33</td>
<td>96.1</td>
</tr>
<tr>
<td>s349</td>
<td>185</td>
<td>220</td>
<td>87</td>
<td>1.4</td>
<td>67</td>
<td>156.3</td>
</tr>
<tr>
<td>s382</td>
<td>182</td>
<td>114</td>
<td>57</td>
<td>2.3</td>
<td>39</td>
<td>144</td>
</tr>
<tr>
<td>s386</td>
<td>172</td>
<td>110</td>
<td>66</td>
<td>1.6</td>
<td>48</td>
<td>112.1</td>
</tr>
<tr>
<td>s444</td>
<td>204</td>
<td>134</td>
<td>64</td>
<td>5.6</td>
<td>47</td>
<td>467</td>
</tr>
<tr>
<td>s510</td>
<td>236</td>
<td>136</td>
<td>52</td>
<td>9.4</td>
<td>51</td>
<td>612</td>
</tr>
<tr>
<td>s838.1</td>
<td>512</td>
<td>174</td>
<td>142</td>
<td>45</td>
<td>134</td>
<td>3867</td>
</tr>
</tbody>
</table>

process, we were able to obtain good results by using the prohibitive edge scheme described in Section 4. The results were in practice faster than the approach in [9] for the general model (with the simplifications described in the prohibitive edge model), by a factor of approximately 10%. Seq 3 was inapplicable even for small circuits. More importantly, the latter modification did not lead to any improvements on the quality of the obtained implementations.

For simplicity reasons we implemented all of our heuristics without considering any area constraints. Note though that all of our heuristics can be trivially modified in order to handle a given upper bound on the total area of the circuit. The idea is to select the module that has the highest gain but whose selection does not violate the area upper bound. When the module with the biggest gain has been obtained, the particular heuristic checks whether by considering this module the overall area of the circuit exceeds the given area bound. If the area bound is exceeded, then we discard the module and we proceed to the module that has the highest gain among the remaining ones. Otherwise, the module is selected.

5. CONCLUSION

We have shown that the general circuit implementation problem is NP-hard in the strong sense even when each module has only two implementations and there is no constraint on the total area of the circuit. We call this problem the TDGCI problem. The BCI problem, where all paths in a module have the same delays but different implementations have different areas is also NP-hard in the strong sense even for two implementations per module.

We proposed the first heuristic for combinational circuits under the general circuit implementation model. The heuristic uses iterative improvement methodology and outperforms an alternative iterative improvement scenario. We also proposed a retiming based heuristic for sequential circuits which uses the one for combinational circuits as a subroutine. The approach is compared to two other schemes we devised.

Acknowledgement

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References

APPENDIX

We show that the BCI problem is NP-complete in the strong sense. A somewhat stronger but more complex reduction was also given in [10] for the same problem. We reduce from a restricted version of the ONE-IN-THREE 3SAT problem [5] which we call the RESTRICTED ONE-IN-THREE 3SAT, and is also NP-complete [5]:

RESTRICTED ONE-IN-THREE 3SAT

Input: Set $U$ of variables, collection $C$ of clauses over $U$ such that each clause $c_k \in C$, $1 \leq k \leq |C|$, has $|c_k| = 3$, and does not contain any negated literal.

Question: Is there a truth assignment for $U$ such that each clause in $C$ has exactly one true literal?

Theorem 1 The BCI decision problem is NP-complete even if the maximum number of possible implementation for each module is two.

Proof Clearly, the BCI decision problem is in NP. Next, we transform RESTRICTED ONE-IN-THREE 3SAT to the BCI decision problem. Let $U = \{u_1, u_2, \ldots, u_n\}$ be a set of variables and $C = \{c_1, c_2, \ldots, c_m\}$ be a set of clauses making up an instance of RESTRICTED ONE-IN-THREE 3SAT. We shall construct an instance of BCI such that the RESTRICTED ONE-IN-THREE 3SAT instance is satisfiable if and only if the constructed BCI instance has an implementation with area at most $A$, and delay at most $D$. We obtain the BCI instance as follows.

Let $l_i^k$ be the $i^{th}$ literal of clause $c_k$. In the RESTRICTED ONE-IN-THREE 3SAT problem no $c_k \in C$ contains a negated literal. Thus, each literal $l_i^k$ is equal to some $u_j$, where $u_j \in U$. For every variable, $u_j$ of the RESTRICTED ONE-IN-THREE 3SAT instance, we construct a module, called variable module, and labeled $U_j$. Each variable module is an $(m, m)$-module, where $m$ is the number of clauses in RESTRICTED ONE-IN-THREE 3SAT instance. Let the first input and first output of module $U_j$ be labeled $U_j U_j$, respectively. The structure of a variable module, as well as the labeling of its inputs and outputs is given in Figure 5a.

The variable modules are connected as follows: Let $l_i^1$, $l_i^2$, $l_i^3$ be the first, the second, and the third literals of clause $c_k$, respectively. Assume that $l_i^1 = u_j$, $l_i^2 = u_j$, and $l_i^3 = u_j$, where $u_j, u_j, u_j \in U$. We connect $U_i^k$ with $U_j$ and $U_j$ with $U_j$.

We now describe the two possible implementations for each variable module, as well as an upper bound $A$ on the area and an upper bound $D$ on the delay. The latter bounds, together with our construction, guarantee that each clause $c_k \in C$ has exactly one true literal if and only if the area is at most $A$, and the delay is at most $D$. More precisely, let $m_i$ be the number of clauses that...
contain variable $u_i$. Clearly $\Sigma_i m_i = 3m$. Every variable module $U_i$ has two implementations. In the first implementation, the area is 0 and the delay is 1. In the second implementation, the area is $m_i$ and the delay is 0. (See also Fig. 5b). If $u_i$ is assigned the value true, then we assign module $U_i$ its first implementation. If $u_i$ is assigned the value false, then we assign its second implementation. Note that the way we construct the variable modules guarantees a consistent true/false assignment on the variables. In addition, we set the area $A$ to be $2m$, and the delay $D$ to be 1. An example of the BCI instance corresponding to a RESTRICTED ONE-IN-THREE 3SAT instance is shown in Figure 5b.

We now show that the RESTRICTED ONE-IN-THREE 3SAT instance is satisfiable if and only if the constructed BCI instance has an implementation with area at most $A$, and delay at most $D$. We call clause path $C_k$, the path along the variable modules for the variables corresponding to the clause $c_k$ (see Fig. 5b). Observe that the clause paths are the longest paths among any input-output paths. In fact, all the remaining input-output paths consist of one edge, and can have delay at most 1. If the RESTRICTED ONE-IN-THREE 3SAT instance is satisfied, then each clause $c_k \in C$ has one true and two false literals. Therefore, the delay on every clause path is the same and equal to 1, and the area of the whole BCI instance is $2m$. Thus, the BCI instance is satisfied.

On the other hand, suppose that the constructed BCI instance is satisfied. Then the delay along any input-output path is at most 1, and the area of the BCI instance is at most $2m$. Next, we show that the delay along any clause path is exactly 1, and the area of the BCI instance is exactly $2m$.

Assume, by contradiction, that one of the clause paths has delay 0. This means that all three variables of the corresponding clause are assigned the value false, and therefore, the corresponding variable modules are assigned their second implementation. Let these three variables be $u_i$, $u_j$, and $u_k$. From the construction, it follows that modules $U_i$, $U_j$, and $U_k$ contribute to the overall area of the BCI instance $m_i$, $m_j$, and $m_k$ units of area, respectively. Moreover in order to satisfy the upper bound on the delay constraint, every other clause must have at least two variables assigned the value false. Thus, besides the clause whose three variables are evaluated to be false, all the other clauses must have at most one variable evaluated to be true. Thus, in the RESTRICTED ONE-IN-THREE 3SAT instance there are less than $m$ variables which are evaluated to be true. The latter implies that the overall area exceeds the bound of $2m$, a contradiction.

Therefore no clause path can have delay 0, and all clause paths have delay exactly 1. The latter implies that exactly one variable per clause is true. Since our construction guarantees consistent true/false assignment to the variables, we conclude that
the RESTRICTED ONE-IN-THREE 3SAT instance is satisfied.

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Dimitrios G. Karayiannis was born in Greece, on March 12, 1969. He received the B.S. degree in Computer Science from Southern Illinois University in 1991 and the M.S. degree in Computer Science from Southern Illinois University in 1993. Currently, he received his Ph.D. degree in Computer Science, Southern Illinois University in 1996.

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