

Two-dimensional Carrier Transport in Si MOSFETs

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The importance of 2-dimensional (2D) features of carriers in Si MOSFETs on the device performance is re-examined experimentally and theoretically from the viewpoint of low-field mobility, velocity in high tangential fields and the inversion-layer capacitance. It is confirmed that low-field mobility and inversion-layer capacitance can be understood well in terms of the 2D subbands and the 2D carrier transport. In order to obtain fully-quantitative understanding of low-field mobility, however, it is still necessary to more accurately determine the amount of the scattering parameters in the inversion layer. On the other hand, saturation velocity is considered to be less influenced by the 2D quantization, while it is found experimentally that saturation velocity is slightly dependent on surface carrier concentration.

According to the knowledge of 2-dimensional carrier transport in Si inversion layer, an effective way to have higher current drive is to increase the occupancy of the 2-fold valleys, which have lower conductivity mass, on a (100) surface. From this viewpoint, two device structures, strained Si MOSFETs and SOI MOSFETs with ultra-thin SOI films, are introduced and the behavior of low-field mobility is analyzed through the calculations of the subband structures and phonon-limited mobility.

Keywords: MOSFET, Si, carrier transport, mobility, carrier velocity, inversion layer, 2-dimensional carrier gas, subband structure, strain, SOI

1. INTRODUCTION

It is well recognized that 2-dimensional (2D) features of carriers significantly affect the carrier transport in the inversion layer of Si, which determines the drain current of MOSFETs. The influence of the 2D quantization on the I-V characteristics of MOSFETs appears typically in the following ways. (1) Mobility is modulated through the change of the scattering probability due to the differences in the density-of-states, the

form factor of the envelope function of 2D carriers and the scattering parameters. (2) Gate capacitance is decreased by the inversion-layer capacitance, which is determined by the finite thickness of the envelope function. (3) The threshold voltage of MOSFETs is increased by the existence of the subband energy. The influences of (1) and (3) are pronounced more with an increase in the substrate impurity concentration of MOSFETs and the influence of (2) is pronounced more with an decrease in the gate oxide thickness. Thus, the accurate

consideration of the 2D quantization is quite important to quantitatively understand the electrical properties of scaled MOSFETs.

Many theoretical and experimental works [1] have so far been done on the characterization of the 2D carrier transport and, as a result, the understanding of the 2D quantization effects on the MOSFETs performance has been basically obtained, particularly at low temperatures. It seems, however, that the direct experimental evidence to verify the contribution of the 2D quantization at room temperature is still lacking and the quantitative description has not been fully obtained yet. In this paper we re-examine the influence of the 2D quantization on the basic physical quantities to determine I-V characteristics of MOSFETs, the mobility and the saturation velocity, v_{sat} , in the inversion layer, and the inversion-layer capacitance, C_{inv} , through the systematic experiments. In addition, the analysis based on the self-consistent subband calculations is performed to explain the experimental results. The present understanding and the questions still unsolved are presented with comparing the self-consistent subband calculations.

Moreover, based on the knowledge of the 2D carrier transport in the inversion layer of Si, a subband engineering scenario to obtain the higher performance of Si MOSFETs is introduced.

2. SUBBAND STRUCTURE OF Si MOS INTERFACE

Figure 1 shows the schematic diagram of the subband structure for inversion-layer electrons on a (100) surface, on which MOSFETs are commonly fabricated. Electrons confined near Si/SiO₂ interface by normal electric field are quantized in the direction perpendicular to the interface and grouped into electronic subbands as 2D Electron Gas (2DEG). A characteristic point of the subband structure on (100) is that electrons in the inversion layer are classified into two electronic systems, the 2-fold degenerate valleys and the 4-fold degenerate valleys, as shown in Figure 1.

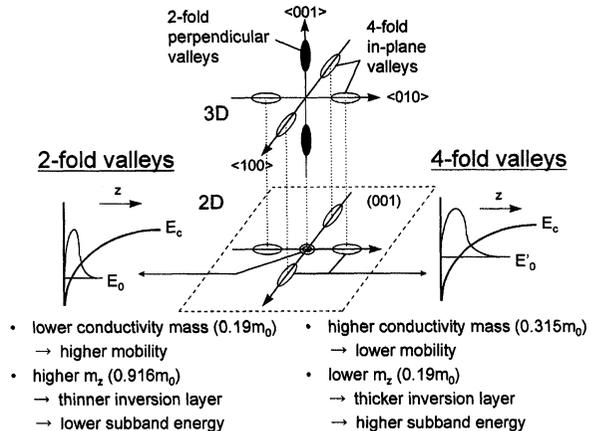


FIGURE 1 Schematic diagram of the subband structures for electrons on a (100) surface and the characteristics of the 2-fold and the 4-fold valleys.

Electrons in the 2-fold valleys have higher mobility due to smaller conductivity mass and thinner inversion-layer thickness due to higher effective mass perpendicular to the Si/SiO₂ interface than those in the 4-fold valleys. As a result, the electrical properties of inversion-layer electrons on (100) need to be understood as the weighed combination over these two electronic systems.

3. IMPACT OF 2D CARRIER GAS ON CARRIER TRANSPORT PROPERTIES IN MOSFETs

3.1. Low Field Mobility

Low field mobility in Si MOSFETs has so far been studied most extensively as the 2-dimensional carrier transport from both the theoretical and the experimental viewpoints. Recently, the inversion-layer mobility has come to be explained in terms of the scattering theory for the 2D carrier gas [2–6], even at room temperature. Figure 2 shows the experimental relationship between electron mobility on (100) and the normal effective field, E_{eff} , as a parameter of the substrate impurity concentration, N_A . E_{eff} is defined by $q(N_{\text{dpl}} + \eta N_s) / \epsilon_{\text{Si}}$, where N_{dpl} is the surface concentration of the space charge in the depletion region, N_s is the surface carrier concentration and ϵ_{Si} is the

permittivity of Si. One evidence of the 2D quantization effects on the inversion-layer mobility appears as its E_{eff} dependence, which is the origin of the “universal curve”. The universality of the inversion-layer mobility for E_{eff} , typically seen in Figure 2, has been verified experimentally over a wide range of the substrate impurity concentration for n - and p -MOSFETs [7–11] fabricated on several surface orientations [12]. The E_{eff} dependence in low and moderate E_{eff} region, which is roughly proportional to $E_{\text{eff}}^{-0.3}$, is thought to be attributable to phonon scattering for 2DEG, while the stronger E_{eff} dependence in higher E_{eff} region is influenced by surface roughness scattering. The mobility limited by intravalley acoustic phonon scattering for 2DEG is represented under the approximation of the single subband occupation [12, 13] by

$$\begin{aligned} \mu_{\text{ac}} &= \frac{q}{m_c} \cdot \frac{\hbar^3 \rho s_1^2}{m_d n_v D_{\text{ac}} k_B T} \cdot W \\ &\approx \frac{q}{m_c} \cdot \frac{\hbar^3 \rho s_1^2}{m_d n_v D_{\text{ac}} k_B T} \cdot \left(\frac{256 \epsilon_{\text{Si}} \hbar^2}{81 m_3 q^2} \right)^{1/3} \\ &\quad \cdot \left(N_{\text{dpl}} + \frac{11}{32} N_s \right)^{-1/3} \propto E_{\text{eff}}^{-1/3} \end{aligned} \quad (1)$$

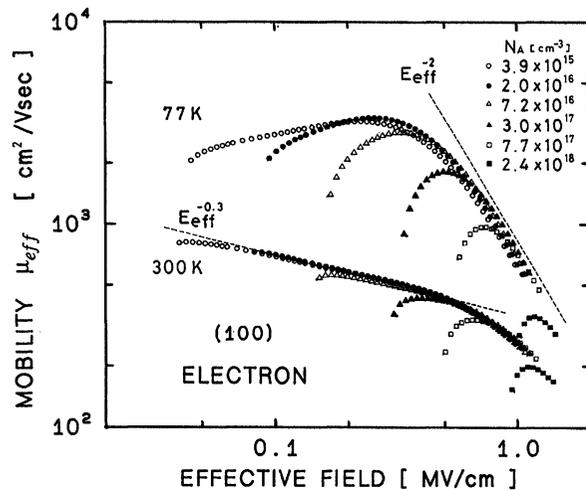


FIGURE 2 Relationship between inversion-layer electron mobility on (100) and the effective normal field, E_{eff} , as a parameter of the substrate impurity concentration. E_{eff} is defined by $q(N_{\text{dpl}} + N_s/2)/\epsilon_{\text{Si}}$ ($\eta=1/2$), where N_{dpl} is the surface concentration of the space charges and N_s is the surface carrier concentration.

m_c is conductivity mass, m_d is density-of-states mass, n_v is the valley degeneracy, D_{ac} is the deformation potential of acoustic phonon, s_1 is sound velocity. This E_{eff} dependence originates in the fact that the mobility is in proportion to the inversion-layer thickness, which is proportional to $E_{\text{eff}}^{-1/3}$ under η of 11/32. Since the inverse of the inversion-layer thickness determines the energy band width of acoustic phonon that can couple with 2DEG, the thinner inversion layer leads to the higher scattering rate with acoustic phonon.

In order to more quantitatively describe mobility at room temperature, however, it is necessary to take the contributions of all the subbands and the interactions with intra- and intervalley phonons into consideration. At present, the amount of the phonon-limited mobility and its E_{eff} dependence seems not to have been perfectly represented by the theoretical calculations [3, 4, 6]. Figures 3 and 4 show the E_{eff} dependence and the temperature dependence of the experimental and the calculated phonon-limited electron mobility, respectively. The

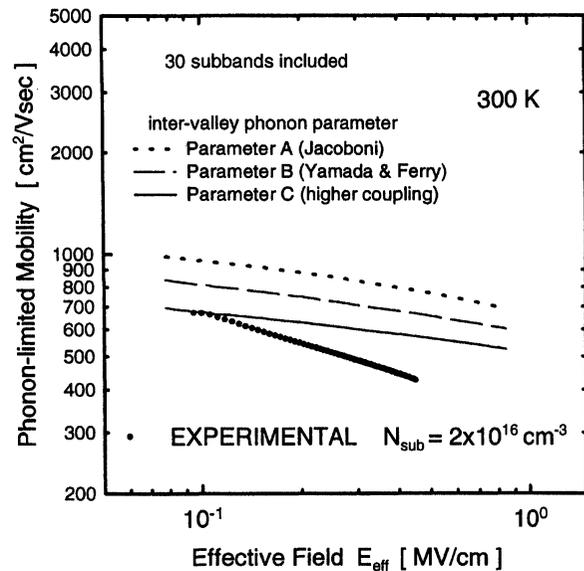


FIGURE 3 Calculated phonon-limited mobility in the inversion layer at room temperature as a function of E_{eff} . Three parameters sets of intervalley scattering, set A , B and C , which are listed in Table I, are compared with the experimental results, which are shown as closed circles.

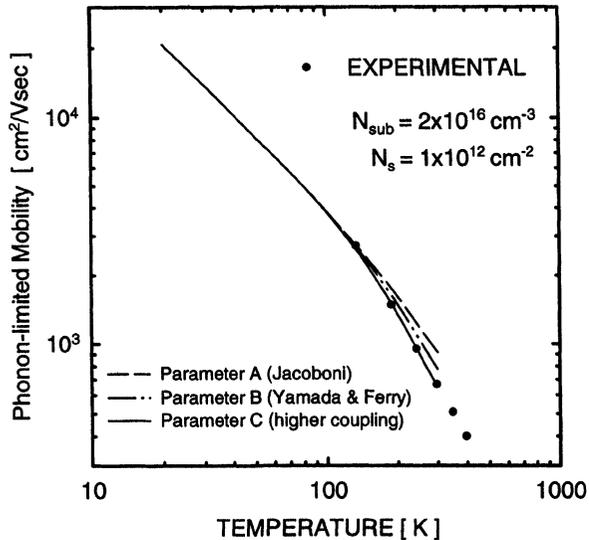


FIGURE 4 Calculated phonon-limited mobility in the inversion layer at N_s of $1 \times 10^{12} \text{ cm}^{-2}$ as a function of temperature. Three parameters sets of intervalley scattering, set *A*, *B* and *C*, which are listed in Table I, are compared with the experimental results, which are shown as closed circles.

mobility calculation was carried out under the relaxation time approximation, based on the results of the self-consistent subband calculations [14] including 20 subbands. Three different parameter sets of intervalley phonon scattering, which are listed in Table I, are used in the calculations. It is found that the amount of the mobility calculated under the bulk phonon scattering parameters (parameter set *A* [15] and *B* [16]) is higher than that of the experimental one and the calculated tem-

perature dependence is weaker than the experimental one.

One possible origin of this discrepancy might be the difference in the scattering parameters in the inversion layer from those in bulk, which might be partly due to the difference of phonons relevant to intervalley scattering between 3DEG and 2DEG, coming from the selection rule in the wave-vector conservation. As one example of the different scattering parameters, a parameter set including larger deformation potential of intervalley f-phonon scattering (parameter set *C*) was used for the mobility calculation. The results are also shown in Figures 3 and 4. It is found that the higher coupling with intervalley phonons than in bulk can provide better agreement with the experimental results for both the magnitude of mobility and its temperature dependence. Furthermore, as described later, the analysis of the mobility enhancement in strained Si MOSFETs also suggests the higher coupling between 2DEG and intervalley phonons. The mobility enhancement factor, the ratio of the mobility in strained Si MOSFETs to that in conventional Si MOSFETs, is also explained well by assuming the higher coupling with intervalley phonons (see Fig. 8). In order to more quantitatively obtain the values of the scattering parameters in the inversion layer, other experimental evidences through the direct evaluation of the scattering parameters are required. On the other hand, even if the parameter set *C* is used, the calculated E_{eff} dependence is still

TABLE I Parameters for intervalley phonon scattering models. E_k and D_k are the values of phonon energy and deformation potential, respectively. The parameters of models *A* and *B* were taken from [15] and [16], respectively

parameter model	type of intervalley scattering	E_k [meV]	D_k [$\times 10^8$][eV/cm]
model <i>A</i> (Jacoboni)	f	19.0	0.3
		47.5	2.0
		59.1	2.0
model <i>B</i> (Yamada and Ferry)	g	12.1	0.5
		18.6	0.8
		62.2	11.0
model <i>C</i> (this work)	f	59.0	8.0
	g	63.0	8.0

weaker than the experimental one. Further refinements on the phonon scattering model including the effect of the anisotropic deformation potential [4, 17, 18] are also expected to provide better agreement.

Another unclear point regarding the universal mobility curve is the origin of η in E_{eff} . It has already been reported that the value of η is 1/2 for electrons on (100) [7–9, 11] and 1/3 for holes on (100) [10, 11] at room temperature. Furthermore, it has also been found [12] that the value of η is 1/3 for electrons on (110) and (111), suggesting that the subband structure can affect the value of η significantly. Although, according to (1), η is roughly 1/3, the only one subband is assumed for this equation. Thus, the detailed analysis of η including all the subbands and the contributions of intra- and inter-valley scattering [19] are required to clarify the origin.

3.2. Saturation Velocity

Saturation velocity, v_{sat} , in the inversion layer is a quite important physical quantity in determining the drain current in ultra-short channel MOSFETs. It seems, however, that the magnitude of v_{sat} in the inversion layer and the dependences on the physical parameters such as E_{eff} , N_s and T have not been fully established yet, partly because the large variation is seen in the measured values among the references [20–22]. While several data have suggested that v_{sat} in the inversion layer is lower than that in bulk, it has not been clarified whether the 2D quantization at the Si/SiO₂ interface has any influence on v_{sat} in the inversion layer. Thus, the relationship between the carrier velocity in the inversion layer and the tangential electric field has been evaluated, using MOSFETs with the resistive gate [20], in order to study the effect of the 2D quantization on v_{sat} . Figure 5 shows the experimental v - E curves as a parameter of N_s . The schematic cross section of the device structure is shown as the inset of Figure 5. It is observed that v_{sat} is dependent on N_s and decreases from the value in bulk Si, 1×10^7 cm/s, with increasing N_s ,

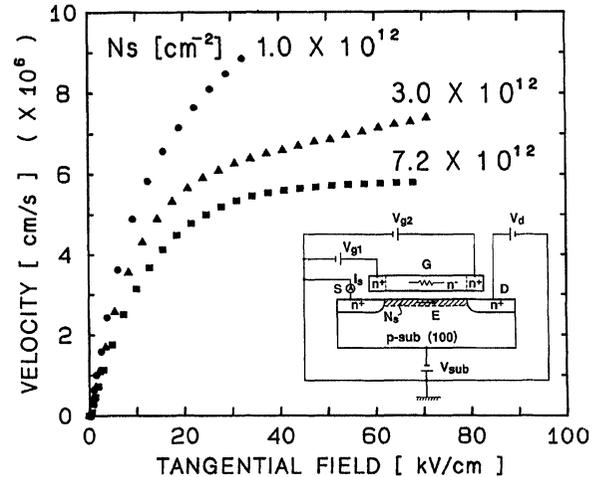


FIGURE 5 Experimental results of the electron velocity–electric field curves in the inversion layer at room temperature as a function of N_s . The direction of the electric field is parallel to (110) axis. The inset figure shows the schematic cross section of resistive gate MOSFETs to evaluate carrier velocity in the inversion layer. In order to realize the uniform N_s along the channel, the voltage of $V_{g1} + V_d$ is applied to the terminal V_{g2} .

though the saturation of v is not obtained at N_s of 1×10^{12} cm⁻².

One of the most important points in experimentally evaluating v_{sat} in the inversion layer is to realize the uniform distribution of N_s and the electric field along the channel of MOSFETs. Note that the velocity determined from the drain current in conventional MOSFETs is inaccurate because of the non-uniformity of N_s along the channel, unless MOSFETs with sufficiently thick gate oxides or SOI MOSFETs with sufficiently thick buried oxides are used [22]. The uniformity of N_s along the channel in the high-resistive gate MOSFETs shown in Figure 5 has been examined [23], using device simulations. As a consequence, it was found that, although a distribution of N_s along the channel is observed, the N_s dependence of v_{sat} in Figure 5 cannot be explained only by this non-uniformity of N_s , but this N_s dependence is provided by some feature inherent to carriers in the channel of MOSFETs.

In order to examine whether the lowering of v_{sat} with an increase in N_s is attributable or not to the 2-dimensional properties of carriers, the substrate

bias dependence of the velocity was measured. It should be noted that the N_s dependence of v_{sat} in Figure 5 can include both effects of the normal electric field and the carrier concentration, because V_g was simply changed to control N_s . The application of both V_g and V_{sub} allows to control N_s and E_{eff} separately. If the 2D quantization plays an important role in the lowering of v_{sat} , E_{eff} is expected to determine v_{sat} in the inversion layer. Figure 6 shows the v - E curves in the inversion layer with and without the substrate bias. The gate voltage in the curve *B* was adjusted so as to make E_{eff} in the curve *B* identical to that in the curve *C*, where the substrate bias of -6 V was applied. On the other hand, the curve *A* and the curve *C* have the same N_s . It is found in Figure 6 that the velocity in the curve *A* is almost the same as in the curve *C* and, thus, the velocity is determined not by E_{eff} but by N_s itself. This fact means that the lowering of v_{sat} with an increase in N_s might be attributable not to the 2-dimensional properties of carriers, but to an effect inherent to N_s or carrier concentration itself like carrier-carrier scattering.

One possible mechanism responsible for the N_s dependence of v_{sat} might be plasmon scattering [24]. If plasmon decays into electrons through the

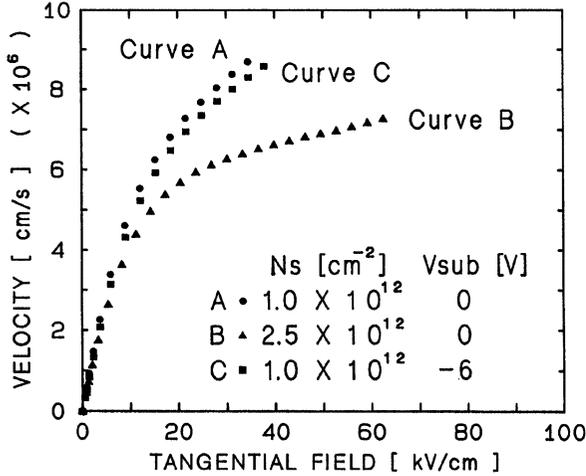


FIGURE 6 Electron velocity-electric field curves with (Curve C) and without (Curve A and B) the substrate bias, V_{sub} . While the value of N_s is in Curve C is the same as in Curve A, the values of E_{eff} in Curve C is the same as in Curve B.

emission of phonons, this process could become the energy dissipation mechanism of hot carriers under the high electric field. Note that the plasmon energy with the carrier concentration of $5 \times 10^{18} \text{ cm}^{-3}$, which is typically seen in the inversion layer, is 40 meV, which is almost the same as the energies of intervalley phonons seen in Table I. As the carrier concentration increases, the plasmon energy increases and the possibility of the energy loss due to the phonon emission might also increase. Further experimental evidence and theoretical verification on the relevance of plasmon with the energy loss of hot carriers in the inversion layer are strongly required.

4. INVERSION-LAYER CAPACITANCE

One of the most crucial limitations in the miniaturization of MOSFETs is that the gate capacitance cannot be sufficiently increased by thinning the gate oxide, because of the existence of the inversion-layer capacitance, C_{inv} [25–27]. Since the total gate capacitance, C_{tot} , is described by $C_{\text{ox}}/(1 + C_{\text{ox}}/C_{\text{inv}})$, the influence of C_{inv} becomes more serious with reducing the oxide thickness. Thus, it is quite important to clarify the origin of C_{inv} and to quantitatively evaluate C_{inv} . Figure 7 shows the schematic diagram of C_{inv} as a function of N_s under the simple analytical models [27], suggesting that the effect of the 2D quantization on C_{inv} is dominant in higher N_s region. The reason why the 2D quantization is important on C_{inv} is that the finite inversion-layer thickness, which effectively works as the series capacitance to the oxide capacitance, is much thicker in 2D carrier gas than in bulk carriers. In the model of the single subband occupation, C_{inv} due to the finite inversion-layer thickness under the 2D quantization can be simply described by

$$C_{\text{inv}}^{\text{thickness}} = \frac{\epsilon_{\text{Si}}}{Z_{\text{inv}}} = \left(\frac{4\epsilon_{\text{Si}}^2 q^2 m_3}{9\hbar^2} \right)^{1/3} \left(N_{\text{depl}} + \frac{11}{32} N_s \right)^{1/3} \approx \left(\frac{11\epsilon_{\text{Si}}^2 q^2}{72\hbar^2} \right)^{1/3} \cdot m_3^{1/3} \cdot N_s^{1/3} \quad (2)$$

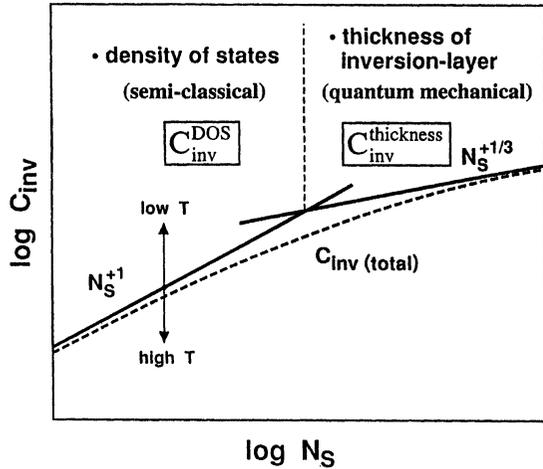


FIGURE 7 Schematic diagram of the physical origins of C_{inv} and the N_s dependence of C_{inv} under the simple analytical models [27].

Here, Z_{inv} is the average thickness of 2DEG, h is the Plank constant and m_3 is the effective mass of Si perpendicular to the Si/SiO₂ interface. According to this formulation, C_{inv} should have the dependence on m_3 . Figure 8 shows the experimental C_{inv} at room temperature as a function of

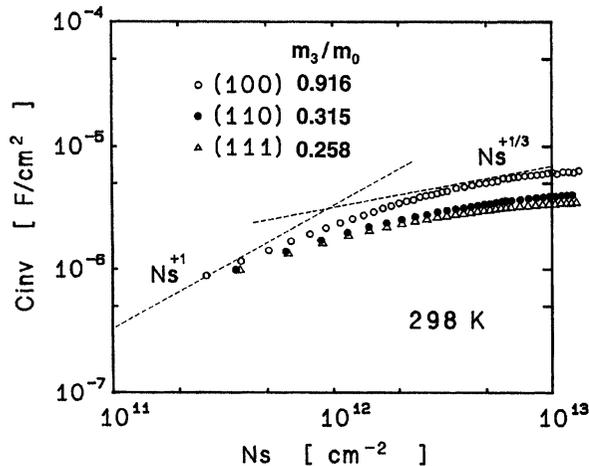


FIGURE 8 Experimental $C_{inv} - N_s$ curves for electrons in the inversion layer on (100), (110) and (111) surfaces at 298 K. The value of effective mass perpendicular to the interface, m_3 , is described for each surface orientation.

N_s for (100), (110) and (111) surfaces, which have the different values of m_3 . It is found that the measured values of C_{inv} become smaller in the order of (100), (110) and (111). Actually, it is confirmed that the surface orientation dependence of C_{inv} is explained quantitatively by the $m_3^{1/3}$ dependence. This result is the direct experimental evidence for the fact that C_{inv} at room temperature is determined by the quantum mechanical inversion-layer thickness, because the surface orientation does not make any difference for 3D carrier gas. This result also means that a larger value of m_3 leads to the suppression of the degradation of the gate capacitance due to C_{inv} .

Figure 9 shows the experimental and the calculated C_{inv} for inversion-layer electrons on (100) at room temperature. The calculated C_{inv} was determined directly from $d\Psi_s/dV_g$ through the self-consistent subband calculations without using any definition of the inversion-layer thickness [27]. It is confirmed that C_{inv} is accurately represented by the calculation, meaning that C_{inv} is quantitatively understood even at room temperature in terms of the 2D subband.

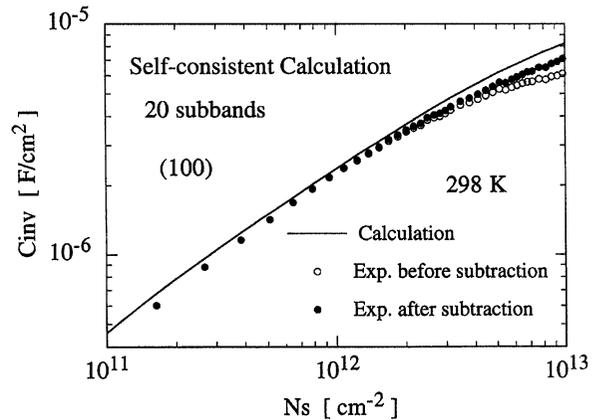


FIGURE 9 Comparison in $C_{inv} - N_s$ curves on (100) surface at 298 K between the self-consistent calculation and the experimental results. The open circles and the closes circles represent the results before and after the influence of the depletion layer in the poly-Si gate was subtracted from the experimental data. In the self-consistent subband calculation, 20 subbands (10 subbands for each subband ladder) were taken into account.

5. SUBBAND ENGINEERING FOR HIGHER PERFORMANCE MOSFETs

In order to obtain the higher current drive in MOSFETs, higher mobility and higher inversion-layer capacitance are required. In terms of the effective mass, these requirements mean lighter effective mass parallel to Si/SiO₂ interface, which increases mobility, and heavier effective mass perpendicular to the interface, which maximizes C_{inv} . From this viewpoint, the 2-fold valleys on a (100) surface are an optimum electronic system in the inversion layer of Si, as summarized in Figure 1. In conventional MOSFETs, however, the energy difference in the lowest subband energy of the 2-fold valleys, E_0 , and that of the 4-fold valleys, E'_0 , is small. As a result, the occupancy of the 2-fold valleys in conventional MOSFETs is not sufficiently large at room temperature. Therefore, an effective strategy to obtain the higher current drive is to increase the energy difference in the lowest subband, $E'_0 - E_0$. There are two possible ways to realize such a modulation in the subband structures. One way is to apply the tensile strain in Si substrate. It is known that tensile biaxial strain parallel to the interface causes the band splitting between the 2-fold valleys and the 4-fold valleys. This structure corresponds to strained Si MOSFETs. The other way is to utilize the size effect due to built-in confinement potential such as the band discontinuity at hetero-interfaces. For example, when SOI films in SOI MOSFETs is thinner than the inversion layer in bulk MOSFETs, the subband structures can be significantly modified and the resultant occupancy of the 2-fold valleys can increase by the size effect of the SOI film itself. The effectiveness of this subband engineering is examined through the subband and mobility calculations.

5.1. Strained Si MOSFETs

It is known that tensile strain in Si, which is typically seen in Si grown on relaxed SiGe, causes the band splitting between the 2- and the 4-fold

valleys, which leads to the increase in $E_0 - E'_0$ and the resulting higher occupation in the 2-fold valleys. As shown in Figure 10, it has been confirmed experimentally [28], [29] that the inversion-layer mobility in strained Si MOSFETs at room temperature increases up to around twice as high as in conventional MOSFETs with an increase in tensile strain, which is controlled by the Ge content of SiGe substrates. The calculated phonon-limited mobility for 2DEG in strained Si is also shown in Figure 10. Good agreement with the experimental mobility ratio is obtained by using the higher coupling constants with intervalley phonons (parameter set C). This is another evidence for the higher coupling of intervalley phonons with 2DEG in the inversion layer than with bulk electrons, as described in 3.1. The calculated results have also revealed that, in addition to the preferential occupation of the 2-fold valleys, the suppression of intervalley scatter-

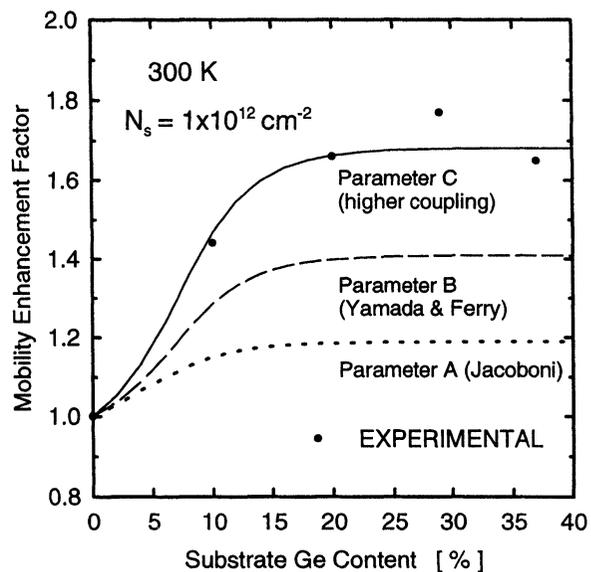


FIGURE 10 Mobility enhancement factor (the ratio of the mobility in strained Si MOSFETs to that in unstrained (conventional) Si MOSFETs) versus the Ge content of a SiGe substrate on which the strained layer is formed. The amount of strain in strained Si is in proportion to the Ge content. The experimental results were taken from [28]. The dotted, dashed and solid lines represent the calculated results using the intervalley phonon scattering parameter sets A, B and C.

ing due to the band splitting leads to the mobility enhancement in strained Si MOSFETs [6, 30]. It has also been found that C_{inv} in the inversion layer of Si slightly increases with tensile strain.

5.2. Ultra-Thin Film SOI MOSFETs

In order to examine the possibility of the modulation of the subband energy and the resultant occupancy of the 2-fold valleys in SOI MOSFETs with SOI films thinner than the inversion layer in bulk MOSFETs, the calculations of the subband structures and the phonon-limited mobility were performed [31]. Figure 11 shows the calculated phonon-limited mobility as a function of the SOI thickness, T_{SOI} . With decreasing T_{SOI} the mobility decreases slightly at first, and increases with decreasing T_{SOI} from 5 nm to 3 nm. With decreasing T_{SOI} from 3 nm, the mobility decreases again. It is found, moreover, that the mobility with the SOI thickness of around 3 nm can be higher than that in conventional MOSFETs. This enhancement is attributable to the fact that, with

decreasing the SOI thickness, the electron occupation of the 2-fold valleys becomes higher, because of the increase in E'_0 . The calculated occupancy of the 2-fold and the 4-fold valleys is shown as a function of T_{SOI} in Figure 12. It is confirmed that the occupancy of the 2-fold valleys increases with a decrease in T_{SOI} and becomes almost 100% around 3 nm of T_{SOI} . The reason why E'_0 increases more rapidly than E_0 with a decrease in T_{SOI} is that the inversion layer thickness of the 4-fold valleys is thicker than that of the 2-fold valleys and, thus, E'_0 is more sensitive to the SOI physical thickness than E_0 .

It has been also confirmed that C_{inv} in SOI MOSFETs with T_{SOI} thinner than 5 nm is significantly improved, because the inversion-layer thickness is determined by the SOI thickness itself [32]. These results demonstrate that, if the SOI MOSFETs that have the perfectly flat interfaces with the gate oxide and buried oxide can be realized, the performance of SOI MOSFETs with T_{SOI} of 3 nm to 5 nm can be much higher than that of bulk MOSFETs.

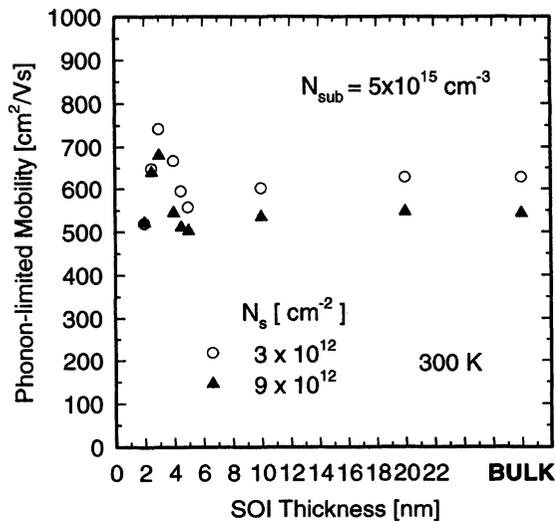


FIGURE 11 Calculated phonon-limited mobility in SOI MOSFETs as a function of SOI thickness at N_s of $3 \times 10^{12} \text{ cm}^{-2}$ and $9 \times 10^{12} \text{ cm}^{-2}$. The substrate impurity concentration and the buried oxide thickness are $5 \times 10^{15} \text{ cm}^{-3}$ and 100 nm, respectively.

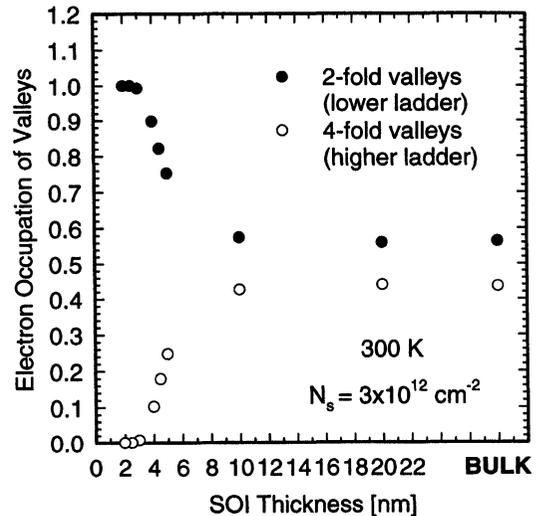


FIGURE 12 Calculated electron occupancy of the 2-fold and the 4-fold valleys as a function of the SOI thickness at N_s of $3 \times 10^{12} \text{ cm}^{-2}$.

6. CONCLUSION

The importance of the 2D features of the inversion layer electrons on the current drive of MOSFETs at room temperature has been re-examined through the systematic experiments and the self-consistent subband calculations. Inversion-layer mobility and inversion-layer capacitance can be understood well from the viewpoint of the 2D subband and the 2D carrier transport. However, further refinements in the scattering parameters and models are still needed to have fully-quantitative description of inversion-layer mobility. On the other hand, saturation velocity in the inversion layer is considered to be much less affected by the 2D features of carriers.

Based on the knowledge of the Si subband structures, an effective strategy for higher MOSFET performance, the enhancement of the occupancy of the 2-fold valleys on a (100) surface, has been presented. Higher mobility of strained Si MOSFETs and SOI MOSFETs with ultra-thin SOI films, both of which are the typical examples of this subband engineering, has been confirmed by the theoretical calculations.

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