Simulation of Quantum-Dot Structures in Si/SiO₂

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We present numerical simulations for the design of gated few-electron quantum dot structures in the Si/SiO₂ material system. Because of the vicinity of the quantum dots to the exposed surface, we take special care in treating the boundary conditions at the oxide/vacuum interfaces. In our simulations, the confining potential is obtained from the Poisson equation with a Thomas-Fermi charge model. We find that the dot occupancy can be effectively controlled in the few-electron regime.

Keywords: Silicon quantum dots, silicon/silicon dioxide, simulation and modeling, finite element method

We present numerical simulations for the design of gated few-electron quantum dot structures in the Si/SiO₂ material system. The motivation for this work is to investigate the feasibility of transferring the emerging technology of quantum dot fabrication from the III-V material system, where it was pioneered over the past few years, to the technologically more important Si/SiO₂ structures. Our main emphasis is on the realization, in silicon, of coupled quantum dot structures, so-called Quantum Cellular Automata [1]. Silicon appears to be a promising candidate due to the excellent insulating behavior of thin Si/SiO₂ films which yields the required crisp gate-control of the potential in the plane of the two-dimensional electron gas at the Si/SiO₂ interface. Another advantage of silicon for quantum dot applications appears to be the higher effective mass, as compared to the III-V materials, which reduces the sensitivity of the energy levels to size fluctuations.

Several recent studies have demonstrated the feasibility of fabricating quantum wire and dot structures in the silicon material system. Examples include mesoscopic transport studies of gate-induced quantum-dot arrays [2] and the proposal of a room-temperature single-electron memory [3].

The present simulations build upon our previous work on quantum dot modeling for the GaAs/AlGaAs material system [4,5], where we demonstrated that the dot occupancy can be effectively controlled in the few-electron regime using various biasing modes. We take special care in treating the boundary conditions for the confining potential at the exposed surfaces, i.e. the semiconductor or oxide to air interfaces. Because of the vicinity of the quantum dots (or wires) to the exposed surface, the choice of the boundary conditions to a large extent determines the behavior of the potential in the plane of the shallow two-dimensional electronic system. In our modeling, we do not make any assumptions about the value of the potential (or its derivative) on the surface. Rather, we treat the exposed surface as an interface between the air (or vacuum) above the structure to the

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As schematically shown in Fig. 1, we view both the semiconductor structure and the air above as one single solution domain, with matching conditions for the potentials and fluxes at the exposed surfaces. As described in detail in Ref. [4], we use a finite element method in the semiconductor domain and a boundary element method for the vacuum region. Since the Green function for the charge-free vacuum domain is known, only relatively few boundary elements suffice at the perimeter of the domain, thus only moderately increasing the total number of nodal points. In other words, with about the same numerical effort as for the semiconductor domain alone, we obtain the potential in both the semiconductor device and air regions.

In our simulations, the confining potential is obtained from the Poisson equation with a Thomas-Fermi charge model. No charges are assumed to exist within the oxide layer, or at the semiconductor/oxide and oxide/vacuum interfaces. A schematic diagram of the simulation region for dots with axial symmetry is shown in Fig. 2 with representative values for the
domain parameters. Typically, we use 2000 nodal points for the finite element portion and 100 boundary elements for the vacuum domain. In all simulations, a semi-insulating silicon substrate is assumed (actually, the substrate is slightly p-type with an unintentional acceptor density of \(10^{-15}\) cm\(^{-3}\)).

Quantum dots may be realized by applying a positive bias to a metallic gate on the surface, as schematically shown in the inset to Fig. 3. The positive voltage induces an inversion layer underneath the biased gate, which may lead to the formation of an “electron droplet” at the silicon/oxide interface, i.e., a quantum dot. Figure 3 shows, for an applied gate bias of 1.7 V, the corresponding potential variations along the Si/SiO\(_2\) interface; the Fermi energy is taken as the zero of energy and indicated by the thin horizontal line. An electronic system is induced when the silicon conduction band edge at the oxide interface, indicated by the solid line, dips below the Fermi level. We see that the formation of a quantum dot critically depends upon the thickness of the oxide layer. Our modeling shows that for a 10 nm gate radius an oxide thickness around (or below) 10 nm is required.

Figure 4(a) shows, for various oxide thicknesses, the radius of a bias-induced quantum dot, as schematically shown in the inset. The positive bias is applied to a circular gate with 10 nm radius.

Figure 4(b) presents the corresponding number of electrons in the quantum dot, which is obtained by integrating the electron density over the inversion region. The data shows that it should be feasible to create electronic systems with dimensions on the order of 10 nanometers, and that it should be possible to control the electron occupancy in the few-electron regime.

In summary, we have developed a numerical technique which allows us to model shallow electronic system by using special matching conditions on exposed surfaces. This enables us to study the electronic potential in near-surface quantum dot and wire systems. We have applied this numerical method for the design of gated quantum dots in Si/SiO\(_2\) structures. Our modeling shows that the dot occupancy can be effectively controlled in the few-electron regime.
FIGURE 4 Gate-induced quantum dot for various oxide thicknesses; shown are, as a function of gate bias, (a) the dot radius, and (b) the number of electrons occupying the dot.
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References


Biographies

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