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Signature Analysis for Test Responses of Sequential Circuits*

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Many test schemes use signature analyzers to compact the responses of a circuit under test. Unfortunately, there can be some faulty circuits with erroneous test responses but exactly the same signature as in the fault-free case. Hence, methods are required to determine how many faults become undetectable due to aliasing. Whereas previous work concentrated on combinational circuits, this paper investigates signature analysis for a wide range of sequential circuits, where the errors in successive responses are correlated. It is shown that for almost all faults of these circuits the probability of aliasing in a signature analyzer with k bits asymptotically approaches 2^{-k} or is 0 if a signature analyzer with an irreducible characteristic polynomial is used and certain test lengths are avoided. The limiting value can be used as a good approximation for practical test lengths. These results are particularly useful for advanced built-in self-test techniques with low hardware overhead.

Keywords: Aliasing, built-in self-test, correlated errors, sequential circuits, signature analysis, test response compaction

1. INTRODUCTION

Built-in self-test (BIST) is one of the most promising techniques for solving the test problems of large and complex circuits and systems [1]. Built-in pattern generators produce patterns that are applied to a (sub-)circuit under test (CUT). The test responses at the outputs of the CUT are collected by an integrated compactor. At the end of the test, the contents of the compactor (*i.e.*, the *signature* of the CUT) are compared to the signature of the fault-free circuit. If they do not agree, the CUT is considered faulty.

Due to a loss of information during compaction, however, even some response sequences that differ from the error-free sequence can lead to the

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error-free signature (*aliasing*). Thus, the CUT may contain a fault that causes errors in the test responses, but is not detected by a differing signature. In order to assess the quality of the applied self-test, it is important to determine how many of the faults can escape.

In principle, the exact number of masked faults can be determined by simulating the CUT and the response compactor for every single fault over the whole test length. But for large circuits, this is computationally unfeasible, in particular, if the simulations have to be done multiple times.

An alternative is to model the response compaction process in a probabilistic way and derive an analytical expression for the probability of aliasing. Then the portion of masked faults can be estimated simply by evaluating this formula. Most BIST techniques apply a large number of pseudo-random patterns resulting in an equally large number of test responses. Thus, the limiting value of the aliasing probability for large test lengths is the key point for evaluating the performance of a response compactor. Fast computation of this limiting value allows us to easily compare different types of compactors and to optimize the parameters of a compactor with respect to a minimal number of aliased faults.

For test response compaction, usually signature analyzers based on linear feedback shift registers [2] and cellular automata [3] are preferred since they can be implemented with a relatively small hardware overhead and achieve good compaction performance. Signature analysis for the responses of combinational circuits is well understood (see the review of previous work in Section 2). Successive test responses of combinational circuits and also the errors contained in them are statistically independent. The results of previous work can be used for BIST schemes that partition the circuit into purely combinational subcircuits and integrate all the flip-flops into scan paths or test registers. However, implementations of these BIST schemes require a relatively large hardware overhead and may slow down the circuit due to the slower scan flip-flops.

In contrast, with advanced BIST techniques only a subset of flip-flops is enhanced to scan flip-flops or test register cells [4–10]. Thus, the hardware overhead is reduced significantly and in many cases performance degradation can be avoided. Again, in the test mode the circuit is segmented into subcircuits that are surrounded by scan registers or test registers (*e.g.*, BILBOs [11]). But now the subcircuits contain flip-flops. As a consequence, errors in the test responses of the subcircuits can be correlated in time. All the previous results on aliasing which are based on the assumption of statistically independent test responses are not applicable; a new approach is required.

This paper deals with the sequential subcircuits that typically occur with advanced BIST techniques. To avoid excessive test lengths, these subcircuits usually have an acyclic structure at gate level such that they can be initialized easily. The assumptions that we use to derive our results on aliasing are significantly more general than in previous work, and many findings of recent years are included as special cases. In all situations where these assumptions hold, the aliasing probability tends to the smallest value that can be achieved, namely $1/2^k$ for a signature analyzer with k flip-flops.

The paper is an extension of [12]. It is organized as follows. Section 2 introduces a formal description of the test response compaction process and reviews previous work. Section 3 first gives an example of a sequential circuit where dependencies between successive response errors increase the probability of aliasing drastically compared to the probability predicted under the assumption of statistically independent errors. Then we propose a set of more general assumptions that hold for most circuits with BIST. In Section 4, the probability of aliasing in a signature analyzer is investigated under these general assumptions, and its limiting value for increasing test lengths is derived. Section 5 shows that numerous situations of practical importance are included. Experimental data, which have been obtained by simulation, are presented in Section 6 followed by conclusions in Section 7.

2. DESCRIPTION OF THE RESPONSE COMPACTION PROCESS AND PREVIOUS WORK

In this paper the circuit under test is a sequential circuit with arbitrary faults that manifest themselves as bit errors at the outputs of the circuit. Figure 1 shows the considered test environment. The pattern generator, the CUT, and the response compactor are clocked synchronously.

In the time interval between $t-1$ and t, a pattern $\mathbf{d}(t-1)$ is applied to the inputs of the CUT (see Fig. 2). At time t a new state $\mathbf{z}(t)$ is stored. Immediately after time t, a new pattern $\mathbf{d}(t)$ is applied. This causes the outputs to get a new value $\mathbf{r}(t)$ that depends on $\mathbf{d}(t)$ and $\mathbf{z}(t)$. With the following clock pulse at time $t+1$, the test response $\mathbf{r}(t)$ is compacted and the compactor reaches a new state $\mathbf{s}(t+1)$.

All the patterns, states, and test responses can be described by column vectors whose components are elements of GF(2). $\mathbf{0}$ denotes the all-zero vector. The bijective mapping $\mathbf{bin}: \{0, 1, \ldots, 2^k - 1\} \rightarrow \{0,1\}^k$ maps each integer $n \in \{0, 1, \ldots, 2^k - 1\}$ to its binary representation, $\mathbf{bin}(n) := (n_{k-1}, n_{k-2}, \ldots, n_0)^T$, where $n_\nu \in \{0,1\}$ for $\nu = 0, 1, \ldots, 2^k - 1$ and $\sum_{\nu=0}^{k-1} n_\nu \cdot 2^\nu = n$. In this paper, boldfaced letters like $\mathbf{n}$ stand for binary vectors, and italics like n denote the corresponding integers.

Figure 3 shows a signature analyzer based on a general linear finite state machine. As special cases, linear feedback shift registers and cellular automata are included. The contents of the register (k bits) are fed to a linear network, whose mapping is described by a $k \times k$-matrix C with entries of

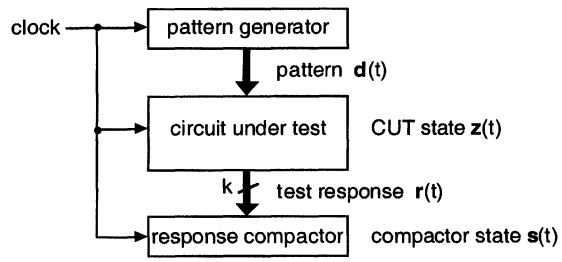

FIGURE 1 Test configuration.

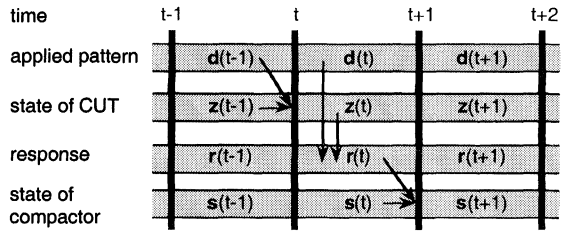

FIGURE 2 Dependencies during test execution.

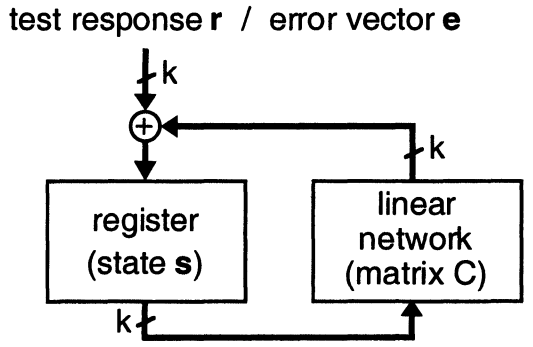

FIGURE 3 Signature analyzer.

$\{0,1\}$. The vector at the output of this network and the test response of the CUT (k-bit vector $\mathbf{r}$) are added bitwise modulo 2. The sum gives the next state of the signature analyzer, $\mathbf{s}(i+1) = C \cdot \mathbf{s}(i) \oplus \mathbf{r}(i)$. After a sequence of t test responses has been fed to the signature analyzer, the register contains the signature $\mathbf{s}(t) = C^t \mathbf{s}(0) \oplus \bigoplus_{i=0}^{t-1} C^{t-1-i} \mathbf{r}(i)$ where $\bigoplus_{i=0}^{n} \mathbf{x}(i)$ denotes the bitwise sum $\mathbf{x}(0) \oplus \mathbf{x}(1) \oplus \cdots \oplus \mathbf{x}(n)$.

As signature analysis is a linear operation, it is sufficient for the investigation of aliasing to consider the bitwise differences between the observed test responses $\mathbf{r}(i)$ and the error-free test responses $\mathbf{r}_{\mathbf{ef}}(i)$, namely the error vectors $\mathbf{e}(i) := \mathbf{r}(i) \oplus \mathbf{r}_{\mathbf{ef}}(i)$ [13]. Without restriction of generality, we initialize the signature analyzer to $\mathbf{s}(0) = \mathbf{0}$, and feed to it only the error vectors $\mathbf{e}(i)$. Then the signature at time t is $\mathbf{s}(t) = \bigoplus_{i=0}^{t-1} C^{t-1-i} \mathbf{e}(i)$. (Actually, this corresponds to the difference between the signature for the observed responses $\mathbf{r}$ and the signature

for the error-free responses $\mathbf{r_{ef}}$). For an error-free response sequence, $\mathbf{e}(0) = \mathbf{e}(1) = \cdots = \mathbf{e}(t-1) = \mathbf{0}$, we get $\mathbf{s}(t) = \mathbf{0}$. Aliasing occurs when erroneous test responses have been compacted, but still the signature of the error-free case is observed.

DEFINITION 1 The probability of aliasing at time t, $p_{al}(t)$, is the probability that the contents of the signature register at time t do not differ from the fault-free case and at least one nonzero error vector has occurred, $p_{al}(t) := \Pr(\mathbf{s}(t) = \mathbf{0}) - \Pr(\mathbf{e}(0) = \cdots = \mathbf{e}(t-1) = \mathbf{0})$.

In recent years, several different ways to model the errors have been proposed. The *symmetric channel error model* [14, 15] assumes that the error-free response vector occurs with probability p_0 and all the possible erroneous test responses have an equal probability of $(1-p_0)/(2^k-1)$. In the *independent error model* (*e.g.* [16]), error bits at different outputs of the CUT are statistically independent and can have different probabilities. The more general error model of [17] and [18] specifies the probabilities of all the 2^k possible error patterns individually. The common assumption of these error models is that errors in successive responses are *statistically independent*. This is valid for purely combinational circuits and faults that do not introduce sequential behavior. A multitude of results has been derived under these models including closed form expressions, simple bounds, and limiting values of the aliasing probability [14–17, 19, 20]. In particular, it has been proved that for every fault (regardless of the error probabilities) the aliasing probability of a signature analyzer is zero or tends to 2^{-k} for long test lengths provided that certain test lengths are avoided and the characteristic polynomial of the feedback matrix C is irreducible. 2^{-k} is the smallest asymptotic value that can be achieved if the error-free test response is not known a priori [21]. Simulation experiments have demonstrated that the asymptotic value is a good approximation of the actual aliasing probability if the test length is not extremely short [22–24].

However, if the CUT exhibits sequential behavior, errors in successive responses can be correlated. This makes the analysis of aliasing more complex. First studies dealt with conditions for aliasing and analyzed aliasing in presence of burst errors [16, 25, 26]. Recently, the symmetric channel error model has been extended to account for time correlation. The probability of an erroneous response is increased by a constant factor if the previous response has been erroneous [27]. Aliasing has also been studied for combinational circuits with stuck-open faults and delay faults [28, 29], for full scan designs with combinational faults [30], and for sequential circuits with fault-free hardware reset [31]. But these results are not sufficient for advanced BIST techniques which now are in the center of interest (see Section 1).

For the analysis of the aliasing probability $p_{al}(t)$, we describe the sequence of states of the signature analyzer by a stochastic chain $(S(t))_{t\geq 0}$ where every random variable $S(t)$ can assume values out of $\{0,1\}^k$ and determines the state $\mathbf{s}(t)$. The distribution of $S(t)$ is represented by $\pi(t) := (\pi_0(t), \pi_1(t), \ldots, \pi_{2^k-1}(t))^T$ with $\pi_i(t) := \Pr(S(t) = \mathbf{bin}(i))$, $i = 0, 1, \ldots, 2^k-1$. State transitions $j \to i$ are described by transition probabilities $p_{ij}(t)$. To be precise, $p_{ij}(t)$ is the conditional probability that the signature analyzer will be in state i at time $t+1$ if it is in state j at time t. The transition probabilities can be combined to a transition matrix $P(t) := (p_{ij}(t))_{0\leq i,j\leq 2^k-1}$. Then the distribution at time t is determined by $\pi(t) = P(t-1)\cdot\pi(t-1) = P(t-1)\cdot P(t-2)\cdot\cdots\cdot P(0)\cdot\pi(0)$, and $p_{al}(t) = \pi_0(t) - \Pr(\mathbf{e}(0) = \cdots = \mathbf{e}(t-1) = \mathbf{0})$.

The transition probabilities of the signature analyzer depend on the probabilities of the error patterns in the test responses. These in turn depend on the probabilities of the input patterns and on the current state of the CUT. So in general, the transition probabilities are not constant in time. Moreover, since the current state of the CUT depends on the previous state and on the previous inputs, the transition probabilities are correlated in time. Hence, in many cases the stochastic process $(S(t))_{t\geq 0}$ is not a Markov chain, and the well-known Markov models [16, 17, 19] cannot be used.

3. BASIC ASSUMPTIONS

Before the stochastic chain $(S(t))_{t\geq 0}$ is analyzed in order to derive results for the aliasing probability, the basic assumptions have to be discussed. We begin with an example of a sequential CUT where dependencies between errors in successive test responses increase the probability of aliasing compared to the probability predicted under the assumption of statistically independent errors.

Let E be the set of patterns that can occur as error vectors at the outputs of the CUT, $E := \{\mathbf{x} | \exists\, t \geq 0\ [\Pr(\mathbf{e}(t) = \mathbf{x}) > 0]\}$. For combinational CUTs with combinational faults, the aliasing probability approaches 2^{-k} for long test lengths provided that at least two error patterns can occur, $|E| \geq 2$, and the multiple input signature register (MISR) has an irreducible characteristic polynomial [16, 19]. If the same MISR is employed to compact the test responses of sequential CUTs where $|E| \geq 2$ also holds, but the errors are correlated in time, then $\lim_{t\to\infty} p_{al}(t) = 2^{-k}$ cannot be guaranteed. As an example we consider a CUT that includes a modulo 5 counter and some combinational logic and has 4 primary outputs. The circuit is tested using random patterns, the test responses are compacted by a 4-bit MISR with characteristic polynomial $x^4 + x + 1$ (see Fig. 4). The feedback matrix of the MISR is

$$C = \begin{pmatrix} 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{pmatrix}.$$

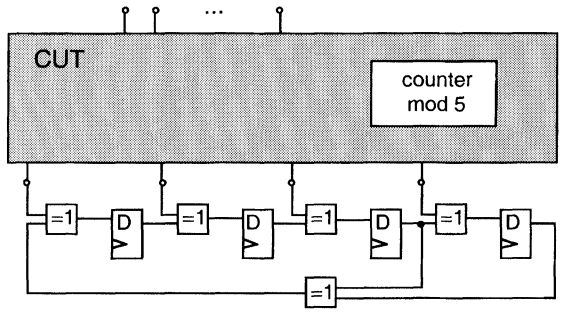

FIGURE 4 Test configuration of the example.

Let the CUT have a fault that can be observed at its outputs only if the embedded counter is in a specific state, *e.g.*, the state that is reached periodically at $t = 5i + 4$, $i = 0, 1, \ldots$ Furthermore, we assume that at these times the error vectors $\mathbf{0}$ and $\mathbf{a} \neq \mathbf{0}$ occur with probabilities p_0 and $1 - p_0$, respectively, $0 < p_0 < 1$. All the other test responses are error-free.

In order to analyze the aliasing probability, the MISR is initialized to $\mathbf{s}(0) = \mathbf{0}$ and the error vectors $\mathbf{e}(0), \mathbf{e}(1), \ldots$ are compacted. Considering the MISR at $t = 0, 5, 10, 15, \ldots$ we get the state transition diagram of Figure 5.

In this case the sequence of MISR states at times $t = 5i$ can be modelled by a Markov chain, $(S(5i))_{i\geq 0}$, which is aperiodic and irreducible. The transition matrix of this Markov chain,

$$\begin{pmatrix} p_0 & 0 & 0 & 1-p_0 \\ 1-p_0 & 0 & 0 & p_0 \\ 0 & p_0 & 1-p_0 & 0 \\ 0 & 1-p_0 & p_0 & 0 \end{pmatrix},$$

is doubly stochastic. Hence for long test lengths (*i.e.*, large values of i), at times $t = 5i$ the states $\mathbf{0}, \mathbf{a}, C^5\mathbf{a}$, and $C^{10}\mathbf{a}$ occur all with the same probability 0.25.

Since the test responses at $t = 5i, 5i+1, \ldots, 5i+3$ are always error-free, the transitions from $\mathbf{s}(5i)$ to $\mathbf{s}(5i+1)$, $\mathbf{s}(5i+2)$, $\mathbf{s}(5i+3)$, and $\mathbf{s}(5i+4)$ are deterministic,

$$\begin{aligned} \mathbf{s}(5i) &\in \{\mathbf{0}, \mathbf{a}, C^5\mathbf{a}, C^{10}\mathbf{a}\} \\ \mathbf{s}(5i+1) &\in \{\mathbf{0}, C\mathbf{a}, C^6\mathbf{a}, C^{11}\mathbf{a}\} \\ \mathbf{s}(5i+2) &\in \{\mathbf{0}, C^2\mathbf{a}, C^7\mathbf{a}, C^{12}\mathbf{a}\} \\ \mathbf{s}(5i+3) &\in \{\mathbf{0}, C^3\mathbf{a}, C^8\mathbf{a}, C^{13}\mathbf{a}\} \\ \mathbf{s}(5i+4) &\in \{\mathbf{0}, C^4\mathbf{a}, C^9\mathbf{a}, C^{14}\mathbf{a}\} \end{aligned}$$

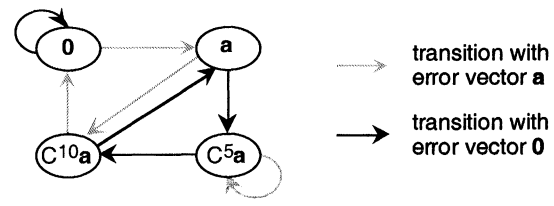

FIGURE 5 State transition diagram of the 4-bit MISR at $t = 5i$.

So at each point of time, only four states (including state **0**) are possible, and for long test lengths each of these states occurs with probability 0.25. Consequently, we get $\lim_{t\to\infty} p_{al}(t) = 2^{-2}$, not $2^{-k} = 2^{-4}$.

It can be shown that choosing any other characteristic polynomial of the same degree or replacing the MISR with external XORs by a MISR with internal XORs cannot improve the situation. Generally, whatever the features of the MISR are, sequential CUTs and faults can be found such that the aliasing probability converges to a limiting value much larger than the optimal value 2^{-k}.

But on the other side, useful circuits do not have arbitrary structures. Design for testability and particularly built-in self-test lead to restrictions of the design space. These restrictions can be exploited when test response compaction and aliasing are analyzed. The following assumptions consider typical BIST environments, but they are also valid in many other cases. In the next section, it will be shown that these assumptions guarantee that the aliasing probability tends to 2^{-k} for increasing test lengths.

(i) The input patterns are chosen randomly.

(ii) For at least one state $\mathbf{z_0}$ of the CUT a synchronizing sequence exists. The synchronization state $\mathbf{z_0}$ as well as the synchronizing sequence may be different for circuits with different faults.

(iii) For a faulty circuit initialized to a synchronization state $\mathbf{z_0}$, there are input sequences $\mathbf{d}(0), \mathbf{d}(1), \ldots, \mathbf{d}(t-1)$ and $\mathbf{d}'(0), \mathbf{d}'(1), \ldots, \mathbf{d}'(t-1)$ that transfer the CUT to the same state, $\mathbf{z}(t) = \mathbf{z}'(t)$, but result in different signatures, $\mathbf{s}(t) \neq \mathbf{s}'(t)$.

(iv) The characteristic polynomial $\det(xI - C)$ of the matrix C, which specifies the linear feedback network of the signature analyzer, is irreducible, *i.e.*, it cannot be factored. (I is the identity matrix.)

Motivated by numerous BIST schemes which apply pseudorandom patterns, all the known probabilistic models implicitly or explicitly assume that test patterns are applied randomly (assumption (i)). The input patterns can have different probabilities of occurrence.

A synchronizing sequence is defined as an input sequence whose application is guaranteed to leave the circuit in a certain final state regardless of its initial state. Signature analysis testing requires that the signature of the fault-free circuit is known. This is possible only if the circuit is initialized to a known state before testing begins. Thus a synchronizing sequence must exist.

Moreover, many partial scan and partial intrusion BIST techniques break all cycles of the circuit structure by inserting scan flip-flops or test register cells [4–6, 8, 10]. Then every state of the resulting acyclic circuit can be reached with a number of input vectors that corresponds to the sequential depth of the circuit. So synchronizing sequences exist for all states. And we can expect that also for the faulty circuit there is a synchronizing sequence for at least one state, and assumption (ii) is valid.

In order to point out that assumption (iii) holds in almost all cases, we consider the two situations (a) and (b) where it does not hold.

(a) *All input sequences lead to the same sequence of signatures* $\mathbf{s}(1), \mathbf{s}(2), \ldots$
This means that the error vectors $\mathbf{e}(0), \mathbf{e}(1), \ldots$ do not depend on the input vectors. Since the state of the CUT is influenced by the input vectors (see the discussion of assumption (ii)), the error vectors cannot depend on the state of the CUT, too. Hence all the error vectors must have the same value. In this situation it does not matter whether the test responses originate from a combinational or sequential CUT. The following theorem considers this situation and was proved in [19].

THEOREM 1 *Suppose that a signature analyzer with irreducible characteristic polynomial compacts a sequence of t identical error vectors $\boldsymbol{e}(0) = \boldsymbol{e}(1) = \cdots = \boldsymbol{e}(t-1) = \boldsymbol{e}$. In the state transition diagram of the signature analyzer that operates under constant input $\boldsymbol{r} = \mathbf{0}$, let n_e be the length of the cycle that contains state $\boldsymbol{e}$. For $\boldsymbol{e} \neq \mathbf{0}$ aliasing occurs if and only if t is a multiple of n_e.*

If the characteristic polynomial of the signature analyzer is a primitive polynomial of degree k, for $\boldsymbol{e} \neq \mathbf{0}$ we get aliasing exactly at $t = 2^k - 1$, $2 \cdot (2^k - 1)$, $3 \cdot (2^k - 1)$, and so on. For $\boldsymbol{e} = \mathbf{0}$ the test responses equal the responses of the fault-free circuit and aliasing does not occur.

(b) *There are input sequences that result in different signatures, but whenever the signatures differ, the states of the CUT differ, too.*

Then $\mathbf{z}(t) = \mathbf{z}'(t) \Rightarrow \mathbf{s}(t) = \mathbf{s}'(t)$ holds for all pairs of input sequences. It can be shown that this condition is satisfied if and only if there is a mapping $\mathbf{f}$ that maps each state $\mathbf{z}$ to exactly one signature $\mathbf{s}$.

Using the arbitrary, but fixed next state function of the CUT, the input vector $\mathbf{d}(i)$ and the present state $\mathbf{z}(i)$ lead to the next state $\mathbf{z}(i+1)$. With a fixed mapping $\mathbf{f}$, the state $\mathbf{z}(i)$ determines the present signature $\mathbf{s}(i)$, and $\mathbf{z}(i+1)$ determines the next signature $\mathbf{s}(i+1)$. In order to change the contents of the signature register from $\mathbf{s}(i)$ to $\mathbf{s}(i+1)$, the error vector $\mathbf{e}(i) = \mathbf{s}(i+1) \oplus C\mathbf{s}(i)$ must occur.

In general, $\mathbf{e}(i)$ is a function of $\mathbf{d}(i)$ and $\mathbf{z}(i)$. This function $\mathbf{g}(\mathbf{d}, \mathbf{z})$ is implicitly implemented by the combinational part of the faulty circuit. The number of possible functions $\mathbf{g}$ is $2^{k \cdot n_d \cdot n_z}$ where n_d is the number of possible input patterns and n_z is the number of possible states. In the special situation considered, the error vector $\mathbf{e}(i)$ is determined by the next state function of the CUT and the mapping $\mathbf{f}$. Since the next state function is fixed and the number of possible mappings $\mathbf{f}$ is $2^{k \cdot n_z}$, the portion of functions $\mathbf{g}$ that satisfy the imposed restrictions is $2^{k \cdot n_z} / 2^{k \cdot n_d \cdot n_z} = 1/2^{k \cdot (n_d - 1) \cdot n_z}$. This value is extremely small. Even for a very small circuit with 5 inputs (32 possible input patterns), 3 outputs, and 10 states, we get $1/2^{k \cdot (n_d - 1) \cdot n_z} = 1/2^{3 \cdot 31 \cdot 10} < 10^{-270}$.

So we can conclude that assumption (iii) holds for almost all faulty circuits where the error vectors are not identical.

For statistically independent error vectors, only the signature analyzers with irreducible characteristic polynomials can guarantee the asymptotic aliasing probability limit of 2^{-k} [17]. Since statistically independent error vectors are a special case of the situation considered here, a condition weaker than (iv) cannot be sufficient for a limiting value of 2^{-k}.

In contrast to the error models of previous approaches, which make assumptions on the distribution of the errors at the outputs of the CUT, the assumptions used here refer to the CUT directly. So it should be easier to verify them for a specific CUT.

4. PROBABILITY OF ALIASING

This section shows that the assumptions stated in the previous section are sufficient for the aliasing probability to converge to the limiting value 2^{-k}. We proceed in the following way. First, it is proved that the stochastic chain $(S(t))_{t \geq 0}$, which describes the sequence of states of the signature analyzer, is irreducible and aperiodic. Its transition matrices are doubly stochastic. Then, using these facts we prove that $(S(t))_{t \geq 0}$ has a limiting distribution. Finally, the limit of the aliasing probability is derived from this distribution.

As the transition probabilities of the stochastic chain are not constant in time, the definition of the terms "irreducible" and "aperiodic" must consider time explicitly. The following definitions include the corresponding definitions for time homogenous Markov chains [32] as a special case.

DEFINITION 2 A state i is *reachable* from state j if for each time $t \geq 0$ there is a number n_t such that the n_t-step transition probability $p_{ij}^{(n_t)}(t)$ is nonzero.

DEFINITION 3 A stochastic chain is *irreducible* if each state is reachable from each state.

DEFINITION 4 A state j of a stochastic chain is *aperiodic* if there does not exist a time $t \geq 0$ and a number $w > 1$ with $p_{jj}^{(n)}(t) = 0$ for all $n \notin \{w, 2w, 3w, \ldots\}$. A stochastic chain is called aperiodic if all its states are aperiodic.

The next lemma shows that the stochastic chain $(S(t))_{t \geq 0}$ is irreducible and aperiodic.

LEMMA 1 *Let a signature analyzer with irreducible characteristic polynomial compact the test responses of a circuit where the assumptions* (ii) *and* (iii) *hold. Then the stochastic chain* $(S(t))_{t\geq 0}$ *describing the state sequence* $\mathbf{s}(0), \mathbf{s}(1), \ldots$ *of the signature analyzer is irreducible and aperiodic.*

Proof See appendix.

It can easily be proved that for a signature analyzer with irreducible characteristic polynomial the transition matrices $P(t)$ of the stochastic chain $(S(t))_{t\geq 0}$ are doubly stochastic (*i.e.*, every row sum and also every column sum gives 1).

The distribution $\pi = (1/2^k, \ldots, 1/2^k)^T$ is a stationary distribution of the stochastic chain $(S(t))_{t\geq 0}$ since $\pi = P(t)\cdot\pi$ holds for every doubly stochastic matrix $P(t)$. The following theorem shows that this stationary distribution is the unique limiting distribution.

THEOREM 2 *Let* $(S(t))_{t\geq 0}$ *be the stochastic chain that describes the state sequence of a signature analyzer with an irreducible characteristic polynomial of degree* k. *If the assumptions* (ii) *and* (iii) *hold, the limiting distribution of* $(S(t))_{t\geq 0}$ *exists and its value is* $\lim_{t\to\infty}\pi(t) = (1/2^k, \ldots, 1/2^k)^T$.

Proof In order to prove that the distribution $\pi(t)$ converges to $(1/2^k, \ldots, 1/2^k)^T$, it is sufficient to show that the difference between the maximum and the minimum of the state probabilities, $\pi_{\max}(t) := \max_{0\leq i\leq 2^k-1}\{\pi_i(t)\}$ and $\pi_{\min}(t) := \min_{0\leq i\leq 2^k-1}\{\pi_i(t)\}$, respectively, tends to 0 for $t\to\infty$. $\lim_{t\to\infty}(\pi_{\max}(t) - \pi_{\min}(t)) = 0$ implies that the probabilities of all states become equal and tend to $1/2^k$.

Every m-step transition matrix $P^{(m)}(t) = P(t+m-1)\cdot\cdots\cdot P(t)$, $m > 0$, is doubly stochastic since it is a product of doubly stochastic matrices. Let $p_{\min}^{(m)}(t)$ be the smallest element of $P^{(m)}(t)$. Then we have

$$\pi_i(t+m) = \sum_{j=0}^{2^k-1} p_{ij}^{(m)}\cdot\pi_j(t) \leq \pi_{\max}(t)\cdot(1 - p_{\min}^{(m)}(t)) + \pi_{\min}(t)\cdot p_{\min}^{(m)}(t)$$

In particular, this holds for an index i with $\pi_i(t+m) = \pi_{\max}(t+m)$ and gives

$$\pi_{\max}(t+m) \leq \pi_{\max}(t) - p_{\min}^{(m)}(t)\cdot(\pi_{\max}(t) - \pi_{\min}(t))$$

In a similar way,

$$\pi_{\min}(t+m) \geq \pi_{\min}(t) + p_{\min}^{(m)}(t)\cdot(\pi_{\max}(t) - \pi_{\min}(t))$$

is obtained. Combining the last two inequalities we get

$$\begin{aligned}\pi_{\max}(t+m) - \pi_{\min}(t+m) &\leq (1 - 2p_{\min}^{(m)}(t))\cdot(\pi_{\max}(t) - \pi_{\min}(t)) \\ &\leq \pi_{\max}(t) - \pi_{\min}(t)(*)\end{aligned}$$

The difference $\pi_{\max}(t) - \pi_{\min}(t)$ is monotonically decreasing with the increase of the test length t.

As the stochastic chain $(S(t))_{t\geq 0}$ is irreducible and aperiodic (Lemma 1), a constant m_0 exists such that for arbitrary $t\geq 0$ each state $\mathbf{s}(t+m_0)$ can be reached from each state $\mathbf{s}(t)$. (The proof of Lemma 1 gives $m_0 = k\cdot u + t_{\text{sync}}$). Every m_0-step state transition is caused by at least one specific input pattern sequence of length m_0. Let q be the smallest nonzero probability of occurrence of all possible m_0-pattern input sequences. Then we certainly have $p_{\min}^{(m_0)}(t) \geq q > 0$ for all $t\geq 0$. According to $(*)$, at time $t = h\cdot m_0$ the difference $\pi_{\max}(t) - \pi_{\min}(t)$ is at most $(1-2q)^h$. Because of $\lim_{h\to\infty}(1-2q)^h = 0$ we finally get $\lim_{t\to\infty}(\pi_{\max}(t) - \pi_{\min}(t)) = 0$, which completes the proof. Q.E.D.

Finally, the following corollary gives the limit of the aliasing probability.

COROLLARY 1 *Let a signature analyzer with irreducible characteristic polynomial of degree* k *compact the test responses of a combinational or sequential circuit. If the assumptions* (ii) *and* (iii) *hold, the probability of aliasing converges to* $\lim_{t\to\infty} p_{al}(t) = 2^{-k}$.

Proof Since in the error vector sequence at least two different values occur with nonzero probabilities, the probability that the sequence of test

responses is error-free tends to 0 as the test length t tends to infinity, $\lim_{t\to\infty}\Pr(\mathbf{e}(0)=\cdots=\mathbf{e}(t-1)=\mathbf{0})=0$. Using Definition 1 and Theorem 2, this gives $\lim_{t\to\infty} p_{al}(t)=\lim_{t\to\infty}\Pr(\mathbf{s}(t)=\mathbf{0})=\lim_{t\to\infty}\pi_0(t)=1/2^k$. Q.E.D.

Taken together, Theorem 1 and Corollary 1 show that for almost all faults the probability of aliasing in the signature analyzer asymptotically approaches 2^{-k} and in special cases it is zero provided that certain test lengths are avoided.

5. IMPORTANT CASES

The result of the previous section includes many results known from literature as special cases, *e.g.* [16, 17, 19, 28–31]. In order to demonstrate the broad range of circuit and fault classes that are covered by the assumptions described in Section 3, we show for some important cases that the assumptions are satisfied (in particular assumptions (ii) and (iii)).

5.1. Combinational Circuits with Combinational Faults

Combinational faults (*e.g.*, stuck-at faults) change the function of the circuit, but in contrast to delay faults and stuck-open faults they do not introduce sequential behavior. Thus the CUT is always in the same state, and explicit synchronization is not required. The synchronizing sequence has length 0. If the fault is detected by some but not all input patterns, or more general $|E|\geq 2$, then input patterns $\mathbf{d}(0)$ and $\mathbf{d}'(0)$ exist that lead to error vectors $\mathbf{e}(0)\neq\mathbf{e}'(0)$ and thus $\mathbf{s}(1)\neq\mathbf{s}'(1)$. So assumptions (ii) and (iii) hold, and Theorem 2 and Corollary 1 include the results that have been proved in [16, 17, 19] for the limiting value of $p_{al}(t)$.

5.2. Combinational Circuits with Delay Faults that Cause Errors Lasting One Clock Cycle

Delay faults most frequently do not exceed one clock period. If two successive input patterns are identical, $\mathbf{d}(t-1)=\mathbf{d}(t)$, then the response $\mathbf{r}(t-1)$ may be erroneous due to the delay fault, but the response $\mathbf{r}(t)$ is error-free. Generally, $\mathbf{r}(t)$ depends on $\mathbf{d}(t)$ and in case of a delay fault also depends on $\mathbf{d}(t-1)$, but not on any input patterns applied before time $t-1$. Hence, an arbitrary pattern $\mathbf{d}(t-1)$ can serve as a synchronizing sequence because it uniquely determines the transient state of the circuit at time t.

Testing such a delay fault requires a pair of input patterns applied at speed. The first pattern initializes the circuit, the second pattern makes the fault observable at a primary output of the circuit. Let $(\mathbf{d}_{\text{init}}, \mathbf{d}_{\text{test}})$ be a test pattern pair for the delay fault. Then the input sequences

$$(\mathbf{d}(0)=\mathbf{d}_{\text{init}},\ \mathbf{d}(1)=\mathbf{d}_{\text{test}},\ \mathbf{d}(2)=\mathbf{d}_{\text{test}})$$

and

$$(\mathbf{d}'(0)=\mathbf{d}_{\text{init}},\ \mathbf{d}'(1)=\mathbf{d}_{\text{init}},\ \mathbf{d}'(2)=\mathbf{d}_{\text{test}})$$

lead to the same transient state at time $t=3$ since $\mathbf{d}(2)=\mathbf{d}'(2)$ holds. But the signatures are different:

$$\mathbf{s}(3)=C^2\mathbf{e}(0)+C\mathbf{e}(1)+\mathbf{e}(2)$$

$$\mathbf{s}'(3)=C^2\mathbf{e}'(0)+C\mathbf{e}'(1)+\mathbf{e}'(2)$$

and

$$\mathbf{e}(0)=\mathbf{e}'(0),\quad \mathbf{e}(1)=\mathbf{e}'(2),\quad \mathbf{e}(2)=\mathbf{e}'(1)=\mathbf{0}$$

give $\mathbf{s}(3)-\mathbf{s}'(3)=C\mathbf{e}(1)-\mathbf{e}(1)=(C-I)\cdot\mathbf{e}(1)\neq\mathbf{0}$ because of $C\neq I$ and $\mathbf{e}(1)\neq\mathbf{0}$.

Consequently, assumption (iii) holds.

5.3. Combinational Circuits with Stuck-open Faults

Stuck-open faults in CMOS circuits make it impossible to charge or discharge a circuit node when certain input patterns are applied. In this way, sequential behavior is introduced without creating feedback connections. The state of the circuit is determined by the charge stored at the nodes.

As the faulty circuit still has an acyclic structure, input sequences exist that set the circuit to specific states regardless of the initial state. Let the circuit be initialized to an arbitrary, but fixed state at time $t = 0$. If the considered single or multiple stuck-open fault is detectable, there must be an input sequence

$$(\mathbf{d}(0), \ldots, \mathbf{d}(t-3), \mathbf{d}(t-2), \mathbf{d}(t-1)) \quad \text{with} \quad \mathbf{d}(t-2) = \mathbf{d}(t-1)$$

that gives an error sequence

$$(\mathbf{e}(0), \ldots, \mathbf{e}(t-3), \mathbf{e}(t-2), \mathbf{e}(t-1)) \quad \text{with} \quad \mathbf{e}(t-3) \neq \mathbf{e}(t-2) \quad \text{and} \quad \mathbf{e}(t-2) = \mathbf{e}(t-1)$$

$$\textit{e.g.} \qquad (\mathbf{e}(0), \ldots, \mathbf{e}(t-3), \mathbf{e}(t-2), \mathbf{e}(t-1)) = (\mathbf{0}, \ldots, \mathbf{0}, \mathbf{a}, \mathbf{a}), \quad \mathbf{a} \neq \mathbf{0}$$

Of course, if successive input patterns are identical, the corresponding error vectors are identical, too. Also the input sequence

$$(\mathbf{d}'(0), \ldots, \mathbf{d}'(t-3), \mathbf{d}'(t-2), \mathbf{d}'(t-1)) := (\mathbf{d}(0), \ldots, \mathbf{d}(t-3), \mathbf{d}(t-3), \mathbf{d}(t-1))$$

can occur where the input pattern $\mathbf{d}(t-2)$ has been replaced by $\mathbf{d}(t-3)$. In this case, we get the error sequence

$$(\mathbf{e}'(0), \ldots, \mathbf{e}'(t-3), \mathbf{e}'(t-2), \mathbf{e}'(t-1)) = (\mathbf{e}(0), \ldots, \mathbf{e}(t-3), \mathbf{e}(t-3), \mathbf{e}(t-1))$$

At time t the CUT is in the same state in both cases. But the signatures are different:

$$\mathbf{s}(t) - \mathbf{s}'(t) = C\mathbf{e}(t-2) - C\mathbf{e}'(t-2) = C \cdot (\mathbf{e}(t-2) - \mathbf{e}(t-3)) \neq \mathbf{0}$$

Again, assumptions (ii) and (iii) hold.

5.4. Full Scan Circuits with Combinational Faults

Figure 6 illustrates the test configuration for a circuit with full scan. Every input pattern contains

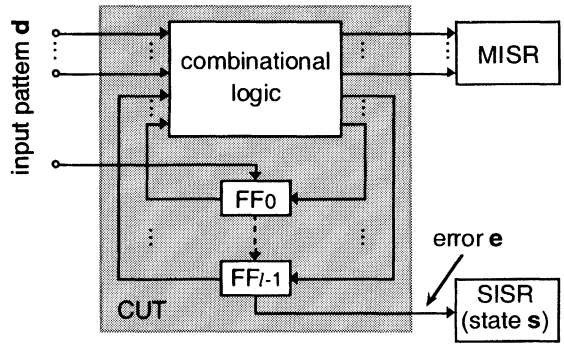

FIGURE 6 Test configuration for a circuit with full scan.

one bit for the serial input of the scan path, the other bits are applied to the primary inputs of the combinational part of the circuit (or ignored). Let l be the length of the scan path. Each input sequence of length l is a synchonizing sequence since it sets the circuit to a new state regardless of the previous state. After that, the immediate response at the primary outputs is compacted by a MISR, and the next state response is latched in the scan path. Concurrently to shifting a new bit sequence into the scan path, the bits of the next state are shifted out and compacted by a single input signature analyzer (SISR). Test response compaction for the combinational part of the circuit has already been considered at the beginning of this section. Here we consider aliasing in the signature analyzer connected to the serial output of the scan path. Only the clock pulses for shifting the scan path and simultaneously compacting its contents are counted.

In the rare cases where the errors contained in the scan path, $(\mathbf{e}(0), \ldots, \mathbf{e}(l-1))$, always lead to the same partial signature $\mathbf{s}(l) = \bigoplus_{i=0}^{l-1} C^{l-1-i}\mathbf{e}(i)$, aliasing occurs periodically at fixed points of time. A detailed analysis gives results similar to Theorem 1. In all the other cases, there are input sequences $(\mathbf{d}(-l), \ldots, \mathbf{d}(0), \ldots, \mathbf{d}(l-1))$ and $(\mathbf{d}'(-l), \ldots, \mathbf{d}'(0), \ldots, \mathbf{d}'(l-1))$ with $\mathbf{d}(i) = \mathbf{d}'(i)$ for $i = 0, \ldots, l-1$ that lead to error sequences $(\mathbf{e}(0), \ldots, \mathbf{e}(l-1))$ and $(\mathbf{e}'(0), \ldots, \mathbf{e}'(l-1))$ such that the signatures differ, $\mathbf{s}(l) \neq \mathbf{s}'(l)$. In both cases the resulting state of the CUT is the same, $\mathbf{z}(l) = \mathbf{z}'(l)$.

If the SISR has a characteristic polynomial of degree k that is irreducible, the state transition diagram of the SISR operating under constant input 0 consists of cycles that all have the same length n_c and one cycle of length 1 [33]. Of course, n_c must be a divisor of $2^k - 1$. Lemma 1 requires synchronizing sequences of length u where u is relatively prime to n_c (see appendix). In the special situation considered here, synchronization can be achieved only after $l, 2l, 3l, \ldots$ input vectors. Hence, Lemma 1 applies if and only if the length of the scan path is relatively prime to n_c, *i.e.*, gcd $(l, n_c) = 1$, and then Theorem 2 and Corollary 1 hold. This is a more general result than presented in [30] where the limiting value $\lim_{t\to\infty} p_{al}(t) = 2^{-k}$ has been proved only for signature analyzers with primitive characteristic polynomials and gcd $(l, 2^k - 1) = 1$. In addition, the derived limiting value is also valid for stuck-open faults in the combinational part of the CUT.

5.5. Sequential Circuits with Hardware Reset

Under the assumption that the reset mechanism is not degraded to partial reset in the faulty circuit, every input pattern with active reset bit is a synchronizing sequence. If not all the error patterns are identical, then assumption (iii) holds (see also [31]), and again we have the same limiting value of the aliasing probability.

6. EXPERIMENTAL RESULTS

In practice, the signature of the fault-free circuit must be known. So the pattern sequence applied to the inputs can be chosen arbitrarily, but for all chips implementing the same design the pattern sequence must be the same. This implies that the times where the circuit is forced to a synchronization state are the same for most of these chips. Due to different faults, however, the applied patterns can cause a multitude of different error sequences at the outputs of the CUTs.

In order to emphasize the difference to signature analysis for combinational circuits, here experiments are described where successive error vectors are strongly correlated. It was assumed that a part of the circuit under test behaves like a resettable counter with a cycle of length w. At time $t = 0$ the CUT was initialized to a known state $\mathbf{z_0}$ for which a synchronizing sequence existed. After state $\mathbf{z_0}$ had been left, only the w-th, $2w$-th, $3w$-th, ... test response could be erroneous. At these times nonzero error patterns occurred with probability $1-p_0$. All the other test responses (including the test responses in state $\mathbf{z_0}$) were error-free. The CUT was forced to state $\mathbf{z_0}$ again at times that were kept fixed throughout an experiment. Before the experiment started, these synchronization points were chosen randomly, each point of time was selected as a synchronization point with a given probability p_{sync}.

The first set of experiments dealt with a CUT having 4 outputs. Using a random number generator, 100 000 test response sequences were generated according to the above specification with $w = 5$, $p_0 = 0.5$, possible error patterns $(0, 0, 0, 0)^T$ and $(0, 0, 1, 0)^T$, and different sequences of synchronization points ($p_{\text{sync}} = 0.1$). Compaction with the same 4-bit MISR as in Figure 4 was simulated, and the aliasing events were counted for each time t separately. At time t an aliasing event occurs if some nonzero error vectors have appeared, but the signature $\mathbf{s}(t)$ is $\mathbf{0}$. The probability of aliasing was estimated by

$$p_{al}(t) = \frac{\#\text{ aliasing events at time } t}{\#\text{ simulated test response sequences}}$$

Figure 7 shows the results. Experiments (a) and (b) used two different sequences of synchronization points. For short test lengths, the aliasing probability strongly depends on the actual sequence of synchronization points. But for longer test lengths, the aliasing probability approaches the same limiting value of $2^{-4} = 0.0625$.

A second set of experiments was carried out using a MISR with the irreducible characteristic polynomial $x^8 + x^5 + x^4 + x^3 + 1$ (not primitive) and a sequence of synchronization points produced

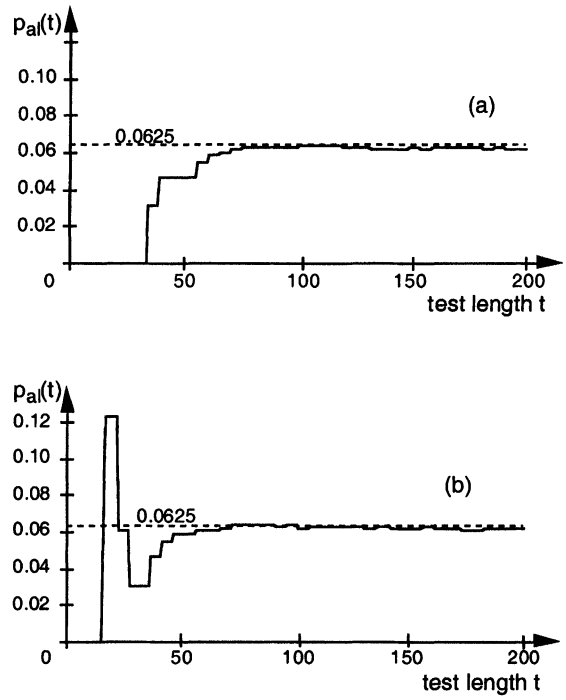

FIGURE 7 Probability of aliasing in the 4-bit MISR, test response sequences with error patterns **0** and $(0,0,1,0)^T$ for two different sequences of synchronization points.

with $p_{\text{sync}} = 0.01$. The test response sequences were generated with $w = 3, p_0 = 0.9$. In order to find out how the number of possible error patterns influences the aliasing probability as a function of the test length, two very different situations were investigated. In one situation only one nonzero error pattern could occur. The 3rd, 6th, 9th, ... test response was chosen to be $(0,0,1,1,1,0,0,0)^T$ with probability 0.1. In the other situation, at these times every nonzero error pattern occurred with equal probability 0.1/255. For both situations, 10^7 test response sequences were simulated. Figure 8 shows the results.

In both cases, the number of nonzero error vectors was almost the same. But due to the larger number of different error patterns, in case (b) the aliasing probability approaches its limit faster. For $t \geq 118$, all values of $p_{al}(t)$ are within $\pm 10\%$ of the limiting value $2^{-8} = 0.0039$. For case (a) the corresponding test length is 161.

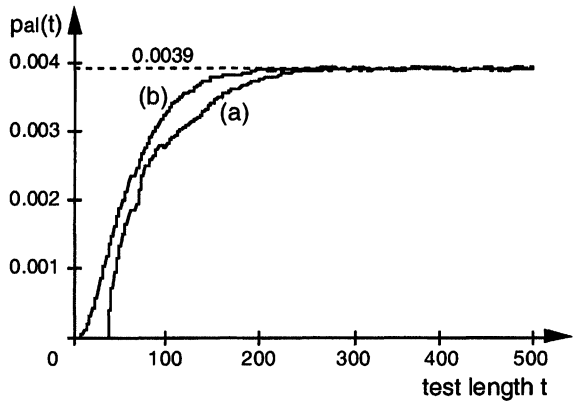

FIGURE 8 Probability of aliasing in the 8-bit MISR, sequential CUT (a) test response sequences with error patterns **0** and $(0,0,1,1,1,0,0,0)^T$ (b) test response sequences with all possible error patterns out of $\{0,1\}^8$.

For comparison, test response sequences of combinational circuits were also considered. Each test response was faulty with probability $1 - p_0 = 0.1$. The nonzero error pattern was always $(0,0,1,1,1,0,0,0)^T$ corresponding to situation (a), or every nonzero error pattern occurred with equal probability corresponding to (b), respectively. With these sequences of statistically independent error vectors, the probability of aliasing in the 8-bit MISR converges faster. For $t \geq 50$ and $t \geq 39$, respectively, $p_{al}(t)$ differs from 2^{-8} by less than 10% (see Fig. 9).

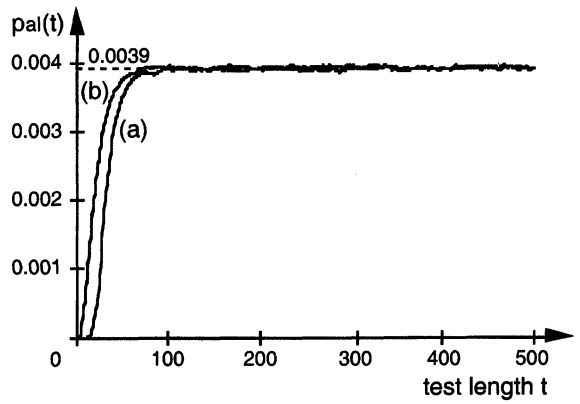

FIGURE 9 Probability of aliasing in the 8-bit MISR, combinational CUT (a) test response sequences with error patterns **0** and $(0,0,1,1,1,0,0,0)^T$ (b) test response sequences with all possible error patterns out of $\{0,1\}^8$.

Many other experiments gave similar results. Independently of the chosen irreducible characteristic polynomial, two observations are made. If the number of different error patterns that occur with nonzero probability is reduced, the probability of aliasing approaches its limiting value more slowly. Convergence is also slower if correlation between successive error vectors is stronger and the number of times at which different error patterns can occur is reduced. In summary, convergence is slower if correlation in time and/or in space is stronger.

7. CONCLUSIONS

If the number of test responses is large, compaction is necessary. In order to choose an appropriate response compactor, to optimize its parameters, and to assess test quality, the portion of faults that do not lead to an erroneous signature must be determined. An efficient way is to employ a probabilistic model of the compaction process and estimate the portion of undetected faults by the probability of aliasing.

This paper has investigated signature analysis for sequential circuits. When test responses of sequential circuits are compacted, strong correlations between errors in successive responses can significantly increase the probability of aliasing. However, the situation is much more favorable if the circuit under test can be set to a fixed state by applying a certain sequence of input vectors. This requirement is met in particular by a large variety of circuits with built-in self-test. For most faults of these circuits, the probability of aliasing in a signature analyzer with an irreducible characteristic polynomial of degree k tends to 2^{-k} as test lengths increase. For some other faults, aliasing does not occur if certain test lengths are avoided. The portion of faults for which these results do not hold has been shown to be extremely small. Experiments have demonstrated that the limiting value can be used as a good approximation of the actual aliasing probability at practical test lengths.

The results are important for advanced BIST techniques with low hardware overhead. Recently developed techniques integrate only a subset of the flip-flops into scan chains and test registers, the subcircuits between the scan chains and test registers contain the remaining flip-flops. Now signature analysis can be applied to these sequential subcircuits in a similar way as to combinational subcircuits.

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APPENDIX

For the proof of Lemma 1 we need an auxiliary lemma:

LEMMA 2 *Consider a sequential circuit with an initial state* $z(0) = z_0$ *for which a synchronizing sequence of length* t_{sync} *exists. If there are two input sequences of equal length* t_0 *leading to the same state,* $z(t_0) = z'(t_0)$, *but different signatures,* $s(t_0) \neq s'(t_0)$, *then for each value* $t \geq t_0 + t_{sync}$ *there are input sequences of length t with* $z(t) = z'(t) = z_0$ *and* $s(t) \neq s'(t)$.

Proof of Lemma 2 Let $\mathbf{d}(0), \mathbf{d}(1), \ldots, \mathbf{d}(t_0 - 1)$ and $\mathbf{d}'(0), \mathbf{d}'(1), \ldots, \mathbf{d}'(t_0 - 1)$ be two input sequences resulting in $\mathbf{z}(t_0) = \mathbf{z}'(t_0)$ and $\mathbf{s}(t_0) \neq \mathbf{s}'(t_0)$. To both sequences we can append $t - t_0 - t_{\text{sync}}$ arbitrary vectors and then the vectors of the synchronizing sequence for state $\mathbf{z_0}$. This gives two input sequences of length t.

Since $\mathbf{d}(i) = \mathbf{d}'(i)$ for $t_0 \leq i < t$ and $\mathbf{z}(t_0) = \mathbf{z}'(t_0)$, we get $\mathbf{z}(i) = \mathbf{z}'(i)$ for $t_0 < i \leq t$ and $\mathbf{e}(i) = \mathbf{e}'(i)$ for $t_0 \leq i < t$. The difference between the two signatures at time t is

$$\begin{aligned}\mathbf{s}(t) \oplus \mathbf{s}'(t) &= \left[C^{t-t_0}\mathbf{s}(t_0) \oplus \bigoplus_{i=0}^{t-t_0-1} C^i \mathbf{e}(t-1-i)\right] \\ &\quad \oplus \left[C^{t-t_0}\mathbf{s}'(t_0) \oplus \bigoplus_{i=0}^{t-t_0-1} C^i \mathbf{e}'(t-1-i)\right] \\ &= C^{t-t_0}\mathbf{s}(t_0) \oplus C^{t-t_0}\mathbf{s}'(t_0) \\ &= C^{t-t_0}[\mathbf{s}(t_0) \oplus \mathbf{s}'(t_0)]\end{aligned}$$

Hence $\mathbf{s}(t_0) \neq \mathbf{s}'(t_0)$ implies $\mathbf{s}(t) \neq \mathbf{s}'(t)$. Q.E.D.

Proof of Lemma 1 We consider a signature analyzer with $k \times k$ feedback matrix C and first assume that the CUT is in state $\mathbf{z_0}$ at time 0. Let $t_{\min}$ be the smallest length for which two input sequences can be found that leave the CUT in state $\mathbf{z_0}$ and cause different signatures, $\mathbf{s}(t_{\min}) \neq \mathbf{s}'(t_{\min})$. Then the smallest number $u \geq t_{\min}$ is chosen that is relatively prime to the lengths of the cycles in the state transition diagram of the signature analyzer operating under constant input $\mathbf{r} = \mathbf{0}$. (This choice

guarantees that the characteristic polynomial of the matrix C^u, $u > 0$, is irreducible [31]). According to Lemma 2, input sequences $\mathbf{d}(0), \ldots, \mathbf{d}(u-1)$ and $\mathbf{d}'(0), \ldots, \mathbf{d}'(u-1)$ exist that lead to the same CUT state $\mathbf{z}(u) = \mathbf{z}'(u) = \mathbf{z_0}$ but result in different signatures. Let the corresponding error vector sequences be

$$\varepsilon = (\mathbf{e}(0), \ldots, \mathbf{e}(u-1)) \quad \text{and}$$
$$\varepsilon' = (\mathbf{e}'(0), \ldots, \mathbf{e}'(u-1))$$

The error vector sequence ε is compacted to the signature $\mathbf{s}_\varepsilon = \mathbf{s}(u)$, the sequence ε' to $\mathbf{s}'_\varepsilon = \mathbf{s}'(u)$, and $\mathbf{s}_\varepsilon \neq \mathbf{s}'_\varepsilon$. The same signatures are obtained if the error vector sequences

$$\tilde{\varepsilon} = (\mathbf{0}, \ldots, \mathbf{0}, \mathbf{s}_\varepsilon) \quad \text{and} \quad \tilde{\varepsilon}' = (\mathbf{0}, \ldots, \mathbf{0}, \mathbf{s}'_\varepsilon)$$

are compacted, which have $u-1$ $\mathbf{0}$-vectors and one last vector that can differ from $\mathbf{0}$.

If the input sequence consists of subsequences of length u that each (applied separately to the CUT with initial state $\mathbf{z_0}$) lead to $\mathbf{s}_\varepsilon$ or $\mathbf{s}'_\varepsilon$ and leave the CUT in state $\mathbf{z_0}$, then the input sequence can be described by numbers α_i in the following way:

$$\alpha_i := \begin{cases} 0 & \text{if the } i\text{-th input subsequence leads to } \mathbf{s}_\varepsilon \\ 1 & \text{if the } i\text{-th input subsequence leads to } \mathbf{s}'_\varepsilon \end{cases}$$

The resulting error vector sequence gives the same signature as the corresponding concatenation of $\tilde{\varepsilon}$ and $\tilde{\varepsilon}'$. For the state of the signature analyzer we get

$$\begin{aligned}
\mathbf{s}(0) &= \mathbf{0} \\
\mathbf{s}(u) &= \mathbf{s}_\varepsilon \oplus \alpha_1 \cdot (\mathbf{s}'_\varepsilon \oplus \mathbf{s}_\varepsilon) \\
\mathbf{s}(2u) &= C^u(\mathbf{s}_\varepsilon \oplus \alpha_1 \cdot (\mathbf{s}'_\varepsilon \oplus \mathbf{s}_\varepsilon)) \\
&\quad \oplus \ \mathbf{s}_\varepsilon \ \oplus \ \alpha_2 \cdot (\mathbf{s}'_\varepsilon \oplus \mathbf{s}_\varepsilon) \\
&\ \ \vdots \\
\mathbf{s}(ku) &= \bigoplus_{i=0}^{k-1} (C^u)^i (\mathbf{s}_\varepsilon \oplus \alpha_{k-i} \cdot (\mathbf{s}'_\varepsilon \oplus \mathbf{s}_\varepsilon))
\end{aligned}$$

$$\begin{aligned}
&= \bigoplus_{i=0}^{k-1} (C^u)^i \mathbf{s}_\varepsilon \oplus \\
&\quad \bigoplus_{i=0}^{k-1} \alpha_{k-i} (C^u)^i (\mathbf{s}'_\varepsilon \oplus \mathbf{s}_\varepsilon) \\
&= \mathbf{s}_* \oplus \bigoplus_{i=0}^{k-1} \alpha_{k-i} (C^u)^i (\mathbf{s}'_\varepsilon \oplus \mathbf{s}_\varepsilon)
\end{aligned}$$

where $\mathbf{s}_*$ denotes the term does not depend on the numbers α_i.

Since the characteristic polynomial of C^u is irreducible and $\mathbf{s}'_\varepsilon \oplus \mathbf{s}_\varepsilon$ differs from $\mathbf{0}$, the sum $\bigoplus_{i=0}^{k-1} \alpha_{k-i} (C^u)^i (\mathbf{s}'_\varepsilon \oplus \mathbf{s}_\varepsilon)$ can assume each value out of $\{0,1\}^k$ if the numbers α_i are chosen appropriately [19]. As all combinations of the numbers α_i occur with nonzero probability, at time $t = k \cdot u$ each state of the signature analyzer can be reached.

Moreover, this argument is independent of the initial state $\mathbf{s}(0)$ of the signature analyzer. So an arbitrary number of additional input vectors followed by a synchronizing sequence can be placed in front of the constructed input sequence. In this way each state of the signature analyzer can be reached for any time $t \geq k \cdot u + t_{\text{sync}}$, and $\pi_j(t) > 0$ holds for all $j \in \{0, 1, \ldots, 2^k - 1\}$ and all $t \geq k \cdot u + t_{\text{sync}}$. Q.E.D.

Author's Biography

Albrecht P. Stroele received the diploma degree in Electrical Engineering from the University of Darmstadt, Germany, and the Dr. rer. nat. degree (Ph. D.) in Computer Science from the University of Karlsruhe, Germany. After several years with Siemens where he was involved in image processing and computer design, he has joined the Institute of Computer Design and Fault Tolerance, University of Karlsruhe. Currently he is a Wissenschaftlicher Assistent and Privatdozent. His research interests include fault modeling, design for testability, built-in self-test techniques, and on-line test. He is a member of IEEE and GI (Gesellschaft fuer Informatik).