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Delay Time Estimation Model for Large Digital CMOS Circuits

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Delay time estimation in simulation or design verification step during a design cycle has become more and more important as the meaning of performance prediction. This paper proposed a delay estimation model for digital CMOS circuits, which works in gate-level but the modeling process includes the characteristics of MOSFETs. This model can handle the variation according to the kind of gates, input transition time, output load(fan-out), and transistor sizes of a gate. The procedure to find the general model was that, a delay model for CMOS inverter was extracted first, then it was extended to other gate by converting it into an equivalent inverter. The resulting model was evaluated and compared with SPICE simulation, which showed that the proposed model has the accuracy of less than 5% relative error rate to the SPICE results for each case and the speed of about 70 times faster than SPICE.

Keywords: Delay time estimation, equivalent inverter model, input signal model, leakage current, MOSFET characteristics, performance prediction

I. INTRODUCTION

Increase in integration ratio has influenced to many areas in design, fabrication, and test. Among them, design verification and performance estimation are the most important steps [1]. Especially for delay time estimation, the previous method in gate-level (each gate is pre-simulated in circuit-level to find the gate delay, which is used to find the total delay in a gate circuit by adding all the gate delays in the critical path [2]) is not sufficiently accurate any more. Meanwhile a circuit-level simulation can be used for delay estimation, but consumes the cost and time very much [3,4].

A special method to find delay time of a given logic gate or circuit has been demanded since 1960's and lots of researches have been performed from the one in [5], although it did not consider the amount of transition time of input signal. Recently, most researches have focused on

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CMOS circuits [3, 4] because it has been dominating other technologies. The principal gate of those methods was the inverter because the structure of a general CMOS gate can be thought as an extension of a CMOS inverter [3, 4, 6, 7].

Researches to find a method calculating delay time easily have been categorized into two groups: look-up table methods [8, 9] and delay time calculation methods [10–17]. A table look-up method has a trade-off between the cost in establishing the table and the accuracy. Also, they don't have enough flexibility for various factors affecting delay time, such as input transition time, fan-out, output capacitance, sizes of MOSFETs, *etc*. The calculation methods are to construct a special delay model and can be divided into two groups: with [10–13] and without [14, 15] the properties of the circuits or MOSFETs. The latter methods considered many factors affecting the delay time but they are not enough for more general cases where the sizes of MOSFETEs, output capacitances, *etc*., are varied. In remodeling methods, RC model could be used for a MOSFET [10] but it could not model exactly enough to include the nonlinear property of MOSFET with linear resistor. In 1990 and 1991, delay models for inverter and other logic gates were modeled with α-power MOSFET model [11, 12], but they considered only the case of very small input transition time, resulting in the decreasing tendency in accuracy as the input transition time increases. This drawback was resolved in [14] by including many presimulation steps.

Recently in [15], similar to [11, 12] but more precise model has been published, which considered the velocity saturation effects and the gate capacitances of MOSFETs. The error rate to SPICE of this model was with 8%. Also in [16], output load was modeled with an RC model and differential equations were solved. This paper insisted within 3.5% of error rate to SPICE without mentioning the calculation speed.

This paper proposes a model for CMOS logic circuits, which can predict the delay time of a given circuit with the accuracy competing the SPICE circuit-level simulation and the speed not much slower than gate-level simulation. This model can handle the variation in transition time of input signal, output capacitance, fan-out, and sizes of MOSFETs. As the procedure to construct a general delay model, an inverter model is first constructed, and then it is extended to other gates by converting them into the equivalent inverters. The resulting model is compared with the SPICE simulation for inverter, NAND, and NOR gates in various situations, to show that the proposed model is very efficient in accuracy and speed.

II. REMODELING MOSFET AND INPUT SIGNAL

First, we remodel the characteristics of MOSFET and input signal to simplify the modeling process.

II.1. MOSFET Characteristics

As well-known, the drain current (I_D) has nonlinear property to the drain-source voltage ($|V_{DS}|$). This characteristics is simplified as shown in Figure 1. In this model, we take the empirical MOSFET SPICE model(MOS3) as the target characteristics and simplify them into piecewise linear characteristics. As shown in this figure, two parameters, I_{DO} and G_{LO} need to be obtained and all other values can be calculated with these two.

G_{LO} represents the conductance in linear region of the simplified model when $|V_{GS}| = V_{DD}$ and can be obtained from a simple simulation or from the equation,

$$G_{LO} = \left[\frac{\partial I_D}{\partial V_{DS}}\right]_{|V_{DS}|\to 0} \tag{1}$$

I_{DO} indicates the saturation current when $|V_{GS}| = V_{DD}$ and is obtained easily from the current equation. The relationship between G_{LO} and I_{DO} is then,

$$I_{DO} = G_{LO} \cdot V_{LS} \tag{2}$$

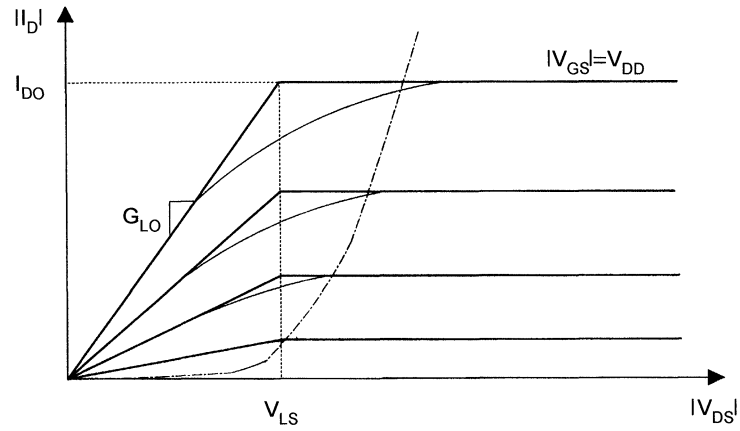


FIGURE 1 Simplified model for MOSFET characteristics.

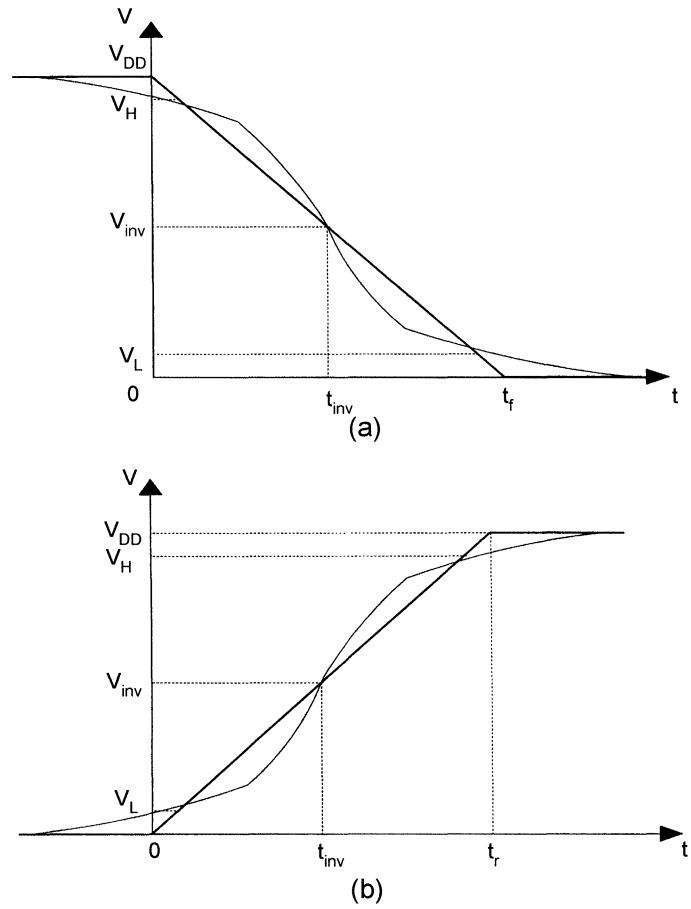


FIGURE 2 Input signal transition models (a) Falling transition, (b) Rising transition.

from which V_{LS} can be obtained. Thus, a given V_{GS}, the saturation current can be expressed as

$$I_D = B(V_{GS} - V_{th})^2 \tag{3}$$

where, $B = I_{DO}/(V_{DD} - V_{th})^2$ is the transconductance factor and V_{th} is the threshold voltage of the MOSFET. The current in linear region can be found only by Eqs. (2), (3), and the linear property.

As shown in Figure 1, this paper assumes that the boundary voltages between saturation and linear regions are the same for all V_{GS}. This is to include the characteristic effect [18–21] when the transistor size becomes smaller by scaling down and is modeled from the empirical data that the boundary voltages have tendency to move to the origin as decreasing the dimension of MOSFETs.

II.2. Input Signals

In general, a signal in a circuit can be thought as an output of the previous gate and it looks as the shallow-lined in Figure 2. This paper linearizes it as the bold-lined such that two points in the signal, $V_H(0.9V_{DD})$ and $V_L(0.1V_{DD})$ are taken, connect them, and extrapolate it to V_{DD} and 0[V]. The signal rising(falling) time is then calculated as the time to transit from 0[V] to V_{DD} (from V_{DD} to 0[V]). In Figure 2, V_{inv} indicates the point of $V_{\text{in}} = V_{\text{out}}$, the logic inversion voltage of a CMOS gate. With this model, the input signal with rising transition is then specified by the following equations. The falling signal can be expressed similarly and is omitted, here.

$$V_{\text{in}}(t) = t \cdot T_r \tag{4}$$

$$T_r = \frac{V_{DD}}{t_r} \tag{4-a}$$

III. DELAY MODEL FOR INVERTER

With the models in Figures 1 and 2, CMOS inverter is first modeled for delay estimation.

III.1. Inverter Operational Modes

From Figure 1, the operational properties in the linear region and saturation region can be easily modeled directly as a resistor and a current source, respectively. The resistance and the supply current are functions of V_{GS} and V_{DS}. Therefore, an inverter in Figure 3(a) can be re-constructed as (b), (c), and (d) according to the operational modes of the two MOSFETs. Here, $I_n(I_p)$ is the saturation current and $R_n(R_p)$ is the resistance in linear mode of nMOSFET(pMOSFET). These values then can be converted into functions of V_{in} and V_{out} as follow.

$$R_n = \begin{bmatrix} R_{LSn} & : & t \le t_{\text{inv}} & \text{or} & V_{\text{in}} \ge V_{\text{inv}} \\ \infty & : & t > t_{\text{inv}} & \text{or} & V_{\text{in}} < V_{\text{inv}} \end{bmatrix} \quad \text{when } V_o \le V_{LSn} \tag{5}$$

$$R_n = \frac{V_{LSn}}{I_{DSn}(V_{\text{inv}})} \tag{5-a}$$

$$I_n = \begin{bmatrix} I_{DSn} & : & t \le \frac{V_{DD} - V_{thn}}{T_f} \\ 0 & : & t > \frac{V_{DD} - V_{thn}}{T_f} \end{bmatrix} \quad \text{when } V_o > V_{LSn} \tag{6}$$

$$I_{DSn} = B_n T_f^2 \left[\frac{V_{DD} - V_{thn}}{T_f} - t \right]^2 \tag{6-a}$$

where, V_{thn} and B_n are the threshold voltage and the transconductance factor of nMOSFET, respectively. I_p and R_p for pMOSFET also can be obtained similarly and are omitted here. With T_f, the above equations indicate the case of input falling, that is, output rising. For rising input, the similar equations can be obtained by replacing T_f with T_r and minor modification, which are also omitted here.

III.2. Relating the Voltages to Times

Calculation of the delay is based on the charging or discharging operation of the load capacitance

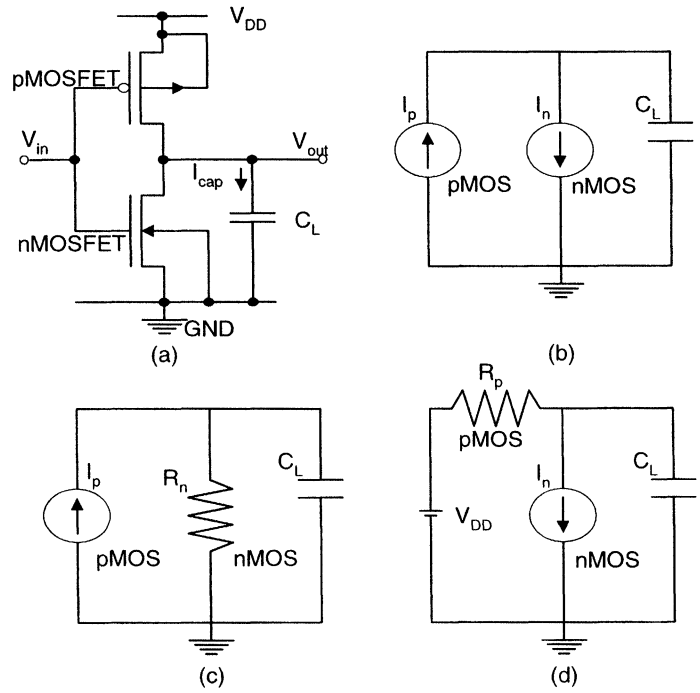


FIGURE 3 Reconstructed CMOS inverter model for delay calculation (a) CMOS inverter, (b) The model for both *p*MOS and *n*MOS in saturation mode, (c) The model for *p*MOS in saturation mode and *n*MOS in linear mode, (d) The model for *p*MOS in linear mode and *n*MOS in saturation mode.

(C_L), which can be expressed with the equation,

$$V_o = \frac{1}{C_L}\int_t I_{\text{cap}}dt \tag{7}$$

where I_{cap} is the current to C_L. In real operation, I_{cap} is not simply the saturation current and should include the current through the resistors of the models in Figure 3. This is known as *leakage current* and is the reason why the previous works showed inaccurate results in large or small input transition time. In this paper, the operation of an inverter in Figure 3 is divided into six phases to handle the leakage current properly. This division was performed by figuring which operational phase the leakage current is dominant in. The resulting operational phases are specified in Table I, which is for the case of falling input. For the case of rising input, similar phases can be obtained and they are omitted here.

In the table, the representative notation ($V_{m1} \sim V_{m6}$) is the output voltage in the corresponding operational phase. For example, the output voltage satisfying the conditions of $V_o \leq V_{LSn}$ and $0 < t \leq t_{\text{inv}}$ (which is equivalent to $V_{\text{inv}} \leq V_{\text{in}} < V_{DD}$) is expressed as V_{m1}. In this phase, *n*MOSFET is in linear region and *p*MOSFET is saturated. Therefore, the model of Figure 3(c) can be used, resulting in

$$V_{m1} = \alpha\left(t_{\text{inv}} - \frac{|V_{thp}|}{T_f}\right)^2 + \beta\left(t_{\text{inv}} - \frac{|V_{thp}|}{T_f}\right) + \gamma - \gamma e^{(t_{\text{inv}} - |V_{thp}|/T_f)/R_{LSn}C_L} \tag{8}$$

$$\alpha = R_{LSn}B_pT_f^2 \tag{8-a}$$

$$\beta = -2R_{LSn}^2C_LB_pT_f^2 \tag{8-b}$$

$$\gamma = 2R_{LSn}^3C_L^2B_pT_f^2 \tag{8-c}$$

For V_{m2}, *n*MOSFET must be in linear region. But in this paper, the leakage current in this phase is neglected that it is expressed as $R_n = \infty$. For V_{m5},

TABLE I Six operational phases and corresponding condition

Rep. notation	Regional condition output, time (input)	MOSFET model *n*-MOS	*p*-MOS
V_{m1}	$V_o \le V_{LSn}$, $0 < t \le t_{\text{inv}}(V_{\text{inv}} \le V_{\text{in}} < V_{DD})$	$R_n = R_{LSn}$	$I_p = I_{DSp}$
V_{m2}	$V_o \le V_{LSn}$, $t_{\text{inv}} < t \le ((V_{DD} - V_{thn})/T_f)(V_{thn} \le V_{\text{in}} < V_{\text{inv}})$	$R_n = \infty$	$I_p = I_{DSp}$
V_{m3}	$V_{LSn} < V_o < (V_{DD} - V_{LSp})$, $(\lvert V_{thp}\rvert/T_f) < t < ((V_{DD} - V_{thn})/t_f)$ $(V_{thn} < V_{\text{in}} \le V_{DD} - \lvert V_{thp}\rvert)$	$I_n = I_{DSn}$	$I_p = I_{DSp}$
V_{m4}	$V_o \ge V_{DD} - V_{LSp}$, $t_{\text{inv}} \le t < ((V_{DD} - V_{thn})/T_f)(V_{thn} < V_{\text{in}} \le V_{\text{inv}})$	$I_n = I_{DSn}$	$R_p = R_{Lop}$
V_{m5}	$V_o \ge V_{DD} - V_{LSp}$, $t \ge ((V_{DD} - V_{thn})/T_f)(V_{\text{in}} \le V_{thn})$	$I_n = 0$	$R_p = R_{LOp}$
V_{m6}	$V_o < V_{DD} - V_{LSp}$, $t \ge ((V_{DD} - V_{thn})/T_f)(V_{\text{in}} \le V_{\text{inv}})$	$I_n = 0$	$I_p = I_{DSp}$

$I_n = 0$ means that *n*MOS is cut-off, while $I_n = 0$ in the case of V_{m6} means that the saturated leakage current is ignored.

For each operational phase in Table I, the output voltage can be calculated by applying the following equations including Eq. (8) for V_{m1},

$$V_{m2} = \frac{B_p T_f^2}{C_L} \int_{t_{\text{inv}}}^{(V_{DD}-V_{thn})/T_f} \left(t - \frac{|V_{thp}|}{T_f}\right)^2 dt \quad (9)$$

$$V_{m3} = \frac{1}{C_L} \int_{t_{LSn}}^{t_f - V_{thn}/T_f} \left\{ B_p T_f^2 \left(t - \frac{|V_{thp}|}{T_f}\right)^2 - B_n T_f^2 \left(\frac{V_{DD} - V_{thn}}{T_f} - t\right)^2 \right\} dt \quad (10)$$

$$V_{m4} = a_2(t - t_{LSp})^2 + a_1(t - t_{LSp}) + a_0 + A e^{(t - t_{LSp})/R_{Lop}C_L} \quad (11)$$

$$a_0 = V_{DD} - B_n T_f^2 R_{Lop}[2R_{Lop}C_L(R_{Lop}C_L + P) + P^2] \quad (11\text{-a})$$

$$a_1 = 2B_n T_f^2 R_{Lop}(R_{Lop}C_L + P) \quad (11\text{-b})$$

$$a_2 = -B_n T_f^2 R_{Lop} \quad (11\text{-c})$$

$$A = V_{DD} - V_{LSp} - a_0 \quad (11\text{-d})$$

$$P = (V_{DD} - V_{thn})/T_f \quad (11\text{-e})$$

$$V_{m5} = V_{DD} - A e^{t/R_{Lop}C_L} \quad (12)$$

$$V_{m6} = \frac{B_p T_f^2}{C_L} \int_{(V_{DD}-V_{thn})/T_f}^{V_{DD}/T_F} \left(t - \frac{|V_{thp}|}{T_f}\right)^2 dt \quad (13)$$

When an input signal changes between 0[V] and V_{DD}, inverter does not always transit through all the six phases. It depends on the relative input transition time which phases the inverter transits through. For example, the phases for V_{m3} and V_{m4} are not included for a very fast input.

III.3. Delay and Transition Time Calculation

With the six phases in Table I, the time for output to transit from 0[V] to $0.5V_{DD}$ (from V_{DD} to $0.5V_{DD}$ for output falling case), $t_{\text{out},0.5V_{DD}}$ is calculated first, then the delay time is calculated as

$$t_d = t_{\text{out},0.5V_{DD}} - \frac{1}{2} t_f \quad (14)$$

for rising output. For falling output, t_f should be replaced with t_r.

IV. EXTENSION TO OTHER GATES

For other CMOS gates than inverter, this paper constructs the models by extending the inverter model such that the parallelly or serially connected MOSFETs are combined into one equivalent MOSFET resulting in the equivalent inverters. In this process the problem occurs when serially

connected MOSFETs are modeled because of the calculational difficulty for the voltage in the connecting nodes. Here, we solve this problem by taking a new saturation current (I_{Do}^{M}) for $|V_{GS}| = V_{DD}$, with which the equivalent conductance (G_{LS}^{M}) is re-calculated by Eq. (2) when N MOSFETs are serially connected, The result is,

$$G_{LS}^{M} = \frac{G_{Lo} \cdot G_{LS}}{G_{Lo} + (N-1)G_{LS}} \tag{15}$$

While, the parallelly connected N MOSFETs are easily modeled by multiplying the drain current by N or reducing the resistance by the factor of $1/N$. It also affects the delay time how many inputs are devoted to drive the gate and which inputs devote to change the output, but the model resulting from the above process has been empirically turned out to handle it quite accurately. Thus, this paper does not include further processing for it.

V. COMPARISON WITH SIMULATION RESULTS

The model proposed above was implemented with C-language and the calculation results were compared with SPICE simulation. The MOSFETs' dimensions used are shown in Table II. SPICE simulation was performed with empirical model(MOS 3).

First, a single stage inverter is compared by varying the input transition time and the output load(fan-out, f_o), which is shown in Figure 4 for output rising and falling cases. In the figure, both the absolute delay values from the model and simulation are shown and the relative error rates of the results by the proposed model to the SPICE results are accompanied. In the figure, f_o means the fanout factor such that $f_o = 2$ means that the output drives two CMOS inverters. As in the figures, the proposed model has the ability to predict the delay time with error rate less than 5% to the SPICE simulation for both the rising and falling cases.

TABLE II The dimensions of MOSFETs used

MOSFET	Gate	Inverter [μm]	NOR [μm]	NAND [μm]
*p*MOSFET	channel length	0.8	0.8	0.8
	channel width	4.0	5.6	4.0
*n*MOSFET	channel length	0.8	0.8	0.8
	channel width	1.6	1.6	1.6

Figure 5 show the comparison results for NAND and NOR gate similiarly to Figure 4, in which the extended model to the NAND or NOR type gate also has the accuracy within 5% of the relative error rate to SPICE. In Figure 5, only the output rising cases are shown, but the falling case would show the similar values.

For the general cases of cascading and signal inputting, the 16 gates are cascaded as Figure 6 for inverter, NAND, or NOR gate. The comparison results for each gate are shown in Figure 7, which also show that the relative error rates are still within 5% to SPICE, regardless of the type of the gate and number of cascaded stages. As in the figure, the relative error rates become smaller as the number of stages increase, by which it can be said that the model proposed is more accurate as the cascaded stages increases. That means, this model is more appropriate to a large circuit.

For more general situation of a gate circuit, 16 stages are cascaded as in Figure 8, where the type of the gate and the output load capacitance in each stage are randomly selected. The load capacitance is between 0.05[pF] and 0.5[pF] representing the arbitrary load capacitance and/or fanout. The comparison results for this circuit are shown in Figure 9 and it also show that the proposed model is accurate enough that the relative error rate to SPICE is less than 5% for the arbitrary output capacitance and the type of gate as well as the arbitrary input transition time. Also, in the case that two or more gates are cascaded, the error rate is within 2% that the proposed

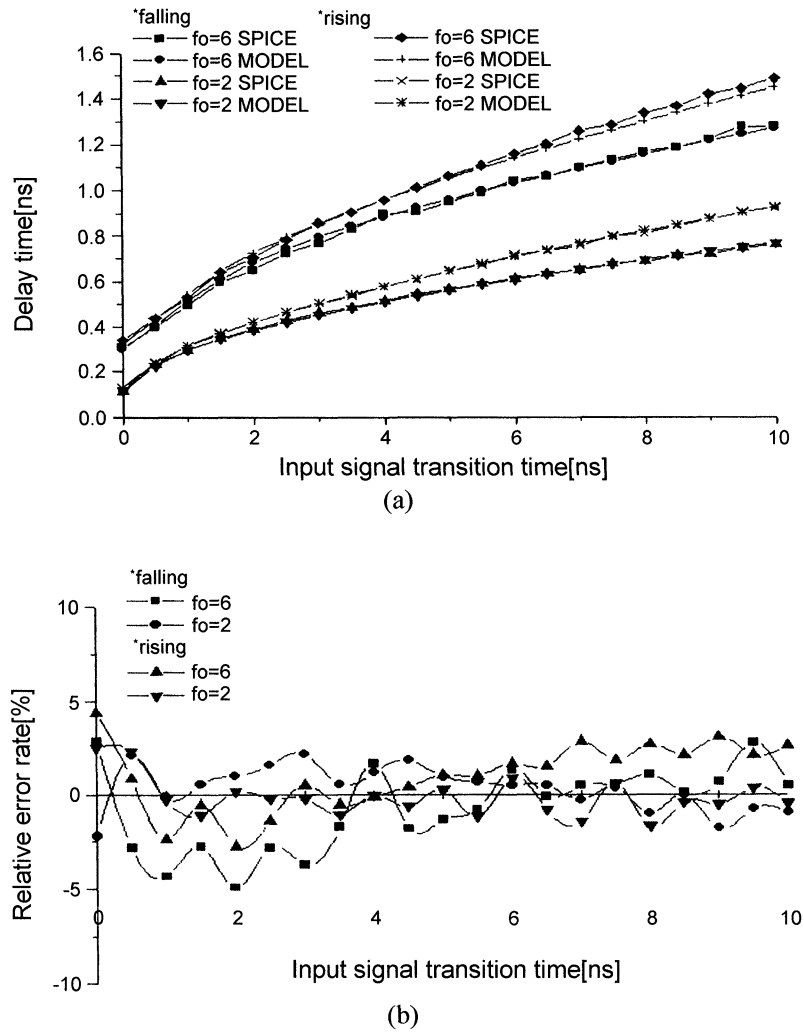
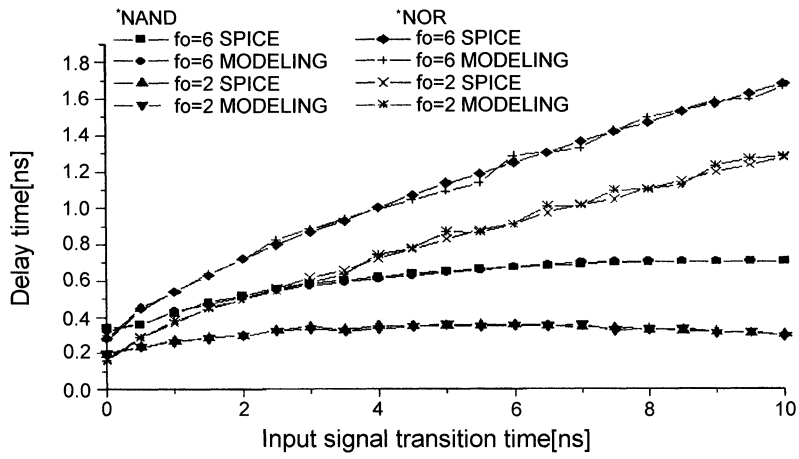


FIGURE 4 Comparison for single stage inverter for output rising and falling cases (a) Comparison of absolute delay times, (b) Relative error rates to the SPICE results.

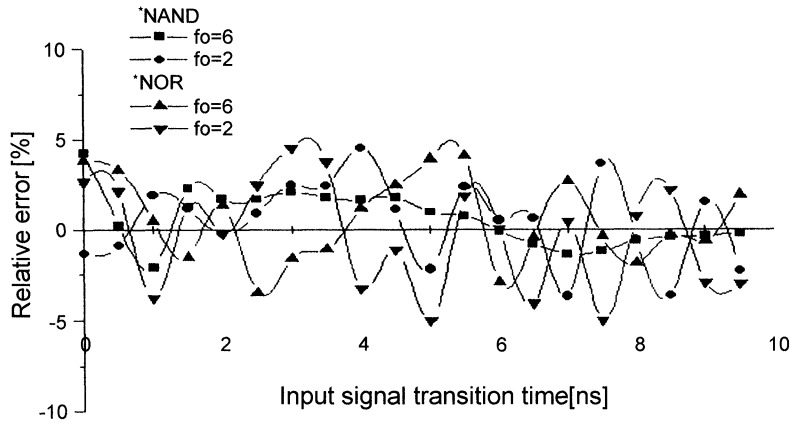
model is more appropriate to the case of cascading several gates than the case of single gate.

In circuit design, the width and length of a MOSFET need to be adjusted for various reasons. Thus, the ability for the proposed model to predict the delay time in a CMOS circuit for the various relative sizes of MOSFETs is examined. As the method, the width and the length of *n*MOS are fixed($W=2\,\mu m$, $L=0.8\,\mu m$), while the width(from $1.0\,\mu m$ to $6\,\mu m$) or the length(from $0.6\,\mu m$ to $3.0\,\mu m$) of *p*MOS is changed. The increasing step is $0.5\,\mu m$ and $0.2\,\mu m$ for the width and the length, respectively. The results are shown in Figure 10, with which it is shown that the proposed model can predict the delay time accurately regardless of the transistor sizes. Here, we include only inverter because other gates are finally converted into the equivalent inverter as explained above.

Finally, we examined the calculation speed by measuring the execution time of the proposed model and run time of SPICE and the results



(a)



(b)

FIGURE 5 Comparison for single stage of NAND and NOR gate (a) Comparison of absolute delay times, (b) Relative error rates to the SPICE results.

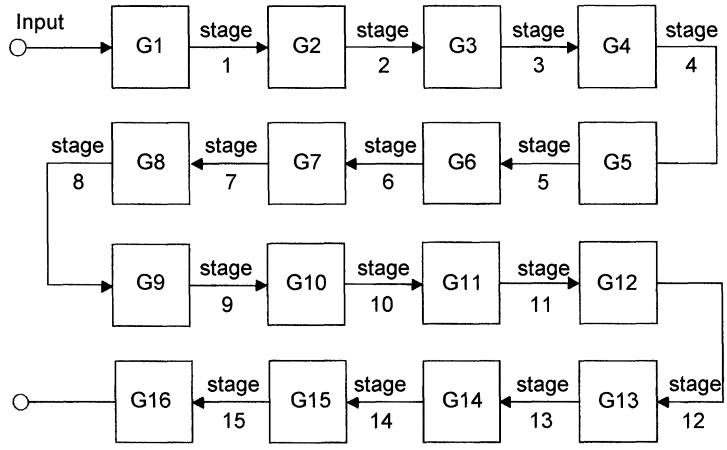


FIGURE 6 16 cascaded stages of CMOS logic gates.

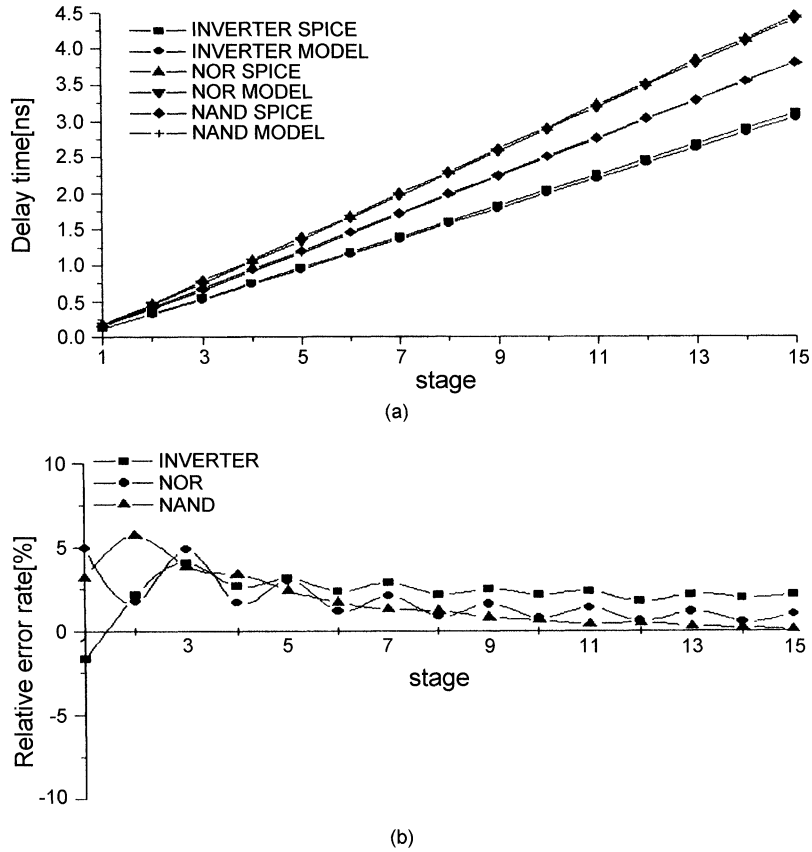


FIGURE 7 Comparison with the circuit of Figure 6 for the various gates (a) Comparison of absolute delay times, (b) Relative error rates to the SPICE results.

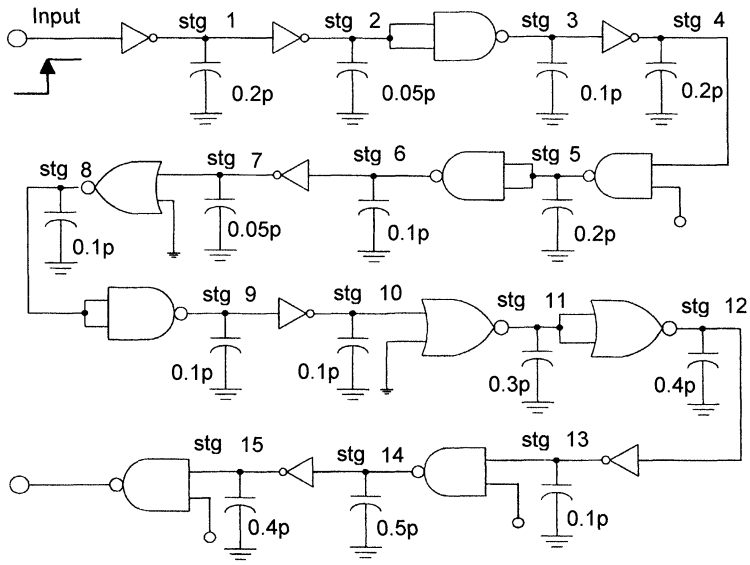


FIGURE 8 Circuit with randomly cascaded inverter, NAND, and NOR gates with randomly selected capacitances.

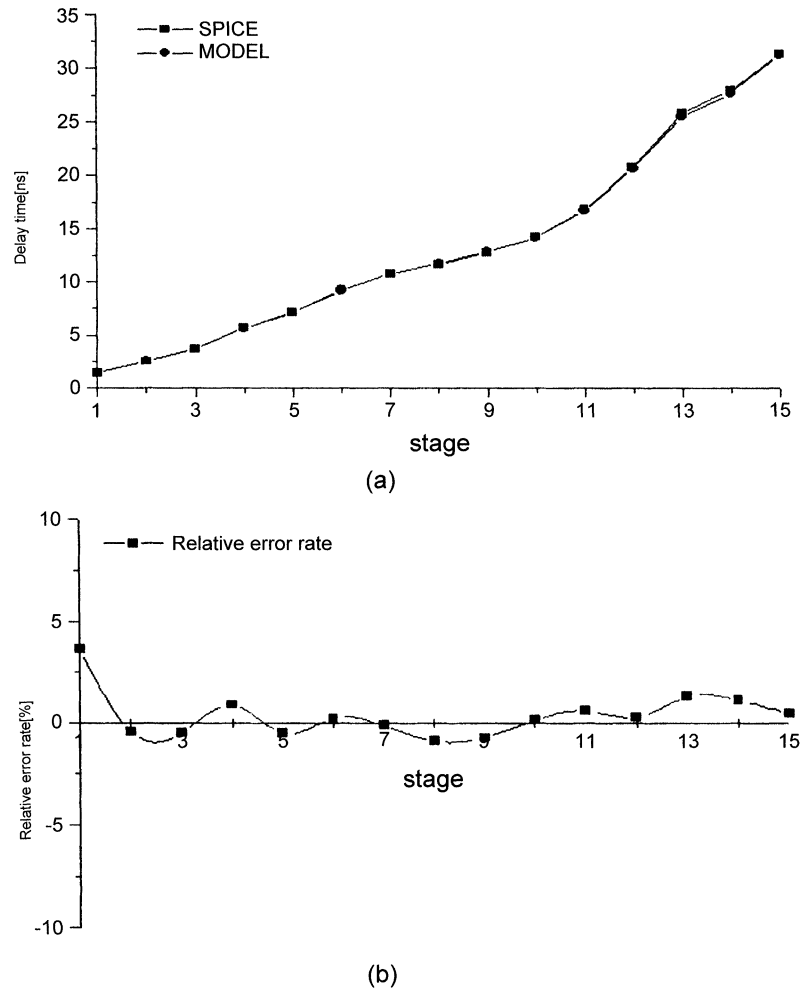


FIGURE 9 Comparison of the circuit in Figure 9 (a) Comparison of absolute delay times, (b) Relative error rates to the SPICE results.

are shown in Figure 11. It can be said by the figure that the proposed model can estimate the delay time of given circuit more than 70 times faster than the SPICE simulation. This speed is not much slower than the gate-level timing calculation.

VI. CONCLUSION

In this paper, a model to calculate delay time for CMOS logic circuits proposed. This model can handle all kinds of CMOS logic gates by converting an arbitrary gate into an equivalent CMOS inverter. It is purely calculational model and need almost no pre-simulation step. The methodology for the proposed model to calculate the delay time of a given circuit is to calculate the output voltages for the appropriate operational phases, relate them to the time, and calculate the delay time.

The proposed model can calculate the delay time regardless of the input transition time, output load(fan-out number), or the sizes of MOSFETs. From the results by comparing the calculated results from the proposed model to those from the SPICE simulation, the proposed model has the accuracy competing the SPICE results such that the relative error rate to SPICE is within 5% and

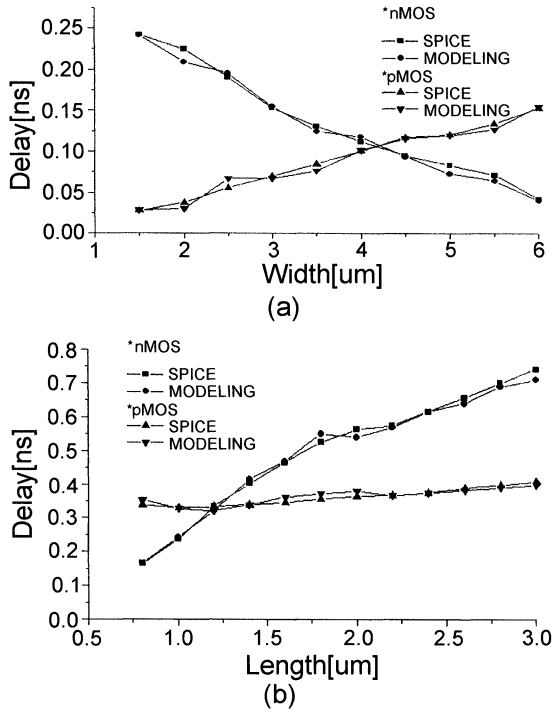


FIGURE 10 Comparison for the variations of the width and the length of the MOSFET (a) variation of the width, (b) variation of the length.

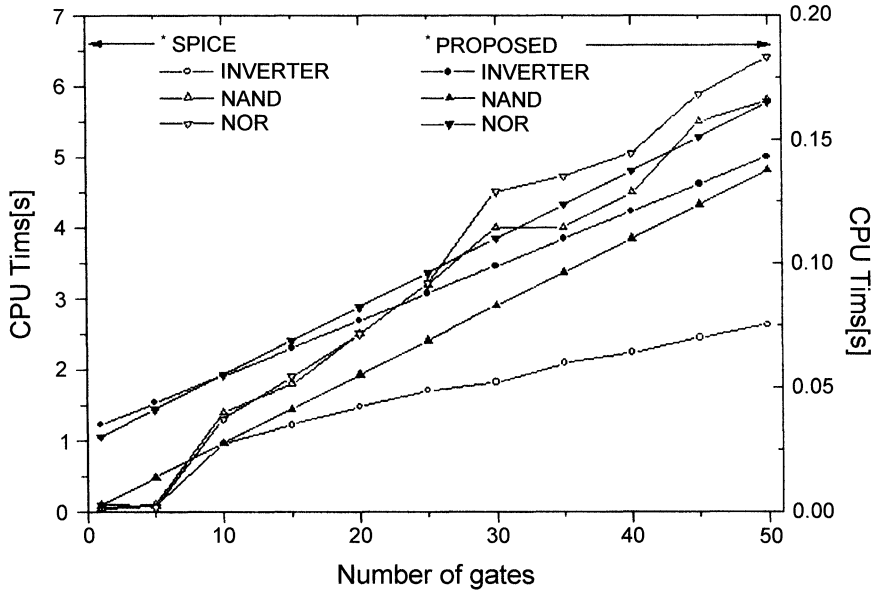


FIGURE 11 Comparison of the speed for inverter, NAND, and NOR gate.

the speed is about 70 time faster than SPICE simulation.

Consequently, the delay model proposed here can be used in the simulation step during the design cycle to predict the delay of a CMOS logic circuit without losing the accuracy of circuit-level simulation and with the speed high enough. This model is especially useful to predict the operational frequency for a large CMOS logic circuit which is usually calculated with the critical path [2] in a given circuit.

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