An Integrated Approach to Data Path Synthesis for Behavioral-level Power Optimization*

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This paper presents an integrated approach to data path synthesis which solves three important design problems: scheduling, allocation, and hardware partitioning with power minimization as a key design objective. Based on the rules of thumbs introduced in prior work on synthesis for low power we derive an integer programming formulation for solving the problems. We then, based on the formulation, develop an efficient algorithm which performs scheduling, allocation and hardware partitioning simultaneously so that the effects of them on power consumption are exploited more fully and effectively. Our experimentation results show that the algorithm is quite effective, producing designs with significant savings in power consumption.

Keywords: Behavioral synthesis; Low-power; VLSI; Scheduling; Allocation; Data path

1. INTRODUCTION

Power consumption in VLSI circuits has become an important consideration in circuit design in recent years [1]. In many application domains, we need to use low-power circuits in order to lower the packaging and cooling costs and to extend the battery life. In designing low-power circuits, a number of techniques for reducing internal power dissipation has been proposed. These techniques often focus on reducing the dominant term in the equation for power dissipation in CMOS digital circuits [1]:

\[ P = C_L V_{DD}^2 f_p \]  

(1)

where \( P \) denotes the power dissipated in charging and discharging the output capacitive load \( C_L \). \( V_{DD} \) is the supply voltage and \( f_p \) is the output switching frequency. One way to reduce power consumption is to lower the total capacitive load \( C_L \). In general, there are different types of


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functional modules which perform the same computation but have different areas, speeds, capacitive loads and power consumptions. Consequently, for power efficient design it is important to make suitable choices among the different types of functional modules available. Another way to reduce power consumption is to reduce $f_p$ by inhibiting unnecessary circuit switching activity. For example, in the design of the PowerPC 603 the clock signal was disabled thereby inhibiting switching during periods of inactivity in the module [2].

Previous research efforts [3–5] in high level synthesis have mostly focused on speed and/or area optimization using a global periodic clock signal and a single type of functional modules for each operation. Much work on power optimization has focused at the logic level. The power trade-off between different types of adders and multipliers was studied in [6]. In [7] power was minimized by modifying the function of each node in the circuit. [8] employed a re-encoding technique using gated clocks for reducing power in sequential circuits. A high-level synthesis system, HYPER-LP, presented in [9] uses a variety of architectural and arithmetic transformations to optimize the power dissipation.

In this paper, based on the observations from the prior work on synthesis for low power [6, 8, 9, 11] we design a new high-level synthesis algorithm which performs the tasks of scheduling, allocation, and hardware partitioning in an integrated fashion for low power design. Specially, for a given unscheduled data flow graph, we are to (1) select functional modules from a given general library (2) schedule the operations on the selected functional modules so that groups of functional modules with similar activity patterns can be deactivated and (3) allocate registers to the variables and partition the registers so that groups of registers can be deactivated. Our objectives are to minimize the total hardware cost as well as power consumption. Our algorithm employs the following techniques to reduce power consumption: functional module selection, selective shutdown of functional modules, and selective shutdown of registers.

### 1.1. Functional Module Selection

In general, an operation can be executed on one of several different types of functional modules which have different execution times, areas and power consumptions. For example, Table I shows that a 32-bit addition operation can be executed on a ripple-carry adder (RCA) in 20 ns which consumes 22.7 mW or on a carry lookahead adder (CLA) in 10 ns which consumes 37.3 mW, and a 32-bit multiplication operation can be executed on a Booth multiplier (BOOTH) in 160 ns which consumes 84.0 mW or on an array multiplier (ARR) in 100 ns which consumes 295.6 mW [10]. To reduce power consumption, utilization of functional modules which consume less power is clearly desirable.

As an example, Figure 1 shows a given unscheduled data flow graph. Suppose the duration of a control step is 120 ns, and to carry out a multiplication operation BOOTH takes 2 control steps and ARR takes 1 control step. Schedule A in Figure 2 shows a schedule when only ARR is available. Schedule B in Figure 3 shows a schedule when both ARR and BOOTH are available. Schedule A uses 2 ARRs and consumes 4138.4 mW. On the other hand, Schedule B uses 1 ARR and 2 BOOTHs, and consumes only 2657.2 mW.

![Figure 1: An example.](image)

<table>
<thead>
<tr>
<th>Table I: Delay and average power of operators</th>
</tr>
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<tbody>
<tr>
<td>Delay (ns)</td>
</tr>
<tr>
<td>-----------</td>
</tr>
<tr>
<td>RCA</td>
</tr>
<tr>
<td>CLA</td>
</tr>
<tr>
<td>BOOTH</td>
</tr>
<tr>
<td>ARR</td>
</tr>
</tbody>
</table>
Consequently, Schedule B yields a 35% saving in power consumption.

1.2. Selective Shutdown of Functional Modules

Recent studies [11] indicate that the clock signal in a digital circuit consumes somewhere between 15% to 45% of the total power. The clock signal is distributed globally to all functional modules and memory modules. However, in most cases, some portions of the circuit are inactive during some control steps (the functional modules are not performing any active computation) and the clock signal is not needed for these functional modules during these control steps. However, since every
module is driven by the clock signal, there will be switching activity even in modules that are not performing any active computation, leading to unnecessary power consumptions in both the clock signal and the modules. In CMOS circuits, a clocked functional module (From now, we assume all functional modules are clocked functional modules.) has registers at its inputs. When the clock signal is on, the contents of the registers are loaded into the functional unit. In other words, if the clock signal is off during time period, there will be no dynamic power consuming activity during that time period [11]. It is therefore desirable that a functional module be driven by a clock signal which is on only during control steps in which the functional module is active.

In order to save power consumption in a clock signal as well as in functional modules, we can regenerate the clock signal so that clock pulses are present only when they are needed. Figure 4 shows a clock regenerator that regenerates the clock signal using a clock gating signal which is designed according to the active/inactive control steps of the functional modules. (An active control step of a functional module is a control step in which the module is performing active computation. Similarly, an inactive control step is one in which the functional module is not performing active computation.) Note that power consumption is reduced both in the functional modules during the inactive control steps and in the clock signal when the corresponding clock pulses are suppressed.

From a power consumption point of view, each functional module should have its own regenerated clock signal. That is, a functional module will be deactivated in all the control steps in which it is not performing any computation. However, in this case, there will be too many distinct clock regenerators and the control logic for clock regenerators will become very complicated. Correspondingly, there also will be too many distinct clock gating signals. Consequently, the clock regenerators and their control logic might become dominant factors of the total power consumption. A more practical approach is to use the same regenerated clock signal for a group of functional modules so that not only will the number of clock regenerators be reduced, but also the control logic for clock gating will not become excessively complicated.

In our approach, we use a regenerated clock signal for each type of functional modules. Figure 5 shows the clock regenerator logic used in our algorithm. Figure 6 shows active and inactive control steps of ARR and BOOTH for Schedule B. With the regenerated clock signals, Schedule B consumes 1222.8 mW on the functional modules and consumes 70% less power than Schedule A does.

FIGURE 4 Clock regenerator.
1.3. Selective Shutdown of Registers

In a dynamic register, information is stored in the form of electric charge which leaks gradually over time. Thus dynamic registers need to be refreshed periodically, usually in each control step.

Consequently, power is consumed in both the refresh circuit and the clock signal. However, data stored in a register might become obsolete, and it is unnecessary to refresh a register after the data stored in the register will no longer be used. Similar to the case of functional modules, by clock gating, we can turn off both the refresh circuit and the clock signal that drives the refresh circuit during control steps in which a register no longer needs to be refreshed.

Again, it is not practical for each register to have its own regenerated clock signal. Consequently, we shall partition the registers into groups and let each group be driven by its own regenerated clock signal.

To partition the registers, we first partition the variables into groups. Each group of variables is
then assigned to the registers to form a group. The partition is to be carried out in such a way that the total number of active control steps in the registers is minimized. (An active control step of a register is a control step in which the register contains the value of a live variable. Similarly, an inactive control step is one in which the register contains data which is obsolete.) Figure 7(a) shows the life times of 9 variables from Schedule B in Figure 3. Figure 7(b) shows three different ways to partition the variables (which are then assigned to registers).

In Partition A, there is only one group of 3 registers. They have only one (common) inactive control step. Thus, the total number of active control steps in the registers is 15. In Partition B, there are 2 groups of registers, P1 and P2. In group P1, there are 2 registers and one (common) inactive control step. In group P2, there are 1 register and 2 (common) inactive control steps. The total number of active control steps in the registers is 14. In Partition C, there are also 2 groups of registers, P1 and P2. In group P1, there

FIGURE 7 Three possible partitioning.
are 2 registers and 2 (common) inactive control steps. In group \( P_2 \), there is 1 register and 4 (common) inactive control steps. The total number of active control steps in the registers is 10. In fact, Partition C achieves a saving of 33% of power consumption in register than using Partition A.

The three techniques mentioned above are closely inter-related. Our algorithm performs the tasks of functional module selection, scheduling, allocation and partitioning simultaneously embodying these techniques. We are given a general library which contains several types of functional modules for each type of operation and the total number of control steps within which all operations in the data flow graph are to be executed. We are to (1) determine an execution schedule for the operations, (2) select the type of functional module for each operation, (3) partition the variables into groups, (4) allocate functional modules and registers and (5) determine the regenerated clock signal for each type of functional modules and each group of registers. The hardware cost, the total power consumption, and the total number of active control steps in functional modules and registers will be minimized. We propose a polynomial time algorithm which is an approximation algorithm for solving an integer programming (IP) problem.

Previous research efforts [3–5] in high level synthesis have mostly focused on speed and/or area optimization using a global periodic clock signal and a single type of functional modules for each operation. In [12, 13] the problem of selecting one type of functional modules for each type of operations from a given library was studied. In [14], the scheduling problem for general libraries was studied, combining both integer linear programming (ILP) and list scheduling techniques. In [11], reduction in power consumption in registers using a partitioning approach was studied.

2. NOTATIONS

Our algorithm accepts as input a VHDL description of a data path. We are given the total number of control steps, \( T \), within which execution is to be scheduled. From the VHDL description, a set of operations and a precedence relation over the operations, \( \prec \), are derived. Let \( \mathcal{O} = \{ op_1, op_2, \ldots, op_N \} \) denote the set of operations. The relation \( op_i \prec op_j \) means that the execution of \( op_i \) must be completed before the commencement of the execution of \( op_j \). A library of functional module types is provided. Each type is specified by its cost, power consumption, execution time, and the set of operations that can be executed on such functional modules. Let \( \mathcal{L} = \{ 1, 2, \ldots, L \} \) denote the library of functional module types. For a type-\( k \) functional module, let \( e_k \) denote its execution time in terms of the number of control steps which is an integer \( \geq 1 \), \( c_k \) its cost, and \( d_k \) the power consumption per control step.

The set of operations that can be executed on a type-\( k \) functional module is denoted \( \mathcal{O}(k) \), i.e., \( \mathcal{O}(k) = \{ op_i | op_i \text{ can be executed on a type-} k \text{ functional module} \} \). For a given operation \( op_i \), let \( \mathcal{U}(op_i) \) denote the set of types of functional modules on which \( op_i \) can be executed, i.e., \( \mathcal{U}(op_i) = \{ k | op_i \text{ can be executed on a type-} k \text{ functional module} \} \). The time frame of an operation \( op_i \), \([ s_i, t_i ] \), indicates the control steps within which the operation is to be executed in order to satisfy the timing constraints (so that execution of all operations will be completed within \( T \) control steps).

Let \( \mathcal{V} = \{ \text{var}_1, \text{var}_2, \ldots, \text{var}_M \} \) denote the set of variables where \( \text{var}_i \) is the output produced by operation \( op_i \). Let \( C(\text{var}_i) \) be the set of operations which have \( \text{var}_i \) as an input, i.e., \( C(\text{var}_i) = \{ op_j | \text{var}_i \text{ is an input to operation } op_j \} \). The value of each variable is stored in a register. We are given the cost of a register, \( c_r \), and the power consumptions per control steps, \( d_r \).

3. PROBLEM FORMULATION

The problem we want to solve is a very complex one. Our major contribution is an efficient approximation algorithm (Section 4) which is
developed from an integer programming (IP) formulation of the scheduling, allocation and partitioning problem. In this section we provide the details of the formulation. For simplicity, we assume that the registers are to be partitioned into two groups. Our formulation can be easily extended to the multiple partitioning.

We introduce first the definitions of several sets of variables. First of all, for each operation \( \text{op}_i \), we have a 0–1 integer variable \( o_{ijkp}, 1 \leq i \leq N, \) \( s_i \leq j \leq t_i - e_k + 1, k \in U(\text{op}_i), p \in \{1, 2\} \).

\[
o_{ijkp} = \begin{cases} 
1 & \text{if \( \text{op}_i \) begins its execution at control step \( j \) on a type-\( k \) functional module and the output variable \( \text{var}_i \) is stored in a register in Group-\( p \) } \\
0 & \text{otherwise}
\end{cases}
\]

Second, for each variable \( \text{var}_i \), we have a 0–1 integer variable \( v_{ijp}, 1 \leq i \leq M, \) \( s_i \leq j \leq t_i, p \in \{1, 2\} \).

\[
v_{ijp} = \begin{cases} 
1 & \text{if \( \text{var}_i \) is alive at control step \( j \) and is stored in a register in Group-\( p \) } \\
0 & \text{otherwise}
\end{cases}
\]

Third, to determine the total number of functional modules of each type, we introduce the integer variables \( f_{kj} \) and \( F_k \), \( 1 \leq k \leq L, 1 \leq j \leq T \). \( f_{kj} \) is the number of type-\( k \) functional modules used in control step \( j \) and \( F_k \) is the total number of type-\( k \) functional modules used throughout all control steps.

Fourth, to determine the total number of registers in each group, we have two sets of integer variables, \( r_{pj} \) and \( R_p \), \( p \in \{1, 2\} \) and \( 1 \leq j \leq T \). \( r_{pj} \) is the number of variables which are alive at control step \( j \) in Group-\( p \). In other words, \( r_{pj} \) is the number of registers needed at control step \( j \) in Group-\( p \). \( R_p \) is the number of registers in Group-\( p \) which is the maximum of \( r_{pj} \) for \( j = 1, \ldots, T \). It should be noted that it is guaranteed that the variables in Group-\( p \) can be assigned to \( R_p \) registers when the left edge algorithm [15] is used since there are at most \( R_p \) variables that are alive in each control step.

Finally, to represent the active/inactive control step of each type of functional modules, we have the 0–1 integer variables, \( a_{kj} \) and \( b_{pj}, 1 \leq k \leq L, p \in \{1, 2\} \).

\[
a_{kj} = \begin{cases} 
1 & \text{if any type-\( k \) functional module is active at control step \( j \) } \\
0 & \text{otherwise}
\end{cases}
\]

Similarly,

\[
b_{pj} = \begin{cases} 
1 & \text{if any register in Group-\( p \) is active at control step \( j \) } \\
0 & \text{otherwise}
\end{cases}
\]

We have the following constraints. First, each operation must be scheduled for execution exactly once. Thus, for each \( i \) (corresponding to operation \( \text{op}_i \), \( 1 \leq i \leq N \), we have

\[
\sum_j \sum_k \sum_p o_{ijkp} = 1 \quad (1)
\]

Second, the precedence relations over the operations are represented as linear constraints. Let

\[
\mathcal{F}(i, j) = \{ o_{ijkp} | s_i \leq j' \leq j - e_k + 1, k \in U(\text{op}_i), p \in \{1, 2\} \}
\]

Thus,

\[
\sum_{o \in \mathcal{F}(i,j)} o = \begin{cases} 
1 & \text{if the execution of \( \text{op}_j \) is completed on or before control step \( j \) } \\
0 & \text{otherwise}
\end{cases}
\]

Similarly, let

\[
\mathcal{I}(i,j) = \{ o_{ijkp} | k \in U(\text{op}_i), p \in \{1, 2\} \}
\]
Thus,
\[ \sum_{o \in \mathcal{I}(i,j)} o = \begin{cases} 1 & \text{if the execution of } op_i \text{ is initiated at control step } j \\ 0 & \text{otherwise} \end{cases} \]

For two operations \( op_a \) and \( op_b \) such that \( op_a < op_b \), we have the following constraints: For each \( j \), \( s_a \leq j \leq t_a - 1 \),
\[ \sum_{o \in \mathcal{F}(a,j)} o \geq \sum_{o' \in \mathcal{I}(b,j+1)} o' \tag{2} \]

which ensures that the execution of \( op_b \) is initiated at control step \( j+1 \) only if the execution of \( op_a \) is finished on or before control step \( j \).

Finally, we have the following set of equations. First, for each variable \( var_i \), we need to determine whether \( var_i \) is alive at control step \( j \) and the group to which \( var_i \) belongs. \( var_i \) is alive at control step \( j \) and is included in Group-\( p \) if operation \( op_i \) completes its execution before control step \( j \) and its output is included in Group-\( p \), and any one of the operations which has \( var_i \) as an input has not been initiated at control step \( j \). For each \( p \in \{1, 2\} \), let
\[ \mathcal{F}_p(i,j) = \{ o_{gkp} \mid s_i \leq j \leq e_k + 1, \quad k \in U(op_i) \} \]

Thus,
\[ \sum_{o \in \mathcal{F}_p(i,j)} o = \begin{cases} 1 & \text{if the execution of } op_i \text{ is completed on or before control step } j \\ \text{and its output variable } var_i \text{ is included in Group-} p \\ 0 & \text{otherwise} \end{cases} \]

\[ \mathcal{I}^+(i,j) = \{ o_{gkp} \mid j \leq s_i \leq t_i, \quad k \in U(op_i), \quad p \in \{1, 2\} \} \]

Thus,
\[ \sum_{o \in \mathcal{I}^+(i,j)} o = \begin{cases} 1 & \text{if the execution of } op_i \text{ is initiated at or after control step } j \\ 0 & \text{otherwise} \end{cases} \]

So we have the following equations:
\[ v_{ijp} = F_p(i,j) \cap \bigcup_{op_n \in C(i)} \mathcal{I}^+(i',j+1) \tag{3} \]

After the determination of values of the variables \( o_{gkp} \) and \( v_{ijp} \), we can compute the values of \( f_{kj} \), \( F_k \), \( r_{pj} \) and \( R_p \) as:
\[ f_{kj} = \sum_{\{i \mid op_i \in O(k)\}} \left( \sum_{j=f-k+1}^{j} x_{ijp} \right) \tag{4} \]
\[ F_k = \max_j f_{kj} \tag{5} \]
\[ r_{pj} = \sum_i v_{ijp} \tag{6} \]
\[ R_p = \max_j r_{pj} \tag{7} \]

Finally, after the values of \( f_{kj} \) and \( r_{pj} \) have been determined, we know the active/inactive control step of each type of functional modules and each group of registers. Therefore the values of \( a_{kj} \) and \( b_{pj} \) can be determined as:
\[ a_{kj} = \begin{cases} 0 & \text{if } f_{kj} = 0 \\ 1 & \text{otherwise} \end{cases} \tag{8} \]
\[ b_{pj} = \begin{cases} 0 & \text{if } r_{pj} = 0 \\ 1 & \text{otherwise} \end{cases} \tag{9} \]

In other word, if any type-\( k \) functional module is used in control step \( j \) (\( f_{kj} \geq 1 \)), all type-\( k \) functional modules will be active at control step \( j \) and \( a_{kj} \) equals to 1. \( b_{pj} \) is computed similarly.

The objective function is
\[ F = \alpha F_{f} + \beta F_{r} \]

where
\[ F_{f} = \gamma \sum_k c_k F_k + \delta \sum_j a_{jk} d_k F_k + \omega \sum_j a_{kj} \]
\[ F_{r} = \gamma \sum_p c_p R_p + \delta \sum_j b_{pj} d_r R_p + \omega \sum_j b_{pj} \]
and \( \alpha, \beta, \gamma, \delta \) and \( \omega \) are weighting factors. \( F_j \) is a weighted sum of hardware cost, power consumption and clock regenerators for the functional modules. Similarly, \( F_r \) is a similar weighted sum for the registers.

4. APPROXIMATION ALGORITHM

This section presents an approximation algorithm for solving the IP problem formulated in Section 3, which yields an approximation solution to the problem of module selection, scheduling, allocation and register partitioning.

In a feasible solution to the ILP, each 0–1 variable \( o_{ijkp} \) will assume the value 0 or 1. In our approximation algorithm, we will determine the values of the 0–1 variables in a step-by-step fashion by examining intermediate solutions in which some of the variables \( o_{ijkp} \) assume non-integral values.

At the beginning, we set the value of one of these variables \( o_{ijkp} \) to 1. Such a choice might lead to the determination of the 0–1 values of other 0–1 variables because of the constraints in (1) and (2).

Let us use the example in Figure 8 to illustrate the idea.

We have the following constraints when the total number of control steps is given to be 5.

Constraints of the form (1):

(1) \( o_{1111} + o_{1112} + o_{1211} + o_{1212} = 1 \)
(2) \( o_{2211} + o_{2212} + o_{2221} + o_{2222} + o_{2311} + o_{2312} + o_{2321} + o_{2322} + o_{2411} + o_{2412} = 1 \)

Constraints of the form (2):

(3) \( o_{3211} + o_{3212} + o_{3221} + o_{3222} + o_{3311} + o_{3312} = 1 \)
(4) \( o_{4311} + o_{4312} + o_{4411} + o_{4412} + o_{4511} + o_{4512} = 1 \)
(5) \( o_{5311} + o_{5312} + o_{5321} + o_{5322} + o_{5411} + o_{5412} = 1 \)
(6) \( o_{6411} + o_{6412} + o_{6511} + o_{6512} = 1 \)

Suppose we set \( o_{1111} \) to 1. Because of constraint (1), we have \( o_{1112} = o_{1121} = o_{1122} = 0 \). On the other hand, suppose we set \( o_{1211} \) to 1. Again, because of constraint (1), we have \( o_{1111} = o_{1112} = o_{1212} = 0 \). Since \( o_{1111} + o_{1112} = 0 \), because of precedence constraints (7) and (8), we have \( o_{2211} = o_{2212} = o_{2221} = o_{2222} = 0 \) and \( o_{3211} = o_{3212} = o_{3221} = o_{3222} = 0 \). Since \( o_{3211} + o_{3212} = 0 \), because of constraint (11), we have \( o_{5311} = o_{5312} = o_{5321} = o_{5322} = 0 \). Since \( o_{5311} + o_{5312} = 0 \), because of constraint (12), we have \( o_{6411} = o_{6412} = 0 \).

On the other hand, suppose we set \( o_{2211} \) to 1. Because of constraint (2), we have \( o_{2212} = o_{2221} = o_{2222} = o_{2311} = o_{2312} = o_{2321} = o_{2322} = o_{2411} = o_{2412} = 0 \). Since \( o_{2211} = 1 \), because of constraint (7), we have \( o_{1111} + o_{1112} = 1 \), and consequently, \( o_{1211} = o_{1212} = 0 \).

After the value of a 0–1 variable is set to 1, and the values of some of the other 0–1 variables are determined according to the constraints (1) and (2), the remaining 0–1 variables \( o_{ijkp} \) are related by

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{type} & \text{hardware cost} & \text{power consumption} & \text{execution time} & \text{operations} \\
\hline
\text{CLA} & 1 & 2 & 4 & 1 + \\
\text{RCA} & 2 & 5 & 1 & 2 + \\
\text{Register} & 10 & 7 & & \\
\hline
\end{array}
\]

FIGURE 8 An example.
the constraints in (1) which are of the form

$$\sum_{j,k} a_{ijk} = 1$$

The variables in the equalities will be assigned equal fractional values. For the example in Figure 8, after setting $a_{1111}$ to 1, we have

$$
\begin{align*}
o_{1112} &= o_{1211} = o_{1212} = 0 \\
o_{2211} &= o_{2212} = o_{2221} = o_{2222} = o_{2311} = \\
o_{2312} &= o_{2321} = o_{2322} = o_{2411} = o_{2412} = 1/10 \\
o_{3211} &= o_{3212} = o_{3221} = o_{3222} = \\
o_{3311} &= o_{3312} = 1/6 \\
o_{4311} &= o_{4312} = o_{4411} = o_{4412} = \\
o_{4511} &= o_{4512} = 1/6 \\
o_{5311} &= o_{5312} = o_{5321} = o_{5322} = \\
o_{5411} &= o_{5412} = 1/6 \\
o_{6411} &= o_{6412} = o_{6511} = o_{6512} = 1/4
\end{align*}
$$

On the other hand, after setting $a_{2121}$ to 1, we have

$$
\begin{align*}
o_{1111} &= o_{1112} = 1/2, \quad o_{1211} = o_{1212} = 0 \\
o_{2212} &= o_{2221} = o_{2222} = \\
o_{2311} &= o_{2312} = o_{2321} = o_{2322} = o_{2411} = o_{2412} = 0 \\
o_{3211} &= o_{3212} = o_{3221} = o_{3222} = \\
o_{3311} &= o_{3312} = 1/6 \\
o_{4311} &= o_{4312} = o_{4411} = o_{4412} = \\
o_{4511} &= o_{4512} = 1/6 \\
o_{5311} &= o_{5312} = o_{5321} = o_{5322} = \\
o_{5411} &= o_{5412} = 1/6 \\
o_{6411} &= o_{6412} = o_{6511} = o_{6512} = 1/4
\end{align*}
$$

After determining the values of the variables $a_{ijk}$, the values of the other variables $f_{jk}, F_j, r_{pj}, R_p, a_{kj}$ and $b_{pj}$ are computed according to the Eqs. in (3) to (9).

We then compute the value of the objective function $F$. For the example in Figure 8, we obtain the values of $F$ corresponding to all possible choices of setting one of the variables $a_{ijk}$ to 1. (The values of the weighting factors in $F$ are chosen to be: when $\alpha=1, \beta=2, \gamma=3, \delta=1$ and $\omega=1$.)

<table>
<thead>
<tr>
<th>Setting</th>
<th>$F$</th>
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<tbody>
<tr>
<td>$a_{1111}=1$</td>
<td>$F=148.92$</td>
</tr>
<tr>
<td>$a_{1112}=1$</td>
<td>$F=148.92$</td>
</tr>
<tr>
<td>$a_{1211}=1$</td>
<td>$F=152.26$</td>
</tr>
<tr>
<td>$a_{1212}=1$</td>
<td>$F=152.26$</td>
</tr>
<tr>
<td>$a_{2211}=1$</td>
<td>$F=175.19$</td>
</tr>
<tr>
<td>$a_{2212}=1$</td>
<td>$F=175.19$</td>
</tr>
<tr>
<td>$a_{5411}=1$</td>
<td>$F=161.72$</td>
</tr>
<tr>
<td>$a_{5412}=1$</td>
<td>$F=161.72$</td>
</tr>
<tr>
<td>$a_{6511}=1$</td>
<td>$F=128.16$</td>
</tr>
<tr>
<td>$a_{6512}=1$</td>
<td>$F=128.16$</td>
</tr>
</tbody>
</table>

On the basis of the value of $F$, the value of one of the variables $a_{ijk}$ will be set to 1. In other words, among all variables $a_{ijk}$, the one that produces the minimum value of $F$ will be set to 1 which together with the values of other variables assigned accordingly constitutes an intermediate solution. For the example in Figure 8, $a_{6511}$ is set to 1. In this case, we obtain an intermediate solution:

$$
\begin{align*}
o_{1111} &= o_{1112} = o_{1211} = o_{1212} = 1/4 \\
o_{2211} &= o_{2212} = o_{2221} = o_{2222} = o_{2311} = o_{2312} = \\
o_{2321} &= o_{2322} = o_{2411} = o_{2412} = 1/10 \\
o_{3211} &= o_{3212} = o_{3221} = o_{3222} = \\
o_{3311} &= o_{3312} = 1/6 \\
o_{4311} &= o_{4312} = o_{4411} = o_{4412} = \\
o_{4511} &= o_{4512} = 1/6 \\
o_{5311} &= o_{5312} = o_{5321} = o_{5322} = \\
o_{5411} &= o_{5412} = 1/6 \\
o_{6411} &= o_{6412} = o_{6511} = o_{6512} = 0
\end{align*}
$$

The step can now be repeated. Among all 0–1 variables that assume non-integral values in the intermediate solution, one of them is set to 1. The
corresponding values of other variables and the value of $F$ are then computed. Finally, a solution is obtained when all $0-1$ variables assume $0-1$ values (and all other variables assume integer values). For the example in Figure 8, we have

$$
\begin{align*}
o_{1111} &= 1, \quad o_{1112} = o_{1211} = o_{1212} = 0 \\
o_{2211} &= 1, \quad o_{2212} = o_{2221} = o_{2222} = o_{2311} = \\
o_{2312} &= o_{2321} = o_{2322} = o_{2411} = o_{2412} = 0 \\
o_{3221} &= 1, \quad o_{3221} = o_{3212} = o_{3222} = \\
o_{3311} &= o_{3312} = 0 \\
o_{4311} &= 1, \quad o_{4312} = o_{4411} = o_{4412} = \\
o_{4511} &= o_{4512} = 0 \\
o_{5411} &= 1, \quad o_{5311} = o_{5312} = o_{5321} = \\
o_{5322} &= o_{5412} = 0 \\
o_{6511} &= 1, \quad o_{6411} = o_{6412} = o_{6512} = 0
\end{align*}
$$

which corresponds to the schedule shown in Figure 9.

A summary of the approximation algorithm is shown below. The algorithm has complexity $O((LTNP)^2)$ in the worst case, where $L$ is the number of types of functional modules in the library, $T$ is the number of control steps, $N$ is the number of operations and $P$ is the number of groups the registers are partitioned into.

Algorithm 1P_solver():

```
repeat
  /* Determine an intermediate solution corresponding to each */
  /* variable $o_{ijkp}$ whose value is not integral */
  for each variable $o_{ijkp}$ whose value is not integral
    • Set $o_{ijkp} = 1$;
    • Compute the values of the other variables according to Eq. (1) to (9);
    • Compute the values of the objective function $F$;
  end for
  • Select the intermediate solution that yields a minimum value of $F$;
until (all variables assume integral values)
```

5. EXPERIMENTAL RESULTS

We tested our program on a number of benchmark examples. Our algorithm described in Section 4 was implemented in C and executed on a Sun Sparc20 workstation. Example df.5 is the differential equation from [3] and the given number of control steps is 5. Example df.7 is the same differential equation example except that the given number of control steps is 7. Examples df2.10 and df2.13 are obtained by unrolling the differential equation example twice and setting the number of control steps to 10 and 13, respectively. Examples ar.8 ar.11 are the AR-Lattice Filter from [16] with the given number of control steps set to 8 and 10, respectively. Examples ewf.18 and ewf.20 are the elliptic wave filter from [16] with the given number of control steps set to 18 and 20, respectively.

Table II summarizes the results produced by our algorithm for the examples df.5, df.7, df2.10, df2.13 ar.8, ar.11 ewf.18 and ewf.20, using the

<table>
<thead>
<tr>
<th>Library lib1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
</tr>
<tr>
<td>------</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>4</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>
library lib1 when $\alpha = 1$, $\beta = 1$, $\gamma = 2$, $\delta = 1$ and $\omega = 1$. The columns rca, cla, booth, and arr give the numbers of functional modules used. The column # of active steps in Functional Modules gives the sum of the numbers of functional modules in each active control step. The columns cost and $P_{fm}$ give the total cost and total power consumption of the functional modules. The columns R1 and R2 give the number of registers in each group after the registers are partitioned into two groups. The column # of active steps in Registers gives the sum of the numbers of registers in each active control step. The columns cost and $P_{reg}$ give the total cost and total power consumption of the registers. The column $F$ gives the value of the objective function $F$. The column time gives the CPU time in seconds.

We also compare the results for different choices of values for the weighting factors in the objective function. The results are summarized in Table III.
TABLE IV Comparison of our algorithm and ILP on df.5

<table>
<thead>
<tr>
<th>Example</th>
<th>Rca</th>
<th>Cla</th>
<th>Booth</th>
<th>Arr</th>
<th># of active steps</th>
<th>Cost</th>
<th>P_{fm}</th>
<th>R1</th>
<th>R2</th>
<th># of active steps</th>
<th>Cost</th>
<th>P_{reg}</th>
<th>F</th>
<th>Time (sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ours</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>13</td>
<td>17</td>
<td>125</td>
<td>2</td>
<td>2</td>
<td>20</td>
<td>40</td>
<td>140</td>
<td>379</td>
<td>2.15</td>
</tr>
<tr>
<td>ILP</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>13</td>
<td>17</td>
<td>125</td>
<td>2</td>
<td>2</td>
<td>20</td>
<td>40</td>
<td>140</td>
<td>379</td>
<td>4208</td>
</tr>
</tbody>
</table>

For the case Hardware (functional modules + registers), we set \( \alpha = 1, \beta = 1, \gamma = 1 \) and \( \delta = \omega = 0 \). Consequently, the result minimizes the cost of the functional modules and registers only and does not take power consumption into consideration. For the case Functional_module_only, we set \( \alpha = 1, \beta = 0, \gamma = 2 \) and \( \delta = \omega = 1 \). Consequently, the result minimizes the cost and power consumption in the functional modules only and does not consider the cost and power consumption in the registers. Similarly, for the case Register_only, we set \( \alpha = 0, \beta = 1, \gamma = 2 \) and \( \delta = \omega = 1 \). Consequently, the result minimizes the cost and power consumption in both functional modules and registers. The column \( P_{fm} \) gives the power consumption in the functional modules and the column \( P_{reg} \) gives the power consumption in the registers. The column \( P_{total} \) gives the total power consumption in the functional modules and the registers. The column \( \text{save} \) shows the percentage reduction in power consumption when compared with the case Hardware. As an illustration, let us examine the results for the example ar.8 closely. If we want to minimize the total hardware cost, we obtain a design which consumes 544 mW in the functional module and 336 mW in the registers. The total hardware cost is 88. If we want to minimize the power consumption in the functional modules only, we obtain a design which consumes only 252 mW in the functional modules but only 252 mW in the registers. The total hardware cost is 88. In Power + Hardware, when we take everything into consideration, we obtain a 42.8% saving in power consumption. The hardware cost is 57.

In order to compare the result produced by our approximation algorithm with the optimal result, we should solve the IP in Section 3. However, since the formulation is cast as a non-linear integer programming problem, the computational effort will be substantial even for small problem instances. Hence, we first generate an integer linear programming (ILP) formulation from the integer programming (IP) formulations in Section 3. Since the objective function \( F \) is a quadratic function, we approximate it by a linear form using La Grange first order conditions. We then used the LINDO package on an IBM3081 to solve the ILP problem. Table IV shows a comparison of the results of example df.5 produced by our algorithm and by ILP. For df.5, ours produced the same results as LINDO did and took much less time, 2.15 vs. 4208 seconds. It should be noted that we can only test example df.5 since the ILP formulation for the other examples are too big and LINDO was not able to generate any solution.

6. CONCLUSIONS

We presented an integrated approach to the problem of solving scheduling, allocation and hardware partitioning with the power consumption as one of key design objectives. We first
proposed an integer programming formulation for solving the problem, from which we derived an efficient approximation algorithm. Unlike previous approaches for low power in which scheduling and allocation are performed independently, our approach combined scheduling, allocation and partitioning together to exploit the effects of them on power consumption more effectively. The experimental results confirmed that our algorithm is quite effective and robust.

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References


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