

Scaling of pHEMTs to Decanano Dimensions

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The effect of scaling into deep decanano dimensions on the performance of pseudomorphic high electron mobility transistors (pHEMTs) is extensively studied using Monte Carlo simulations. The scaling of devices with gate lengths of 120, 70, 50 and 30 nm is performed in both lateral and vertical directions. The devices exhibit a significant improvement in transconductance during scaling, even though external resistances become a limiting factor.

Keywords: pHEMT; Monte Carlo simulation; Scaling; Roadmap; Transconductance

1. INTRODUCTION

Pseudomorphic high electron mobility transistors (pHEMTs) with low indium content channels and channel lengths 0.25–0.15 μm are today the workhorse of the MMIC industry [1]. However, there is potential for enhancing their performance by proper scaling to decanano dimensions. The aim is very realistic since suitable approaches (electron beam lithography, dry etching and δ-doping techniques) exist within III-V technology for controlling the critical atomistic limits. Up to now, this technology has been somewhat ahead of silicon in lithographic resolution and engineering of active layers. However, with MOSFET approaching 0.1 μm [2] there are new incentives for exploring the pHEMT scaling. The GaAs technology has a lot of advantages although the research in ultrafast compound FET's is focused mainly on high In channel devices on InP substrates and

strain relief buffers [3, 4]. The GaAs substrate is still much cheaper, more manufacturable and has a large accessible scale of strain in comparison with the InP substrate.

We extensively study the potential performance of the pHEMTs when such devices are scaled into deep decanano dimensions [5]. We have considered a set of pHEMTs fully scaled in both lateral and vertical directions in proportion to gate lengths of 120, 70, 50, and 30 nm. This is the first phase of a large experimental programme in Glasgow aiming to establish Roadmap benchmarks for high-speed III-V devices.

2. THE FINITE ELEMENT MONTE CARLO SIMULATOR

The finite element Monte Carlo device simulator (MC/H2F) has been developed [6] to investigate

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electron transport properties in compound FETs. The simulator uses quadrilateral elements to depict a complex geometry of the pHEMTs and accurately calculates electrostatic effects caused by the gate and recess geometry as well as the surface potential pinning. It is capable of precisely reproducing a T-shape gate and recess formation in the device [7]. The Monte Carlo module includes electron scattering with polar optical phonons; inter- and intra-valley non-polar optical phonons; acoustic phonons; and ionized and neutral impurity scattering. In addition, alloy scattering and strain effects [8] are considered in the InGaAs channel of the pHEMT.

The electron scattering rate caused by an alloy potential is calculated using the following formula:

$$\Gamma(E) = \frac{3\pi m^{3/2}}{32\sqrt{2}\hbar^4} a^3 x(1-x)\mathcal{D}_{\text{alloy}}^2 d \sqrt{E(1+\alpha E)}(1+2\alpha E)G(E,E), \quad (1)$$

where x is the content of the second minor material, a is the material lattice constant, d is the degree of disorder (the order is perfect for $d=0$ and a maximum disorder goes with $d=1$) and $\mathcal{D}_{\text{alloy}}$ is the alloy scattering potential [10] which is in very good agreement with experimental data, and $d=1$ since the InGaAs channel is 10 nm thick. The ionized impurity scattering rate is calculated using the Ridley model which includes third-body exclusion [11]. We have used a direct technique to generate a final state of the electron after the ionized impurity scattering [12].

Following [13], all scattering rates and generation of final states are modified with a form factor G (the overlap integral) given by

$$G(E, E') = \frac{(1+\alpha E)(1+\alpha' E') + (1/3)\alpha E \alpha' E'}{(1+2\alpha E)(1+2\alpha' E')}. \quad (2)$$

It is assumed in the above equation that an electron with an initial energy E scatters with a final energy E' and that α and α' are the

non-parabolicity parameters for the electron in initial and final bands, respectively. The non-parabolic energy dispersion is used to represent the band structure and calculate the scattering rates.

The introduction of the above features in the analytical band model for III-V materials allows us to extend the regime up to an electric field of 300 kV/cm over which we can confidently predict electron transport properties. Bulk simulations of the drift velocity as a function of the applied electric field have shown that the introduction of the form factor (2) into the scattering rates can substantially improve agreement with experimental data as well as with full band simulations [14]. The inclusion of the alloy scattering mechanism decreases the electron drift velocity at low electric field in bulk simulation of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. It also plays an important role at very high electric field by significantly decreasing the drift velocity. Even with these improvements the analytical band model is expected to break down at very high electric fields ($> 300-400$ kV/cm) and therefore full band models have to be used. We calibrate our simulations against measured I-V characteristics of 120 nm pHEMTs with a maximum drain voltage of 2 V. In such conditions the maximum energy gained by electrons rarely exceeds 1.0 eV. Therefore, we are able to neglect all effects caused by possible impact ionization as well as the hole transport and additional electrostatic effects induced by holes [1].

3. EFFECT OF SCALING ON pHEMT PERFORMANCE

The whole scaling investigation is based on careful calibration of the MC simulations against the 120 nm gate length pHEMT as designed and fabricated by the Nanoelectronics Research Centre at the University of Glasgow. The structure of the devices is schematically drawn in Figure 1. It has a T-shaped gate [15]; a 30 nm heavily Si-doped $2 \times 10^{18} \text{ cm}^{-3}$ n+GaAs cap layer; an $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ etchstop layer; a $7 \times 10^{12} \text{ cm}^{-2}$ Si delta doped

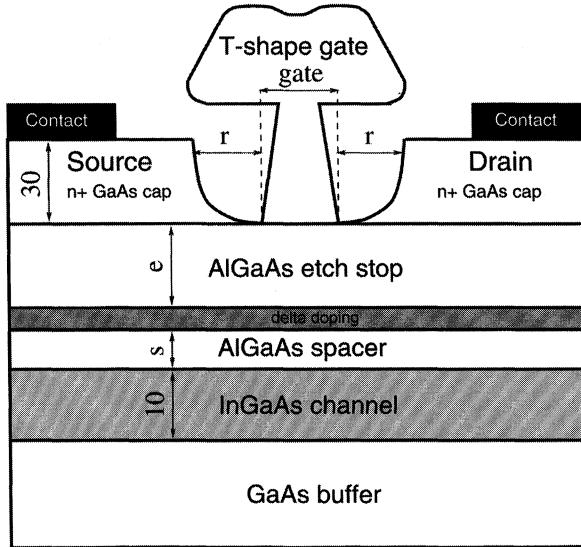


FIGURE 1 The cross-section of the simulated pHEMT. All quoted dimensions are in nm and remain unchanged in the scaling process. The distances given by letters (r =recess, e =etchstop and s =spacer) have been scaled according to Table I.

layer on top of an $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ spacer layer and, finally, an InGaAs channel with indium content $x=0.2$. The whole device structure is grown on top of a 50-nm GaAs buffer. The simulated I-V characteristics, obtained directly from device simulator MC/H2F, represent the typical behaviour of the intrinsic device. To compare this with experimental data the contact resistances of the source and drain are included in the I-V curves at a post-processing stage. The final I-V characteristics (open symbols in Fig. 2) for gate voltages from -1.0 V to 0.4 V are in good agreement with the experimental data (full symbols in Fig. 2). The external resistances of the source and drain, which have been used to remap the intrinsic I-V characteristics according the procedure described in Ref. [16], are 5.22Ω and 0.6Ω , respectively. The result for an intrinsic device is also shown by the dashed line for a gate voltage of 0.4 V only for comparison.

All lateral dimensions have been scaled proportionally to the respective gate length while, in the vertical dimension, the etchstop and spacer have

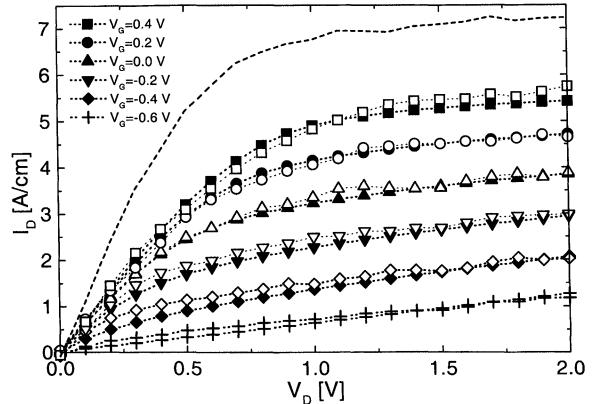


FIGURE 2 I-V characteristic (drain current *versus* drain voltage) of the calibrated pHEMT with a gate length of 120 nm. Full symbols represent experimental data for several fixed gate voltages. Open symbols represent MC simulations when external resistances of the drain and source are included. The I-V characteristic for an intrinsic device (dashed line) is shown for comparison at a gate voltage of 0.4 V .

been scaled with respect to technologically achievable dimensions. Thickness of the etchstop and space layers and the extent of the recess considered in the scaling process are given in Table I. A rapid increase of the average channel velocity for the scaled pHEMTs can be observed in Figure 3 for gate lengths scaled from 120 nm to 70 nm. This improvement in channel velocity saturates with the further scaling of the devices to 50 and to 30 nm. The continued device improvements below the 70 nm velocity cut-off results solely from the reduction of the channel length and the decrease in the source-drain separation. The drain current and transconductance are plotted in Figure 4 as a function of the gate voltage for intrinsic devices for a drain voltage of 1.5 V . The intrinsic transconductance increases steadily during the scaling process, despite an almost constant channel

TABLE I Dimensions used in the scaling process as referred to in Figure 1

Dimension of	Gate length [nm]			
	120	70	50	30
Recess (r) [nm]	50	29	21	13
Etchstop (e) [nm]	18	10	7	5
Spacer (s) [nm]	7	5	4	2

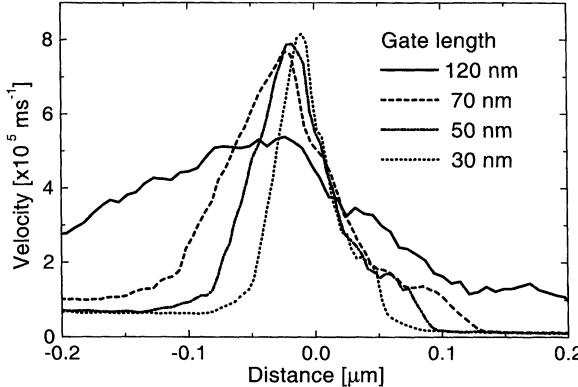


FIGURE 3 Average velocity along the InGaAs channel of the scaled pHEMTs for drain bias of 1.5 V and gate bias of 0.0 V.

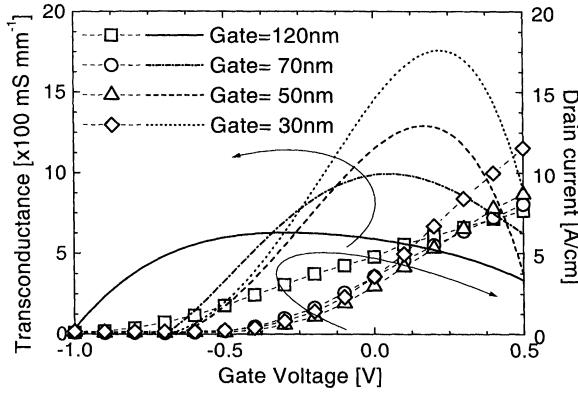


FIGURE 4 Scaled pHEMTs transconductance and drain current *versus* gate voltage for intrinsic devices.

velocity, when the gate length is shrunk below 70 nm. This means that with a proportional scaling from 120 nm to 30 nm (which includes the gate recess), the gate-fringing effect should have no significant influence on the performance of the pHEMTs. We should point out that when the device gate length decreases to deep decanano dimensions, it becomes comparable to the inelastic mean-free path of the carriers. Hence, electrons travelling through the gate region have a high probability to pass through this region without suffering any collisions. However, the reduction of the gate to channel separation below 10 nm may require inclusion of the effect of electron tunneling between the gate and channel in the simulations.

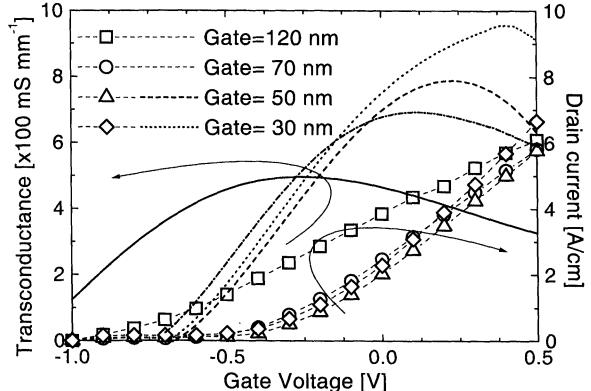


FIGURE 5 Scaled pHEMTs transconductance and drain current *versus* gate voltage with the inclusion of external resistances.

Figure 5 illustrates the effect of the external contact resistance on the device performance, assuming that the value of these resistances remains unchanged in the scaling process. Influence of the external resistances on the device performance (both on the drain current and the transconductance) becomes increasingly important with the reduction of the device dimensions. We expect that the problems related to the handling of external resistances will be one of the main issues for further technological improvement.

4. CONCLUSIONS

We have performed a Monte Carlo study of the pHEMTs' performance with low indium content when these devices are scaled into the deep decanano dimensions. We have not incorporated the phenomena of electron-electron (e-e) interactions into the Monte Carlo module. The e-e interactions are a fast process, responsible for a thermalization of electrons. Therefore, it should be considered only in regions with very high electron density. pHEMTs with the structure shown in Figure 1 have two regions of high electron density: the heavily doped cap where changes in electron density have no influence on the drain current, and the delta-doped layer where the e-e interaction

may reduce the induction of electrons into the channel. The latter is partially compensated by considering a lower, effective delta-doping concentration. Based on the careful calibration of the pHEMT with 120-nm gate length, we have found a continuous improvement in the intrinsic device performance with the proportional scaling. If we wish to take an advantage of the performance potential of the intrinsic device then its contact resistances need to be reduced as much as possible.

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