Guest Editorial

SUNIL R. DAS

*School of Information Technology and Engineering, University of Ottawa, 770 King Edward Avenue, CBY A-608,
Ottawa, Ontario, Canada K1N 6N5*

(Received 15 August 1999; In final form 11 September 2000)

With increasing complexity in systems design with increased levels of integration densities in digital design, better and more effective methods of testing to ensure reliable operations of chips, mainstay of today's many sophisticated systems, are required. The concept of testing has a broad applicability, and finding highly efficient testing techniques that ensure correct systems performance has thus assumed significant importance. The unprecedented response to our Call for Papers for this Special Issue on VLSI Testing from various parts of the globe is brilliant testimony to the profound interest and increased activities of the researchers, engineers and scientists in this important arena.

All the selected papers in this special issue of **VLSI Design** are from those who are established authorities in the field of fault-tolerance and test generation in digital circuits including very large scale integrated circuits or VLSI circuits. Our first paper in this issue is by Jone, Huang, Chang and Das and considers an important area of activity in the discipline-defect level estimation for pseudorandom testing using stochastic analysis. Pseudorandom testing has been widely used in built-in self-testing of VLSI circuits, and the defect level estimation for pseudorandom testing has also been performed using sequential statistical analysis, though it proved to be of limited application because of combinatorial enumerations involved. The authors in the current work instead have used Markov modeling to describe pseudorandom test behaviors and derived a closed form of the defect level equation for the first time by solving the differential equations derived from the Markov model. The Markov model is also extended to consider *all* single stuck-line faults rather than the *worst* single stuck-at faults. A closed form of the defect level equation is successfully derived that takes into consideration all single stuck-line faults. The defect level equation clearly describes relationships among defect level, fabrication yield, number of input combinations, circuit detectability in terms of the worst single stuck-line faults and pseudorandom test length. Although the discussions in the paper primarily pertain to single stuck-at faults, it is not difficult to extend the results to include other fault types.

The second paper by Chandra, Chakrabarty and Hansen presents methods for test set encoding and pattern decompression for core-based systems. The proposed methods are based on the use of twisted-ring counters and offer important advantages like significant test compression, less tester memory, reduced test time and ability to use slower tester, without any performance degradation for the core under test. As shown by the authors, the encoded test sets obtained from partially specified test sets are often smaller

than the compacted test sets generated by automatic test pattern generation programs. Experimental results with ISCAS benchmark circuits demonstrate that the test architecture as suggested offers an attractive solution to the problem of achieving high test quality and low test time with relatively slower, less expensive testers.

The next paper in the issue by Savir describes an efficient method based on fault simulation of solving diagnostic problems created due to the presence of embedded memories in BIST designs. The author's basic concept is to first create an event table for the memory by good-machine simulation of the circuitry driving the memory address and control lines; the event table is then rearranged to form a simulation event table which couples each memory write operation to a particular address with subsequent read operations on that address. Each line of the simulation event table can be considered as a memory write-through operation in which the memory Prelogic is essentially coupled directly to the memory Postlogic. Simulation of the memory-removed structure by the simulation event table can then identify the failing circuit. Special techniques are also described to address faults in the logic embedding the memory control or address inputs. It is, however, presumed that the memory has been tested previously using ATPG techniques through the corresponding inputs, and thus has been found to be fault-free. The paper also analyzes the bottlenecks associated with an efficient BIST diagnostic scheme, suggests ways to overcome them, and provides experimental results to support the conclusions.

Liu, Sathe and Mourad in their paper investigate the effects of reverse body bias on current testing of 0.18 μm gates. Using SPICE simulation, the authors explore the role of reverse body bias on off-state leakage of scaled CMOS devices along with I_{DDQ} of typical CMOS circuit cells. It was shown that reverse body bias can effectively reduce defect-free I_{DDQ} of typical 0.18 μm technology devices and logic gates, while the faulty current is not that much reduced. Further investigation showed that reverse body bias also made the defect-free I_{DDQ} less sensitive to the input state, and thus a single I_{DDQ} current threshold might still be used for testing of 0.18 μm CMOS circuits. There might exist an optimal reverse body bias that minimizes the defect-free I_{DDQ} current, authors conclude, and this bias decreases as the temperature goes down, varying from circuit to circuit, process to process and technology to technology.

The next paper in the series is by Savir again and it considers modification issues of test generators to handle CMOS designs. CMOS designs possess some unique properties that prevent existing test generators from computing test vectors for faults whenever they exist. The basic premise that it is necessary to set a line to logic 0(1) in order to detect a stuck-at 1(0) fault and then propagate the error information to an observable output is not a necessary and sufficient detection condition in the said context. This is due to the existence of unknown logic states in the circuit. The paper illustrates the problem with example and discusses means to rectify it, besides proposing possible enhancements to existing test generation algorithms and outlining the risks in the event no correction steps are undertaken.

Lala and Walker in their paper propose a logic cell that can be used as a building block for self-checking FPGAs. The logic cell proposed is comprised of two 2-to-1 multiplexers, three 4-to-1 multiplexers and a D flip-flop, and has been designed using differential cascade voltage switch logic. It is self-checking for all single transistor stuck-on and stuck-off faults as well as for stuck-at faults at the inputs of multiplexers and D flip-flop. The multiplexers and D flip-flop provide either correct or complementary outputs in the absence of the above faults, the outputs being identical otherwise.

The paper by Chang, Chen, Cheng, Jone and Das then considers the problem of enhancing random pattern testability by circuit restructuring, called *circuit rewiring*. Generally, there exist random-pattern resistant faults in circuits that result in poor fault coverage in built-in self-test methodologies. The basic idea explored in the paper deals with circuit rewiring which is replacing a circuit wire by another wire keeping the functionality unchanged. For two types of rewiring – fanin rewiring and fanout rewiring – the authors analyze the testability change for each type of wire replacement. Based on the

analysis, an efficient algorithm is next developed to enhance circuit testability. For a poor observability node, the authors endeavor to increase observability by adding additional fanout to the node, with removal of alternative wire whose source node has relatively good observability. The proposed technique does not introduce hardware overhead and performance degradation, since a wire addition is followed immediately by a wire removal. Thus the approach is basically cost neutral when compared to other testability enhancement techniques.

Varaprasad, Patnaik, Jamadagni and Agrawal consider cost-effective test pattern generation for on-chip BIST. The authors' methodology is based on the use of suitable linear feedback shift register (LFSR) which cycles through the required test vectors aiming at a desired fault coverage with minimum circuit toggling and hence low power consumption during testing. The proposed technique uses circuit simulation data for modeling, and the authors use graph theoretic techniques to identify the LFSR and compute its characteristic polynomial for realization of test pattern generator.

The final paper in the issue is also by Savir, where, expanding upon past work, the author discusses the problem in testing of logic surrounding embedded memories. The author assumes in the paper that the logic surrounding the memory is functionally partitioned and that the different partitions are logically isolated from one another. The author's flexible design rule allows feedforward connections between the datapath Prelogic and Postlogic. The techniques described in the paper are intended to be used in conjunction with the cutting algorithm for testability measurement in built-in self-test (BIST) designs and may also be suitable for use with other detection probability and simulation tools.

In concluding this guest editorial, I would like to express my sincerest gratitude to all those who helped make this special issue a reality. First and foremost amongst all is Professor George W. Zobrist, Editor-in-Chief of this Journal, who has been a continuing source of encouragement, advice and guidance. His immense help and valued suggestion came whenever and in whatever form they were solicited. Without him, this Special Issue on VLSI Testing would never have been realized.

I would also like to specially acknowledge the contributions of Professor Wen Ben Jone, New Mexico Tech; Professor Krishnendu Chakrabarty, Duke University; Professor Jacob Savir, New Jersey Institute of Technology; Professor Samiha Mourad, Santa Clara University; Professor Parag K. Lala, University of Arkansas; Professor Lalit M. Patnaik, Indian Institute of Science and my colleague, Professor Emil M. Petriu, Director, School of Information Technology and Engineering, University of Ottawa, Ottawa, Ontario, Canada. My thanks are also due to those people behind the scenes – those anonymous reviewers – whose selfless, dedicated and timely professional help contributed to the superb quality of this special issue.

Finally, my special thanks are due to all of my colleagues including many staff members, and to my graduate students, Mr Mansour H. Assaf, Mr Made Sudarma and Miss Jingyi Liang at the School of Information Technology and Engineering, University of Ottawa who provided me the moral and material support needed during the days the special issue was being planned and prepared.