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Timing Challenges for Very Deep Sub-Micron (VDSM) IC

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Many IC design houses failed to be market leaders because they miss the market window due to timing closure problems. Compared to half-micron designs, the amount of time spent on timing verification has greatly increased. Cell delays can be accurately estimated during logic synthesis. However, interconnect delays are unknown until the wire geometry is defined in physical design. Logic synthesis using the cell library models for interconnect delay estimates may be statistically accurate, but can not predict the delay of individual nets accurately. Delay estimates for individual nets (global nets, long wires, large fan-outs, buses), which matter most for the critical paths can be inaccurate and cause a design failure. Inaccurate timing verification causes silicon failure in shipped products that results in the loss of millions of dollars spent designing a high-performance product and potentially larger costs due to lost market share. Full-chip, sign-off verification with silicon-accuracy will allow these problems to be discovered and fixed before tape-out.

Keywords: Very deep sub-micron; Timing verification; Static timing analysis; Interconnect; Coupling noise; Signal integrity

INTRODUCTION

Now the industry is on the brink of logic integrated circuits (ICs) crammed with over 100 million transistors. The ICs of this dimension are built with the 0.13 μm CMOS technology and toward the 0.1 μm CMOS technology. The high-end microprocessor will contain 100 million transistors in 2002 and 200 million by 2005 and will target the clock frequency beyond 2 GHz for top-of-the-line system in the new millennium. The features of semiconductors for high-performance IC in the year 2005 is projected in Table I.

Successful delivery of the complex ICs rests on three pillars of support. They are superior electronic design automation (EDA) tools, advanced technology IC manufacturing, and powerful design flow methodology. Much attention is given to innovative changes that occur within each pillar as well as the dynamic relationships among the three pillars. So when the IC technology changes, the EDA tools and design flow methodology are directly affected. The very deep sub-micron (VDSM) (below 0.25 μm) IC manufacturing technology, to produce the complex ICs today and in the future, has had a direct influence on both the EDA tools and design flow methodology.

As IC technologies operates at increasingly higher speeds, system performance has become limited by the cycle time which is being reduced rapidly with the reduction of transistor feature size. To produce the high performance ICs in a wide range of application specific design areas, such as microprocessors, digital signal procession, communication, and networking, the accuracy of timing verification becomes vital when designs are being optimized for performance. The timing inaccuracy results in a productivity gap, especially for VDSM ICs, in which both EDA tools and traditional design flows break as they cannot keep pace with the rapid IC technology advances. The future mission is to develop silicon-accurate timing verification tools and positioning the tools in design flow methodologies to close the productivity gap of VDSM ICs.

Traditionally a dynamic simulator, at either the logic level or the circuit level, has been employed to verify the functionality and timing of an entire design or functional blocks within the design. However, dynamic simulation is a very time consuming process. This is especially true if detailed, precise timing behavior also needs to be taken into account while doing a functional simulation. Furthermore, dynamic simulation based methodology requires the careful crafting of test vectors that can serve

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TABLE I Semiconductors for high-performance IC in the year 2005

Process technology	0.1 micron
Total No. of transistors	200 M
Total No. of logic gates	40 M
Chip size	520 mm × mm
On-chip clock frequency	2.0–3.5 GHz
Total No. of I/O	4000
Total No. of wiring levels	7–8
Supply voltage	0.9–1.2 V
Supply current	~160 A
Power dissipation	~160 W

to exercise all the functional paths and the timing critical paths of the design. This is in itself an extremely difficult undertaking. And both the simulation time and the effort required for test vector generation has reached an unbearable level for designing present and future-generation multi-million-gate chips in VDSM process technology with several hundreds of MHz or even GHz clock frequency. The trend is thus to separate timing verification from functional verification. Functional verification is increasingly done with no regard to precise timing considerations, while timing verification is conducted without worrying about the functional behavior of the design.

Static timing analysis is an exhaustive method of analyzing and verifying the timing behavior of a design. This is accomplished by breaking down the design into sets of signal paths. The delay of each path is then calculated and analyzed against a collection of timing constraints for any possible violations. Since the methodology does not rely on simulation vectors, one major portion of the preparation effort is eliminated. The analyzer tends to run a lot faster compared to a dynamic simulator; thus the methodology can be applied to designs of much higher complexity. Furthermore, the method performs an exhaustive analysis of all signal paths, which would be nearly impossible using the dynamic simulation approach, considering the time it would take to run and the effort required to come up with the needed test vectors.

WHY NEEDS SILICON-ACCURATE TIMING VERIFICATION TOOL

No Present Verification Tools Guarantee Silicon-accurate Timing for VDSM ICs

It is witnessed in the industry that many IC design houses failed to deliver their products simply because they missed the market window for producing the chips that can prove to be market leaders. Today, for an advanced IC design, the percentage of time engineers spend in the timing verification is highly increased (may up to 40–50 % of the total design time) while compared with the time spent in the half-micron designs. Moreover, designers worry the most about the designs cannot meet timing specification in silicon and the timing problems that cause silicon fail cannot be captured before and even after the designs are taped out. Therefore, a more fully developed timing verification methodology will rely on an extensive assortment of timing verification tools. These tools greatly improve the efficiency of the design process by eliminating tremendous time and costs of debug before and after silicon. As we know designers find more design bugs earlier in the design, where they are less expensive to correct. The savings go directly to the bottom line when the working chips go to the market sooner. Nurturing this design art is a key challenge to deliver a silicon-accurate timing verification tools.

Traditional Design Flow Failed in Timing Sign-off for VDSM IC

In the traditional design flow, timing verification were done by the logic designer in the RTL simulation and logic synthesis stages, and if the design constraints including timing were met, the deliverable to the ASIC vendor would be a golden netlist. No more changes were made to the netlist before the ASIC vendor created the physical implementation (floor planning, cell placement, and routing). Using the traditional design flow with today's highly scaled IC technologies, timing achieved after the physical implementation differs greatly from timing estimated in the logic synthesis. A key to the breakdown of the traditional design flow is the overall delay of a high-speed, VDSM digital IC is dominated by its parasitic impedance (interconnect resistance and capacitance, coupling capacitance) rather than the gate capacitance, as was the IC with larger and slower circuit geometry. For example, the ratio of intrinsic delay to interconnect RC delay of global critical path can vary widely on larger die. Adequate simulation of these high-speed circuits requires the parasitic impedance be considered and represented accurately, which cannot be accurately estimated any more in the logic synthesis stage today. Timing inaccuracy in both the gate and transistor levels renders a high possibility of design failure for VDSM ICs. This fact manifests the traditional design flow facing the timing violation problems in the physical design.

Interconnect Delay Modeling Faced New Challenges for VDSM ICs

Cell delays can be accurately estimated during logic synthesis, however, interconnect delays are unknown until the wire geometry is defined in physical design. Logic synthesis uses the statistical models to estimate the interconnect delays. These estimates may be statistically accurate, but may not predict the delay of a single net accurately. Delay estimate for individual nets (global nets, long wires, large fan-out), which matters most for the critical path (the IC performance is determined by its longest timing critical path), can be inaccurate. Such interconnect prediction errors are not new, but these errors

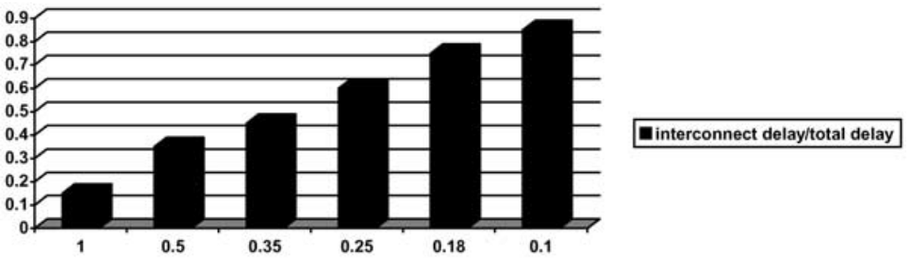

FIGURE 1 Delay ratio vs. device feature size (μm).

are not an issue when interconnect delays were a small percentage of total delays as they were in the half-micron world as seen in Fig. 1. It is anticipated to see below 0.18 μm the design tools and traditional design flows that optimize logic to achieve timing convergence fail—timing achieved after the physical implementation differs greatly from the timing estimated in synthesis. The statistical models accounting for interconnect delays will no longer be relied on for timing analysis and even for timing optimization for VDSM ICs. Silicon-accurate interconnect delay becomes an essential part of timing verification before the design can be signed off.

Pessimistic Timing Constraints Rendered a Difficult Delivery of VDSM ICs

Today, creators of VDSM ICs must wrestle with area and timing optimization, noise and power while attempting to bridge logic synthesis with physical design to speed up the overall design flow. It is witnessed designers used timing constraints in a conservative way to warrant the required timing relationships maintained before the designs are taped out. This design scenario either caused speed suffer and the circuit became slow not being able to meet the performance requirement or rendered the timing optimization in both logic synthesis and physical implementation very difficult or even unable to achieve. To achieve timing convergence, all design flow tools need to be driven by the same or equivalent timing constraints. To the extent, the timing of critical path obtained after physical implementation is not fast enough and because of pessimistic timing constraints further logic synthesis and optimization may still not solve the problem. At this point, designs are positioned in an unstable and timing in-convergent design flow in which the delivery of silicon becomes very difficult.

Unintentional Clock Skew and Phase Delay Cause Circuit Malfunction

Clock signals connect to every flip-flop and toggle faster than any other signals in a digital IC. For every data transition most clocks need to transition twice to complete a full cycle. If clock skew is not properly controlled and accurately analyzed, unexpected timing violations and system failures are possible. Being the fastest and most heavily loaded signals, clocks deserve special attention. As chip size increases, the resistance and capacitance of global interconnect increases linearly with the chip dimension. As a result, clock tree network produces large RC loads which greatly increases the unintentional clock skews, originated from process and environmental variations. These skews constitute a significant portion of the total cycle time and limit the clocking rate and chip performance. Another important factor that contributes to the clock cycle time is the propagation delay (phase delay) caused by interconnect. The large phase delay may result in insufficient charging/discharging devices thereby causing a circuit malfunction. It is in demand of an unique solution to automate the timing simulation in SPICE for entire clock tree, report SPICE-proven clock skews and phase delays, identify timing problems caused by unintentional clock skew and large phase delay.

IR Drop Effect Creates Variations in Timing and Causes Silicon Failure

As power and ground is distributed via metal lines across the chip, these metal lines are plagued by two major problems: electromigration and extensive metal line resistance, specifically for today's DSM ICs with the increasing chip size and the decreasing power supply voltage. As the line resistance increases, the voltage drops on the power lines also increases. This IR drop effect creates variations in the actual voltage seen at each cell. These voltage variations affect each cell's timing, interconnect delay, chip performance and may cause silicon failure if timing is not accurately considered. IR drop delay analysis is needed to help design houses to avoid the risk of silicon failure caused by IR drop effects. IR drop delay analysis will improve the accuracy of timing analysis by reading in power grid voltage values provided by IR drop analysis tool. It will then map these actual voltage values to the instances on the critical paths and nets, and then automate Spice runs using the actual voltage seen at each instance. IR drop delay analysis flow will provide Spice-proven timing view considering IR drop effects on critical path timing as well as clock skew and phase delay.

Timing Closure and Signal Integrity Faces New Challenges for VDSM IC

Lack of timing closure is caused by the inability of synthesis timing to correlate physical timing, wire delay due to interconnect dominates timing. While there has been progress in taking crosstalk into account physical timing, approaches that link synthesis with placement cannot effectively account for signal integrity effects. Thus, iterations between the logical and physical domain for timing convergence have not been fully eliminated in today's solutions and will continue to increase unless signal integrity effects are taken account. Signal integrity effects have always existed, but as technology scales down that have become a great concern. Coupling capacitance becomes a dominant factor, interconnect resistance increases, device noise margin decreases, and inductive effects caused by high frequencies increase. These factors contribute to VDSM IC becoming more sensitive to crosstalk noise and delay. Signal noise due to crosstalk may cause the neighboring receiver gate switch erroneously; therefore causes chip malfunction.

SILICON-ACCURATE TIMING TOOL

Silicon-accurate Timing

A silicon-accurate timing tool for integrated circuit design verification embodies a number of major techniques in advancing the art of timing verification. Table II compares present and future silicon-accurate timing tools. A silicon-accurate timing tool will take block SPICE Netlist, partitions the netlist into groups, characterizes timing in each group and then verifies block timing. The timing report is presented to pinpoint the timing critical paths. In Addition, the timing tool can be used for full chip timing solution by collecting and analyzing pre-characterized block timing results. Instead of relying on the pre-stored timing models, a silicon-accurate timing tool actually generates the necessary interfacing information and invokes the timing simulator to produce the needed timing data for the subsequent analysis. This is of paramount importance for the current and future multi-million transistors, VDSM, very high performance integrated circuit designs

A silicon-accurate timing tool will need to be positioned in a structured custom design flow (a combination of standard cell synthesis flow and custom design flow). Logic designers first do the timing iterations according to the timing verification in the RTL entry, simulation and synthesis stages. If the constraints were met, the deliverable to the placement and routing would be a netlist representing a functionally complete design that met timing in logic synthesis. Then the physical designers take the netlist and created the physical implementation (floor planning, placements, and routing). It is witnessed, in VDSM IC technology, timing achieved after placement and routing differs greatly from timing estimated in logic synthesis stage. The main cause is the delay of interconnects in VDSM IC designs. It is required that after RC extraction for the loading and interconnect delays, the physical designers use timing tools to do the timing iterations for the post layout synthesis. The counter part of synthesis flow is custom design flow. The custom design flow supplies the high timing accuracy demand for the high-speed design community. In this flow, the custom designers use the timing tools for timing verification for circuit designs, custom layouts of cells and blocks, and even for the entire chip combining the blocks synthesized from the synthesis flow. Global nets with RC back-annotation are considered to guarantee the timing constraints met in the chip level.

Because interconnect delay now dominates gate delay, the trend in physical implementation is to include placement within a floor-planning tool and use a separate router for wiring. The initial logic synthesis contains no or little information on any interconnects loading. From the initial floor-plan inter-block capacitance values are input to the logic synthesis tools as load constraints and intra-block capacitance values are input as wire-load models. At this point the logic synthesis tool is able to re-synthesize

TABLE II Present and future silicon-accurate timing tools

Present timing tools	Future silicon-accurate timing tool
Require pre-characterized cell libraries and statistical models to estimate wire delays that result inaccurate timing in VDSM Ics	Proven Spice accuracy by combining the cell and interconnect RC load for timing simulation
Separate cell-based and custom design flow	Support a combination of cell-based and custom design flow
Not support parallel simulation	Support parallel simulation
Use design patent recognition and/or Boolean equivalence for timing verification	Recognize transistor and circuit design style for meaningful timing verification
Not support Spice-proven timing accuracy for coupling C and distributed RC back-annotated from physical designs	Proven Spice accuracy for coupling C and distributed RC back-annotated from physical designs
Not support silicon debug to identify the timing violations	Support silicon debug to identify the timing violations
Not characterize memory/cache with proven vectors and proven SPICE timing accuracy	Characterize memory/cache with proven vectors and proven SPICE timing accuracy

TABLE III Summary of benchmarks (2.0 V, 0.25 μm CMOS)

Circuit	ead	feu	mac	ebm	ebr	exd
MOS count	6709	44,980	53,313	3942	1237	6641
Subckt count	31	153	93	0	0	0
Subckt instantiation	2057	16,506	36,577	0	0	0
Net count	2230	18,300	25,868	1128	505	2868
Clock net	1	2	1	15	13	36

TABLE IV Critical Path Delays of Benchmarks

	ead	error (%)	feu	error (%)	mac	error (%)	ebm	error (%)	ebr	error (%)	exd	error (%)
Present popular commercial timing tool	967	31.56	866	9.76	2249	14.57	1432	7.67	1218	5.64	4680	42.42
Silicon-accurate timing tool	747	1.63	810	2.66	1966	0.15	1325	−0.38	1157	0.35	3278	−0.24
SPICE deck simulation	735	–	789	–	1963	–	1330	–	1153	–	3286	–

"Present popular commercial timing tool" denotes critical path timing results using Hspice by a commercial tool.
"Silicon-accurate timing tool" denotes critical path timing results using Hspice by silicon-accurate timing tool.
"SPICE deck simulation" denotes dynamic timing results of the critical path using Hspice.

the logic based on estimates of interconnect loading each gate is driving. The synthesis tool produces an estimate delay file to constrain path delays in the placement step. After employing the placement using constraints from the synthesis tool, the location of every logic cell on the chip is fixed and estimates of interconnect delay are passed back to the logic synthesis tool. The synthesis tool employs in-place optimization (IPO)—changes the drive strength of cells based on interconnect delay estimates without altering the netlist structure. Then the placement information is ready to be input to the routing step. As we know without complete routing, interconnect delay still cannot be accurately estimated. A silicon-accurate timing tool is employed in post layout timing verification, which uses standard delay format (SDF) to back-annotate the interconnect delay. If the timing were not met which is very possible for VDSM IC, the logic synthesis tool would use the back-annotated SDF from a silicon-accurate timing tool to improve the logic structure. The SPICE-proven accuracy of a silicon-accurate timing tool will position it in an approach to timing closure design methodology.

Timing Accuracy

Prior art timing analysis tools take analytical approaches and place emphasis on supporting modeling capabilities to create estimate timing models for logic gates or certain composite cells, allowing designers to perform the timing analysis. These timing engines are not designed to accurately characterize interconnect and will generate results that are inconsistent with actual timing in physical layout. Therefore, it is critical to establish a physically accurate reference for timing and interconnect delay information. Using simulation-based technology, a silicon-accurate timing tool simulates logic gates and composite cells including interconnect parasitic impedance, guarantees consistency between physical and silicon timing calculation. Table III presents circuit description of benchmarks that include several microprocessor circuits. Table IV compares the timing accuracy of silicon-accurate timing tool and a popular commercial timing tool. As seen from Table IV the timing accuracy of silicon-accurate timing tool is within 3% error in

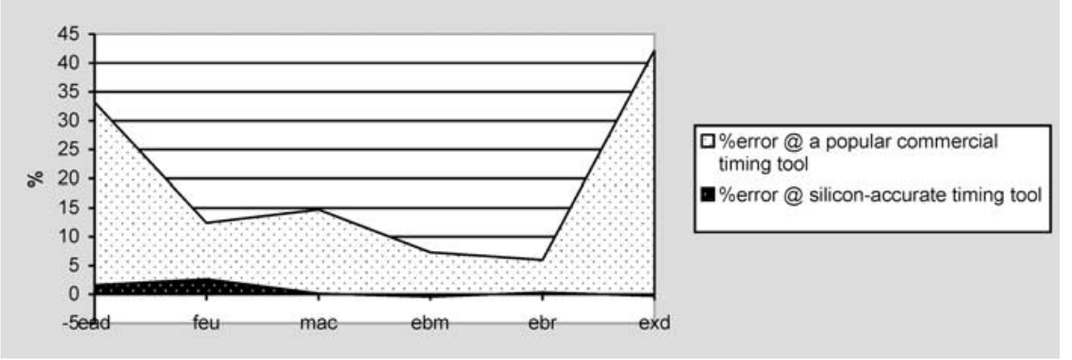

FIGURE 2 Timing accuracy comparison.

comparison with Spice deck simulation results. Figure 2 depicts the timing accuracy comparison.

CONCLUSION

Designing high-performance VDSM IC poses a tremendous challenge for IC design houses. Larger geometry, lower voltage, and high frequency requirements are causing silicon-accurate timing problems to appear in integrated circuits even worse. Present EDA tools have neither the ability to achieve timing convergence for VDSM IC, nor the capacity to handle today's system-on-chip (SOC) designs. Timing convergence refers to the iterative process of getting timing results from a design's physical layout to match those reported by logic synthesis. Silicon-accurate timing tools are necessary to overcome timing challenges and limitations that cause timing convergence and capacity problems.

Ichiang Lin received the Ph.D. from Department of Computer Science, University of Minnesota, Minneapolis. He has been as a technical member and senior consultant in IBM, Silicon Graphics, AMD/NexGen, NEC, where he has delivered timing solutions to many IC designs. He is currently President and CEO of Baynacre, Inc. His expertise in the timing analysis has been applied to VDSM ICs, which addresses the technical issues challenged in the IC design communities of the Silicon Valley. He has published several journal and conference articles in this area.

Chien-In Henry Chen received the B.S. degree from the National Taiwan University, the M.S. degree from the University of Iowa, and the Ph.D. degree from the University of Minnesota, all in electrical engineering. He is currently a Professor of Electrical Engineering at Wright State University at Dayton, Ohio. From June 1999 to August 2000 he was on leave with Baynacre, Inc., developing silicon-accurate timing verification technologies. His work is primarily in the areas of digital and mixed-signal design synthesis and testing, timing analysis and optimization for VDSM IC, and IC chip design for signal processing, communication and networking. He has written over 70 publications in professional journal and conference proceedings. He is a technical committee member of the 1995, 1996, 2000, 2001 and 2002 IEEE International ASIC/SOC Conference. He was a plenary speaker of 1995 the 6th VLSI Design/CAD Symposium.