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Research Article

Power Consumption and BER of Flip-Flop Inserted Global Interconnect

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In nanometer scale integrated circuits, concurrent insertion of repeaters and sequential elements into the global interconnect lines has been proposed to support multicycle communication—a concept known as interconnect pipelining. The design targets of an interconnect-pipelining scheme are to ensure high reliability, low-power consumption, and less delay cycles. This paper presents an in-depth analysis of the reliability in terms of bit error rate (BER) and the power consumption of wire-pipelining scheme. In this analysis, the dependencies of power consumption and BER on the number of inserted flip-flops, and the size of repeaters are illustrated. To trade off the design targets (wire delay, BER, and power consumption), a methodology is developed to optimize the repeater size and the number of flip-flops inserted which maximize a user-specified figure of merit. The methodology is demonstrated by calculating optimal solutions for interconnect pipelining for some International Technology Roadmap for Semiconductor technology nodes.

1. INTRODUCTION

The delay associated with global interconnect lines has been increasing with technology scaling because the global interconnect length do not scale down with feature sizes. In fact, with the decreasing feature sizes of MOS devices, more functionalities are expected to be integrated on a chip, which leads to increasing length and number of global interconnects [1]. Consequently, in future nanometer designs, it will be impossible to carry signal across the chip in a single clock cycle, and multicycle cross-chip communication will become necessary. With multicycle interconnect cross-chip wires removed from all the timing constraints, chip speed can be determined by the most critical intrablock/local combinational path, in order to continue employing higher frequencies [2, 3]. Insertion of sequential elements in interconnects lines—a concept that has become known as *interconnect pipelining*—is one feasible solution to support multicycle communication in modern nanometer technologies. The idea is to divide a wire, whose delay is longer than one-clock cycle, into several segments by inserting sequential elements to store signal values that require multiple clock cycles to travel through a particular global wire. Two types of sequential elements can be used for this purpose, and hence interconnect pipelining can be divided into two types: (i) flip-flop based, and (ii) latch-based wire pipelining.

The implementation issues of interconnect pipelining can be addressed from several aspects, such as, CAD related problems, architecture-level design issues, and circuit-level design and performance issues. Current CAD tools must be modified to take interconnect pipelining into consideration. A list of CAD related challenges of wire pipelining, and the corresponding changes that must be made to current CAD tools are identified in [4]. In [5], a floor-planning methodology, which considers interconnect pipelining and its impact on performance using the IPC sensitivity models is described. To address the problem of altering function or cycle behavior of a circuit [2] due to wire pipelining, several approaches at the logic and architecture level have been proposed, such as, wire retiming [6], algorithm working at the gate level [7], and latency insensitive technique [8]. The authors in [3] explored the possibilities of sharing interconnect pipelining to reduce wiring overheads. In [9], a study of bit error rate in interconnect pipelining is presented using statistical timing analysis approach. In [10, 11], prospects and challenges of latch-based interconnect pipelining have been analyzed and two techniques to deal with the short path constraint of latch-based wire pipelining are provided in [10].

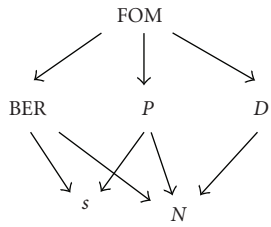


Figure 1: Dependence of the parameters of wire pipelining.

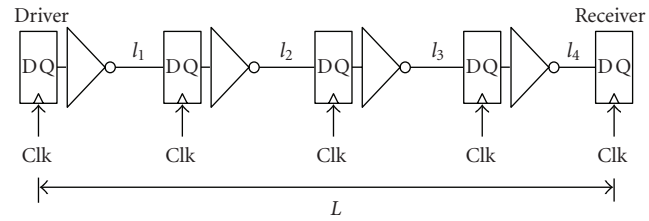


Figure 2: DFF pipelined interconnect.

The analytical model to determine the number, position and feasible region for flip-flop, based wire pipelining has been presented in [12]. A method of estimating the interconnect power at the chip level considering concurrent repeater and flip-flop insertion is given in [13]. However, most of the existing works on interconnect pipelining address CAD and architecture-level design issues. There are very little work done for analyzing circuit-level implementation and performance issues.

As the system delay is now dominated by the interconnect delay, an increasing number of repeaters and flip-flops or latches are expected to be used to reduce the interconnect delay. Additional power consumption due to these repeaters and sequential elements will become a significant portion of the total system power [14]. The reliability of a wire-pipelining scheme depends on the circuit level parameters. One of the most important measures of the reliability of interconnect pipelining scheme is the bit error rate (BER), which will be affected by the parameters of inserted sequential elements and the circuit as a whole. Therefore, the relationships between the design targets and basic circuit-level parameters must be constructed. There are many techniques to optimize global interconnect in terms of latency, bandwidth, and power dissipation [15–18]. But none of them take wire pipelining into consideration. This paper studies the dependency of the bit error rate (BER) and power consumption on the number of flip-flops inserted and the size of repeaters. Here, an optimization technique for flip-flop-based global wire pipelining has been proposed to maximize a user-defined figure of merit.

For global interconnect system ,three very important design metrics are (i) reliability, (ii) power consumption (P), and (iii) delay cycles (D). In an interconnect-pipelining scheme, reliability can be measured by bit-error rate (BER), and delay cycles are equal to the number of wire segments N. Again, BER and power consumption are functions of repeater size and number of wire segments or the number of inserted sequential elements. So the parameters involved with these three metrics are (i) number of wire segment or number of sequential element and (ii) repeater size. Figure 1 illustrates the dependence of the figure of merit (FOM) on the three above-mentioned performance metrics and corresponding parameters in a wire-pipelining scheme. Depending on the requirements and constraints of any global interconnect system to be implemented, this FOM can be any function of these three or any other performance metrics. The designer will determine the function based on the requirements and constraints in the specific case. The concept illustrated in Figure 1 is general and it can be extended for any number of performance metrics and parameters. Section 4 defines one such FOM and presents a methodology to optimize that FOM.

2. POWER ESTIMATION OF INTERCONNECT PIPELINING

In typical D flip-flop-based interconnect pipelining (as shown in Figure 2), two types of components are used: DFF and repeater. Because of the structure of the wire pipelining, it is convenient to divide the total power dissipation into two parts: power consumed by flip-flops and the power consumed by repeaters.

First, let us consider the DFF power consumption. Usually, the power consumption is composed of 3 parts: dynamic power, leakage power, and short-circuit power. But according to [16], with technology scaling, the short circuit power is becoming a minor part in nanometer circuit. Therefore, only dynamic and leakage power components are considered here. If the clock frequency is denoted by f_{clk}, the switching probability and the total capacitance of node i are represented by α_i and C_i, respectively and the swing range coefficient of node i is given by k_i, the dynamic power consumption of a single DFF can be expressed by [15]

$$P_{\text{dF}} = f_{\text{clk}} C_{\text{eff}} V_{\text{DD}}^2 \quad \text{where } C_{\text{eff}} = \sum_{i=1}^{N} \alpha_i k_i C_i. \tag{1}$$

And, the leakage power is

$$P_{\text{lF}} = V_{\text{DD}} I_{\text{off}} s_F, \tag{2}$$

where I_{off} is the unit leakage current and s_F is the total gate size of one FF. Therefore, the total power consumption of a DFF can be estimated as

$$P_{\text{FF}} = P_{\text{dP}} + P_{\text{lP}} = f_{\text{clk}} C_{\text{eff}} V_{\text{DD}}^2 + V_{\text{DD}} I_{\text{off}} s_F. \tag{3}$$

The power consumption of different types of DFFs is different. Figure 3 shows the comparison of the power dissipation in two types of flip-flops for different technology nodes. The schematic of these two types of flip-flops (a dynamic flip-flop and a static flip-flop) are shown in Figure 4 [19].

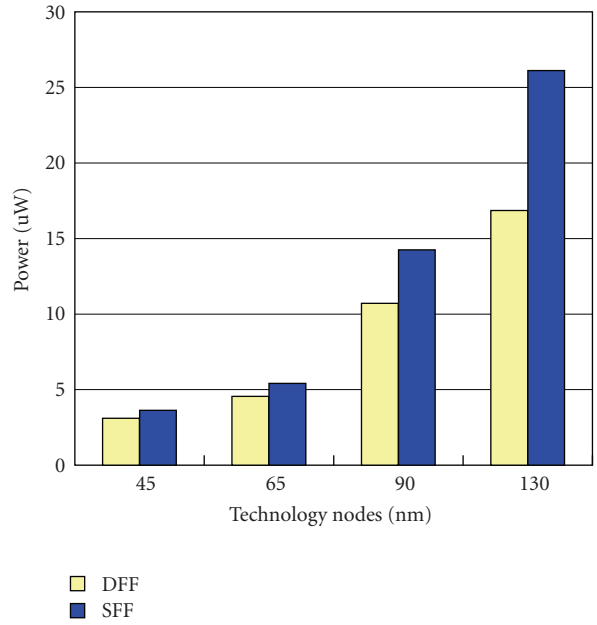


Figure 3: Comparison of the power consumption of the two kinds of flip-flop.

From the comparison, it can be observed that, for all technology nodes, the power dissipation of dynamic flip-flop is smaller than that of the static counterpart. The results are acquired through Spectre circuit simulator. In this simulation, the switching probability is 0.5 and the clock frequency is 1 GHz. The parameters used in this simulation are listed in Table 1, which is obtained from [17, 20].

Now, let us consider the power consumption of the repeaters. Here, we assume that for a minimum-sized repeater, the input capacitance is c_0, the output parasitic capacitance is c_p, and output resistance is r_s. The size of the repeaters are usually large enough so that it can drive the whole wire segment (Figure 5). If the repeater size is denoted by s, the total output resistance is $R_{\text{tr}} = r_s/s$, the output parasitic capacitance $C_p = c_p s$ and the input capacitance is $C_L = c_0 s$. And, a uniform interconnect of resistance r per unit length and capacitance c per unit length is assumed.

If l is the wire length and α is the switching factor, the switching power of the repeater is given by [16]

$$P_{\text{dR}} = \alpha\left(s(c_p + c_0) + \text{lc}\right) V_{\text{DD}}^2 f_{\text{clk}}. \tag{4}$$

And, the average leakage power of a repeater can be expressed as [16]

$$P_{\text{lR}} = \frac{1}{2} V_{\text{DD}} \left(I_{\text{off}\,n} W_{n\,\text{min}} + I_{\text{off}\,p} W_{p\,\text{min}}\right) s. \tag{5}$$

Here, $W_{n\,\text{min}}$ and $W_{p\,\text{min}}$ are the width of the NMOS and PMOS transistor in minimum-sized inverter, respectively. In this paper, we assume that $I_{\text{off}\,n} = I_{\text{off}\,p} = I_{\text{off}}$ and $W_{p\,\text{min}} = 3W_{n\,\text{min}}$, and (5) can be written as

$$P_{\text{lR}} = 2V_{\text{DD}} I_{\text{off}} W_{n\,\text{min}} s. \tag{6}$$

Considering only dynamic and leakage power components, the total power consumption of the repeaters can be given by

$$P_{\text{repeater}} = P_{\text{dR}} + P_{\text{lR}}. \tag{7}$$

If $(N-1)$ flip-flops are inserted in a global interconnect of length L, the wire will be divided into N segments and there will be total $(N+1)$ *flip-flops* in the wire-pipelining scheme including the driver and receiver registers. In that situation, N repeaters are required to drive the N wire segments. Therefore, the total power consumption in the pipelined-interconnect will be

$$P_{\text{total}} = (N+1)P_{\text{FF}} + NP_{\text{repeater}}. \tag{8}$$

Using (7) and (4), we may write a detailed expression of the power consumption based on the number of inserted flip-flops and the size of the repeaters s,

$$P_{\text{total}} = (N+1)P_{\text{FF}} + k_1 Ns + k_2, \tag{9}$$

where $k_1 = \alpha(c_p + c_0)V_{\text{DD}}^2 f_{\text{clk}} + 2V_{\text{DD}} I_{\text{off}} W_{n\,\text{min}}$, $k_2 = \alpha L c V_{\text{DD}}^2 f_{\text{clk}}$, and $L = Nl$. From (9), it can be observed that power consumption in pipelined wire will increase with the increase of the repeater size and the number of inserted repeaters and flip-flops.

To compare power consumed by the inserted flip-flops and repeaters, a 4-stage pipelined wire is implemented as shown in Figure 2 using dynamic DFF, and repeaters of size 10 times of the minimum size. The power is measured by Spectre® circuit simulator, which is illustrated in Figure 6. From the comparison, it can be observed that the power consumed by the repeaters is much higher than the power consumed by the DFF in all the technology nodes. Usually, in a global wire, the power consumption of the repeaters is more than 10 times of the power consumed by the flip-flops. For example, for 90 nm technology the power consumed by repeaters is 415 uW; but, it is only 39.7 uW for the flip-flops.

3. BIT ERROR RATE ANALYSIS

A detailed study of flip-flop-based wire pipelining is given in [12], where a set of models are presented to determine the minimum number of flip-flops to be inserted, central position, and feasible region of each inserted flip-flop. However, the analysis does not take many circuit-level issues into consideration including repeater sizing, process and parameter variations, and clock signal variation. In real circuits, non-ideal behaviors of circuits and signals due to temporal and spatial variation of clock signal (clock skew and jitter), wire delay uncertainty, and variations of timing parameter f the sequential elements will greatly decrease the reliability of a wire-pipelining scheme.

One indication of the reliability of pipelined interconnect is the bit error rate (BER), which is the error probability when a single data bit is transmitted through a pipelined global interconnect wire. BER is dependent on the repeater size and the number of wire segments or inserted flip-flops. In order to estimate the BER in flip-flop-based wire pipelining, a method based on statistical timing analysis is presented

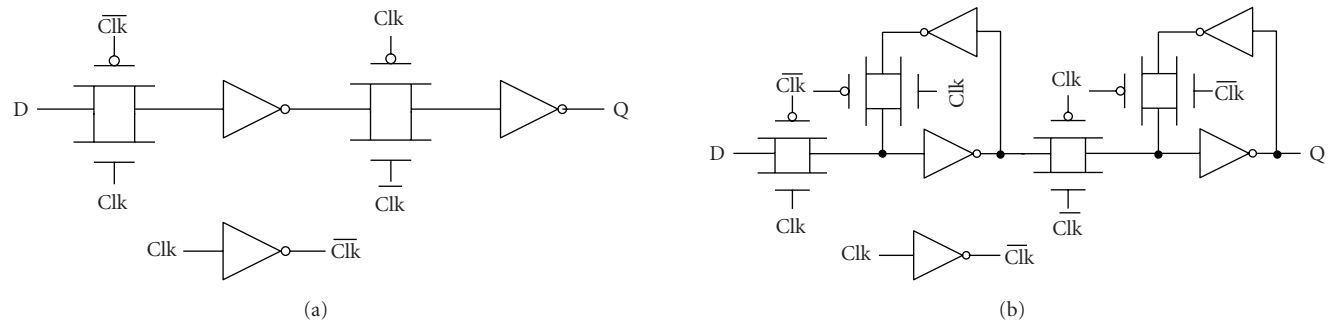


Figure 4: Dynamic DFF and static DFF.

Table 1: Technology and equivalent circuit model parameters for different technology nodes.

Tech. node (nm)	130	90	65	45
Width (nm)	335	230	145	103
Thickness (nm)	670	482	319	236
r (Ω-um)	0.098	0.198	0.475	0.905
c_a (fF/mm)	207	181	165	143
c_b (fF/μ^2)	0.057	0.071	0.103	0.116
c (fF/um)	0.226	0.197	0.180	0.155
V_{DD} (V)	1.1	1	0.7	0.6

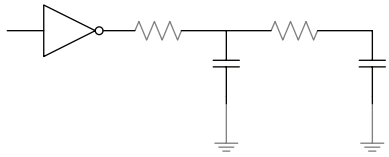


Figure 5: A long wire driven by a repeater.

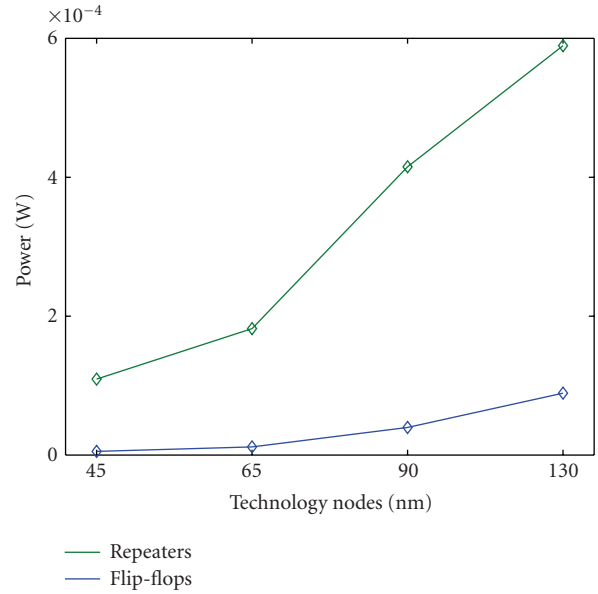


Figure 6: Comparison of the power consumed by flip-flops and repeaters in a wire-pipelining scheme.

in [9]. For a typical DFF-based interconnect pipelining as shown in Figure 1, consider T_{setup} to be the set up time of a DFF, T_{prop} to be the propagation delay from D to Q after the positive clock edge, T_{clk} to be the clock period, and t^i_{wire} to be the propagation delay from the output of DFF at $(i-1)$th stage to the input D of DFF at ith stage. For the DFF at the ith stage to properly latch on a data bit, the propagation delay can be given by (11), which must satisfy a timing constraint given by (10),

$$0 \le d_i \le T_{\text{clk}} - T_{\text{setup}}, \tag{10}$$

$$\text{where } d_i = T_{\text{prop}} + t^i_{\text{wire}}. \tag{11}$$

If we define a variable $\delta_i = T_{\text{prop}} + t^i_{\text{wire}} + T_{\text{setup}} - T_{\text{clk}}$ with a probability density function $p(\delta_i)$, then the probability to have correct data transmission between the $(i-1)$th and ith stage can be expressed as in

$$q_i = \Pr\left(T_{\text{setup}} - T_{\text{clk}} \le \delta_i \le 0\right) = \int_{T_{\text{setup}}-T_{\text{clk}}}^{0} p(\delta_i)\, d\delta_i. \tag{12}$$

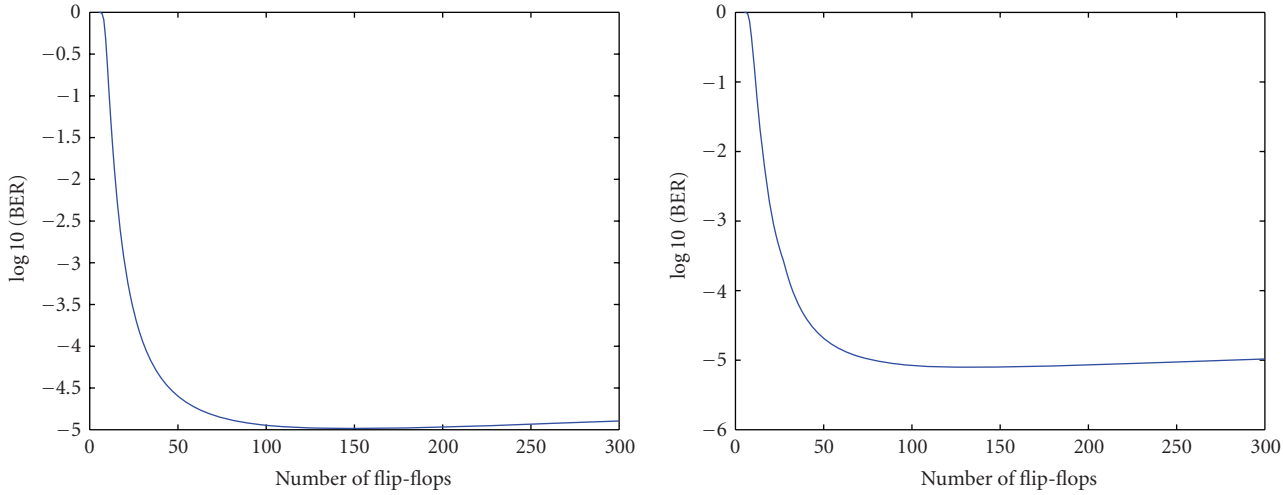
Since $d_i = T_{\text{prop}} + t^i_{\text{wire}}$ is definitely greater than zero, the probability of the event $\delta_i < T_{\text{setup}} - T_{\text{clk}}$ is zero. Therefore, the above equation can be written as in (13), where the lower bound of integration is extended from $T_{\text{setup}} - T_{\text{clk}}$ to $-\infty$,

$$q_i = \int_{-\infty}^{0} p(\delta_i)\, d\delta_i. \tag{13}$$

Due to the presence of a DFF, the probability of correct data transmission at each stage is independent of each other. Hence, for an N-stage flip-flop-based wire pipelining the BER can be given by

$$\text{BER} = 1 - \prod_{i=1}^{N} q_i. \tag{14}$$

In reality, because all the process parameters have normal distributions, it is reasonable to assume that all timing variables T_{prop}, t^i_{wire}, T_{setup}, and T_{clk} also have normal



(a) 130 nm (b) 65 nm

Figure 7: BER versus number of DFFs.

distributions. In that case, δ will also have a normal probability density function (*p.d.f*) with

$$\mu_{\delta i} = \mu_{T\text{prop}} + \mu_{\text{itwire}} + \mu_{T\text{setup}} - \mu_{T\text{clk}},$$
$$\sigma^2_{\delta i} = \sigma^2_{T\text{prop}} + \sigma^2_{\text{itwire}} + \sigma^2_{T\text{setup}} + \sigma^2_{T\text{clk}}. \tag{15}$$

Hence, the probability to have correct data transmission between the $(i-1)$th and ith stage can be expressed as in

$$q_i = P(\delta \le 0) = \frac{1}{2} + \text{erf}\left(-\frac{\mu_{\delta i}}{\sigma_{\delta i}}\right), \tag{16}$$

where $\text{erf}(x) = (1/\sqrt{2\pi})\int_0^x \exp(-t^2/2)dt$. If define $\delta' = T_{\text{prop}} + T_{\text{setup}} - T_{\text{clk}}$, (13) can be written as in (17), and the BER of the whole wire pipelining can be given by (18),

$$q_i = \int_{-\infty}^{0} p(T_{\text{prop}} + t_{\text{wire}} + T_{\text{setup}} - T_{\text{clk}})d\delta_i = \int_{-\infty}^{-t_{\text{wire}}} p(\delta')d\delta', \tag{17}$$

$$\text{BER} = 1 - \left(\int_{-\infty}^{-t_{\text{wire}}} p(\delta')d\delta'\right)^N. \tag{18}$$

It is assumed that all the flip-flops are evenly distributed along the global interconnect in the above equation, so all the wire segments have the same delay t_{wire}. From (18), it is clear that the BER of the wire pipelining will be affected by the wire-segment delay and the number of flip-flops inserted. Again, the wire-segment delay will be affected by the number of inserted flip-flops, and the size of repeater, which can be observed from the expression of the wire-segment delay given by [21]

$$t_{\text{wire}} = \left(r_s(c_0 + c_p) + \frac{r_s}{s}cl + rlsc_0 + \frac{1}{2}rcl^2\right)\ln 2. \tag{19}$$

Here, l is the length of the wire segment and $l = L/N$. Substituting (19) into (18), the final expression for BER can be obtained.

To observe the impacts of the number of inserted flip-flops and the size of repeaters on the reliability of wire-pipelining scheme, several sets of analysis results are presented here. First, keeping the repeater size fixed, the relationship between the number of inserted flip-flops and the BER is illustrated in Figure 7. In these examples, the length of the global interconnect is 20 mm and the standard deviations of all the parameters are 10% of their nominal value. It is shown that the lowest BER is reached when the number of flip-flops is unusually large (147 for 130 nm technology and 135 for 65 nm technology). But in real circuit, it is impractical to insert so many flip-flops into a global interconnect, because excessive delay and power consumption of the flip-flops will nullify the gain of wire-pipelining. So, a trade-off must be made between the BER and the total delay time.

The Spectre simulation reveals the same conclusion for an example wire pipelining scheme in 65 nm technology, where the distance between the driver and the receiver is 3.2 mm. From the experimental results in Figure 8, it is observed that when N equals 3, a bit error will occur, and increasing N will solve this problem. According to the output waveform, it is unnecessary to insert more than 5 DFFs into this global interconnect because the output waveform is already good enough with 5 flip-flops.

To observe the relationship between BER and buffer sizing, consider a 0.5 mm long line in 65 nm technology driven by a buffer of size s. Analytical observation of the relationship between the wire delay and the repeater size is shown in Figure 9. It can be noticed that the minimum delay is achieved when the repeater size is 65. The size of the repeater for a particular line can also be calculated by [21]

$$s_{\text{opt}} = \sqrt{\frac{r_s c}{r c_0}}. \tag{20}$$

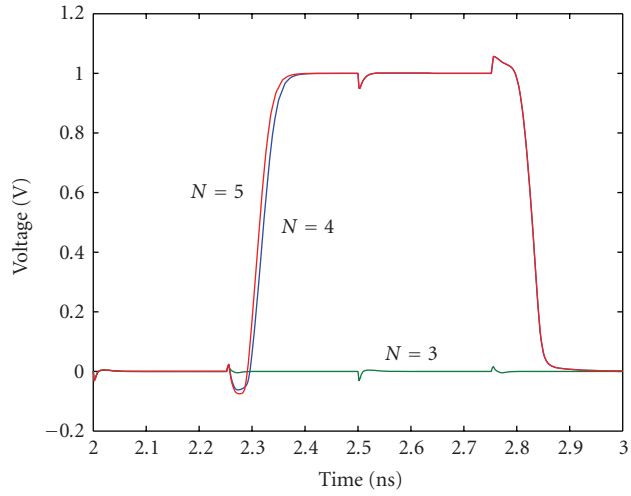


FIGURE 8: Output waveform for different numbers of inserted DFFs.

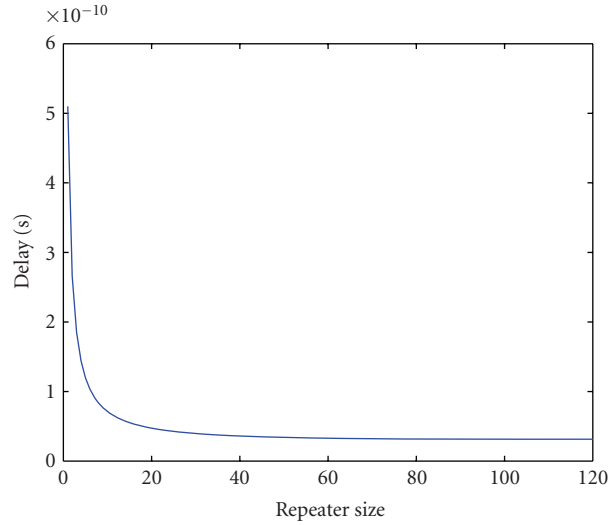


FIGURE 9: Delay versus repeater size.

But in practice, the repeater size is usually much smaller than the repeater size given by (20) due to the high power consumption and area cost involved with such large repeater. Again, driving a repeater of such size will be problematic.

For simulation, a 3-stage wire pipelining scheme in 65 nm technology is considered, where the same DFF as previous experiments has been used. This time, the distance between the driver and the receiver is 5 mm and all the inserted flip-flops are evenly distributed along the global wire. The Spectre simulation of Figure 10(a) shows the relationship between the total delay for one wire segment and the repeater size. Using the data obtained from this simulation, the BER for different repeater sizes can be calculated. The result is given by Figure 10(b), where it can be observed that the BER will be greater than 50% if the repeater sizes are less than 12.5 times of the minimum size. In this calculation, the standard deviation of all the parameters is 3% of their nominal values. The output waveform is shown in Figure 11, in which it can be noticed that it is nearly impossible to transmit signal through this pipelined wire if the repeater size is less than 12 times the minimum size. The simulation results are nearly identical with the calculated results.

Although increasing repeater size will lower the BER, from earlier analysis in Section 2 it can be inferred that power consumption will restrict the maximum size of repeater. Therefore, a trade-off must be made between tolerable BER and power consumption for an optimum design solution, which will be discussed in the next section.

4. OPTIMIZATION METHODOLOGY

The maximization of the performance of global interconnects will ask for simultaneously achieving smaller delay D, lower power consumption P, and higher reliability (lower BER). However, earlier analysis reveals that lower BER can be obtained either by increasing the repeater size when the repeater size is smaller than a certain threshold or by increasing the number of inserted flip-flops as long as the number of inserted flip-flops is small. But both options will definitely increase the power consumption. Again, with the increase of the number of inserted flip-flops, the delay cycles of the whole interconnect, which is equal to the number of wire segments, will increase. But it is not desirable to have higher delay cycles. Therefore, in order to obtain an optimal solution for a particular wire-pipelining scheme, some trade-off must be made between power consumption, BER, and number of delay cycles. Here, a figure of merit (FOM) is introduced, which is a function of BER, power consumption P, and number of delay cycles N as defined in (21). Here, i, j, and k are the weights of the cost functions which imply which design objective is more important,

$$\text{FOM} = \frac{(1 - \text{BER})^{i}}{P^{j} \cdot N^{k}}. \tag{21}$$

The range of the BER is from 0 to 1, and the number of delay cycles N is an integer that is greater than or equal to 1. Power consumption of different implementations for a particular wire pipelining varies relatively little. According to the range of these three parameters, the choices of 3, 3, and 1/2 for i, j, and k, respectively, are reasonable. Different values for i, j, and k may be chosen by the designer for different design objectives. For example, a larger value of j may be used by a designer who desires a power-efficient design. Optimal number of wire segments, and size of repeater for the maximum value of the figure of merit can be determined by setting the derivatives of (21) with respect to N and s to zero as shown,

$$\frac{\partial \text{FOM}}{\partial N} = 0, \qquad \frac{\partial \text{FOM}}{\partial s} = 0. \tag{22}$$

The methodology outlined above is used to optimize the number of inserted flip-flops, and the size of the repeaters in two examples of wire pipelining for ITRS technology nodes of 130 nm and 65 nm. Here, a global wire of 5 mm in length

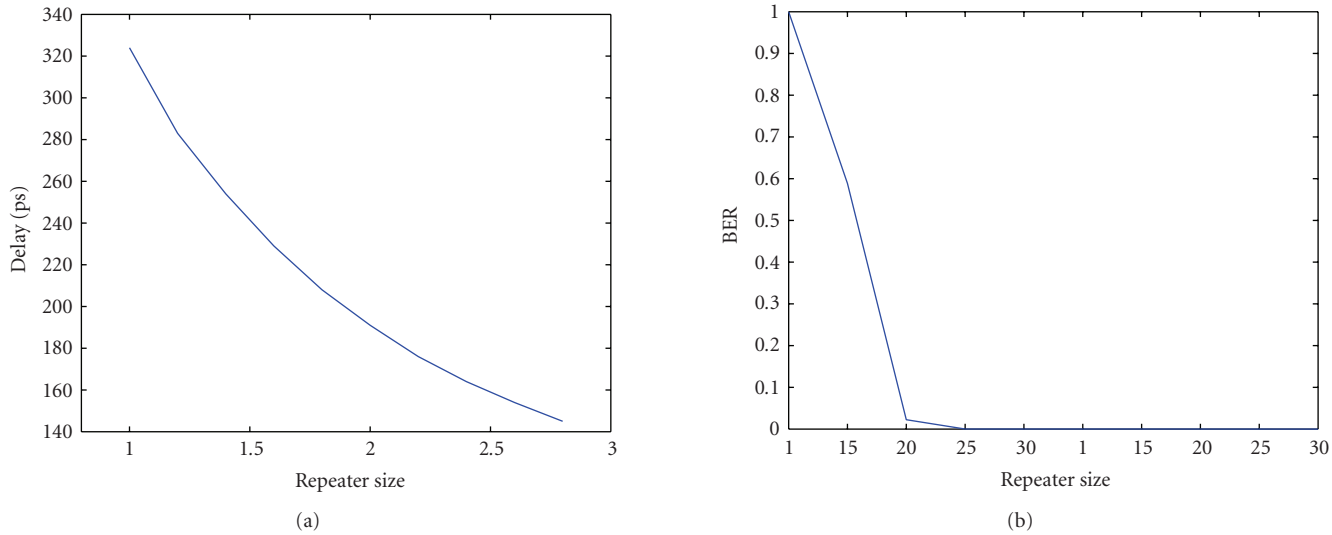


Figure 10: (a) Repeater size versus delay, (b) BER versus repeater size.

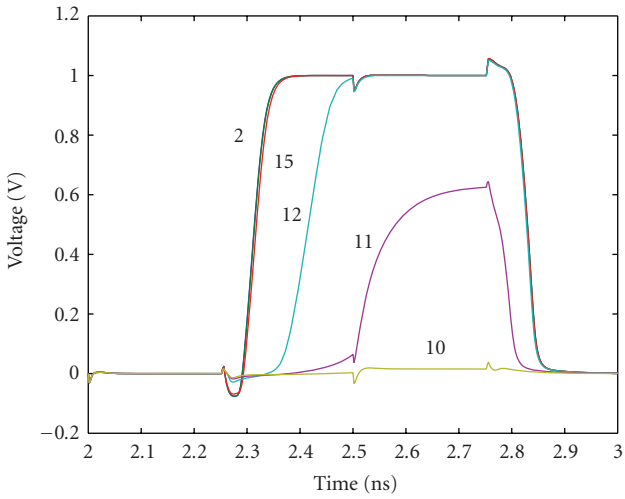


Figure 11: Output waveform for different repeater sizes.

Table 2: BER and power consumption of 130 nm technology.

N	s	D	BER	Power (mW)	FOM
4	3	4	1	1.0200	0
	4	4	0.9671	1.2147	9.9346E-6
	5	4	0.0050	1.3660	0.19324
	6	4	6.28E-08	1.4611	0.1603
	7	4	0	1.5424	0.13626
3	5	3	0.9997	1.1306	1.078E-11
	6	3	0.2317	1.2512	0.13368
	7	3	0.00107	1.3543	0.23168
	8	3	1.86E-09	1.4276	0.19844
	9	3	2.27E-13	1.4769	0.17922
2	7	2	0.9999	1.0244	6.577E-13
	8	2	0.8606	1.1123	0.0013919
	9	2	0.1711	1.1842	0.2425
	10	2	0.0064	1.2457	0.35882
	11	2	6.28E-09	1.2776	0.33908
1	13	1	0.1168	0.7948	1.3722
	15	1	3.06E-04	0.8550	1.5985
	16	1	6.22E-06	0.8789	1.4729
	17	1	2.84E-07	0.9016	1.3645
	19	1	1.12E-10	0.9421	1.1959

is considered and the selected clock frequency is 2 GHz. The circuits are implemented using Cadence tools and then simulated using Spectre circuit simulator. When calculating the BER, it is assumed that the standard deviation of all the timing parameters is 3% of their nominal values. Table 2 shows the simulation results for 130 nm technology, and Table 3 shows the data for 65 nm technology. It is observed that BER will decrease when the repeater size is enlarged or more wire segments are added. But the whole pipelined wire will consume more power in both cases. According to the figure of merit defined here the optimal number of wire segment and repeater size for 130 nm example are 1 and 15, respectively. That means, there is no need to insert any sequential element for this global interconnect in 130 nm technology. But for 65 nm technology, 5 flip-flops need to be inserted, and the repeater size should be 6 for optimal solution. This difference of the optimal number of flip-flops and the optimum size of repeater between 130 nm and 65 nm technology examples is mainly because of the vast difference of global wire resistance in the wires of two different technology nodes, which can be seen from Table 1. The resistance of 1 um global interconnect is only 0.098 Ω in 130 nm technology, but it is 0.475 Ω for 65 nm technology.

Table 3: BER and power consumption of 65 nm technology.

N	s	D	BER	Power (mW)	FOM
7	2	7	1	0.1264	0
	3	7	0.761	0.1976	0.7914
	4	7	0.223	0.2530	11.0758
	5	7	4.22E-02	0.3107	10.0710
	6	7	5.40E-06	0.3762	7.0988
6	4	6	1	0.2167	0
	5	6	9.69E-02	0.3006	11.067
	6	6	2.25E-05	0.3315	11.21
	7	6	2.08E-09	0.3591	8.8161
	8	6	3.15E-13	0.3711	7.9889
5	6	5	0.183	0.3382	6.3002
	7	5	9.96E-04	0.3710	8.7302
	8	5	5.40E-07	0.3884	7.6327
	9	5	1.05E-09	0.4076	6.6036
	10	5	2.01E-12	0.4191	6.0761
4	8	4	0.159	0.3413	7.4808
	9	4	0.0039	0.3622	10.4
	10	4	1.15E-04	0.3792	9.1667
	12	4	1.54E-08	0.4014	7.731
	15	4	1.41E-12	0.4172	6.8855

5. CONCLUSION AND FUTURE WORK

This paper presents an analysis of the circuit-level performance issues of wire pipelining. It is illustrated that increasing the number of inserted flip-flops and enlarging the size of repeaters will lower the BER at the cost of additional power consumption. Therefore, trade-off must be made between the solidity of a wire pipelining and the power consumption. It is also illustrated that with the increase of the number of inserted flops, the delay cycles of the pipelined interconnect will increase. A figure of merit is introduced to relate these conflicting performance metrics. A methodology is developed based on this figure of merit to find the optimal solution for an interconnect-pipelining scheme from both BER and power consumption point of view. The solution provides optimal number of flip-flops to be inserted and optimal size of repeater to be selected. Our ongoing attempt is to take area cost into consideration and try to find the best solution for a wire pipelining scheme considering other circuit-level issues, such as, the variability and unpredictability of capacitive and inductive coupling. Similar work can be done for latch-based wire pipelining.

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