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Research Article

Eight-Bit Semiflash A/D Converter

D. P. Dimitrov[1] and T. K. Vasileva[2]

[1] *Melexis, Bulgaria Ltd, Bulgaria*
[2] *Technical University of Sofia, Bulgaria*

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An 8-bit semiflash ADC is reported that uses a single array of 15 comparators for both the coarse and the fine conversion. Conversion is implemented in two steps. First, an estimate is made of the 4 most significant bits, which are then memorized in the output latch. Next, the remaining 4 bits are evaluated by the same array of comparators. The auto-zeroed comparators also perform the function of a sample-and-hold circuit. In the proposed 8-bit semiflash ADC, there are no sample-and-hold circuit, no DAC, no subtraction circuit, and no residue amplifier. As a result, a moderate conversion speed has been combined with a drastically reduced power consumption. The ADC was fabricated in a standard 0.6 μm double-poly, double-metal CMOS process. Experimental results show monotonic conversion with very low integral and differential nonlinearities. These features, combined with the ultra-low power consumption, make the proposed circuit very suitable for low-power mixed-signal applications.

1. INTRODUCTION

When there is a need for fast analog-to-digital conversion, flash (or parallel) A/D converters (ADC) are usually considered [1–7]. A block diagram of a flash ADC is shown in Figure 1. The unknown input voltage to be digitized is compared to a set of reference voltages. These reference voltages are usually provided by a resistor string. There is one comparator for each transition level. All the comparators connected to reference voltages lower than the unknown input voltage have "1" at their outputs and all comparators connected to reference voltages higher than the input voltage have "0" at their outputs. A simple combinatorial circuit decodes this "thermometer" code into binary code.

An N-bit converter must resolve 2^N input signal levels and there are 2^N-1 transitions between these levels, so the same number of comparators (i.e., 2^N-1) is needed to accomplish the A/D conversion. As the conversion is performed in one step, very fast conversion rates can be achieved. The only analog block in flash ADCs is the comparator, and the conversion accuracy is determined by the mismatch in the resistor string and the comparator performance. The main disadvantage of flash ADCs is related to the fact that the number of comparators increases exponentially with the number of bits. For example, 8-bit A/D conversion requires 255 comparators, and 10-bit A/D conversion requires 1023 comparators. The large number of comparators results in large size and high-power dissipation. Another potential problem is the increased input capacitance. Thus the circuit in front of the converter must be able to drive a large capacitive load. For these reasons, the flash ADC resolution is usually limited to 8 to 10 bits.

To reduce the number of comparators, two-step (semiflash) ADCs are usually used [1, 2, 7]. Conventional two-step ADCs require $2(2^{N/2}\text{-}1)$ comparators instead of 2^N-1 in the one-step flash converters. Thus for an 8-bit converter, 30 comparators are needed instead of 255. In the patented "average flash" technique [7], the ratio of the coarse comparators to the numbers of fine comparators is 1:4. As a result, less die area is occupied, less power is dissipated, and less capacitive loading is applied to the signal source; hence, faster speed capability is achieved.

Figure 2 shows the block diagram of a conventional two-step ADC [2].

The coarse flash ADC usually has a resolution of $N/2$ bits and determines the first most significant bits. Next, the input signal is reconstructed by means of an auxiliary digital-to-analog converter (DAC). To determine the remaining bits, this reconstructed voltage is subtracted from the input voltage, the residue voltage is thus available at the output of the subtraction circuit.

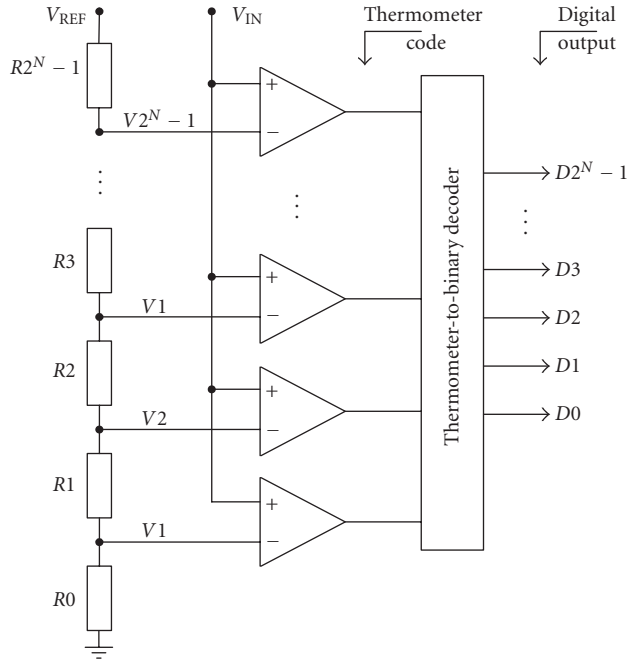

Figure 1: Flash ADC: block diagram.

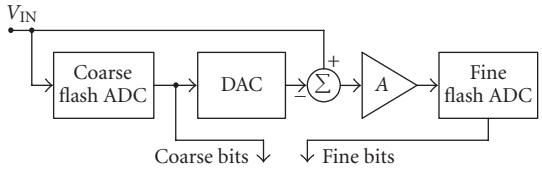

Figure 2: Conventional two-step flash ADC.

This residue voltage is then digitized by the fine flash ADC to determine the remaining less significant $N/2$ bits. To facilitate the fine ADC operation, a residue amplifier is put in front of it which amplifies the residue voltage $2^{N/2}$ times.

The most obvious disadvantage of two-step flash converters is the reduction of speed as the fine conversion cannot start until the coarse conversion has been completed. Another disadvantage is the reduced differential linearity, although experiments show that this is not such a great problem with low-resolution converters.

However, in contrast to the parallel A/D converters, there are many more error sources in the two-step converters—each of the analog blocks contributes to the total conversion error. The coarse converter, the auxiliary DAC, and the subtraction circuit must have N-bit accuracy, while the requirements for the residue amplifier and fine converter are less strict—they only need to be accurate up to $N/2$ bits. It is also worth mentioning that in some cases 2^{N-1}-2 comparators are still too power-hungry.

This article proposes a way to further reduce the number of comparators and to eliminate the need for DAC and residue amplifier. As a result, the die area and power consumption are dramatically reduced. Since there are no sample-and-hold circuit, no auxiliary DAC, and no residue amplifier in the proposed circuit, the number of error sources is reduced to minimum. The merits of the proposed circuit have been proved by experiments.

2. CIRCUIT DESCRIPTION

The main feature of the proposed scheme is that only a small number of comparators are used. If the same array of comparators is used twice [1]—first for the coarse conversion and next for the fine conversion—then only $2^{N/2}$-1 comparators are needed as compared to $2(2^{N/2}$-1) in the conventional semiflash ADC.

Thus, for 8-bit conversion, only 15 comparators are necessary as opposed to 31 comparators in a conventional two-step ADC or 255 comparators in a true parallel ADC.

The converter consists of a resistor array, a comparator array of 15 comparators, a thermometer coder, output latches, and a control unit (Figure 3).

During the coarse conversion, the reference voltage is divided into 16 ranges and an estimate is made in which range the input signal fits. The number of the segment is represented by the most significant bits. Next, in the fine conversion step, the control unit connects the same comparators to the resistor taps of one particular segment (defined in the previous step) in order to obtain the least significant bits. Intermediate conversion results are stored in the output latch. After the conversion has been completed, an end-of-conversion signal is activated to show that the output data is valid.

3. RESISTOR ARRAY

The reference levels for the comparators are generated by an array of 256 resistors organized in 16 rows with 16 poly1 resistors in each row. There are 15 switches connected to the interrow taps and each row has 15 switches associated to the interresistor taps in it (Figure 4).

During the coarse conversion, the switches are connected to the inter-row taps, hence V_{IN} is compared to the coarse reference voltages.

During the fine conversion step, the Allrow signal is low while one of the ROWSEL0...ROWSEL15 signals is activated, thus connecting the comparators to the resistors in one particular row which has been chosen by the control unit. Now V_{IN} is compared to the fine reference voltages.

The size and value of the unit resistor are a compromise between the accuracy desired and the need to keep the die area small. In addition, low impedance of the resistor array is highly desirable so that the input capacitances of the comparators are quickly recharged. As the resistor array defines the set of reference voltages which are compared to the unknown input voltage, the resistor mismatch defines the integral nonlinearity of the converter. The maximum error is expected in the middle of the scale. The used poly1 resistor feature Pelgrom matching coefficient of some 10% x μm. For the chosen unit resistor size of 20/4 μm (L/W) and value of

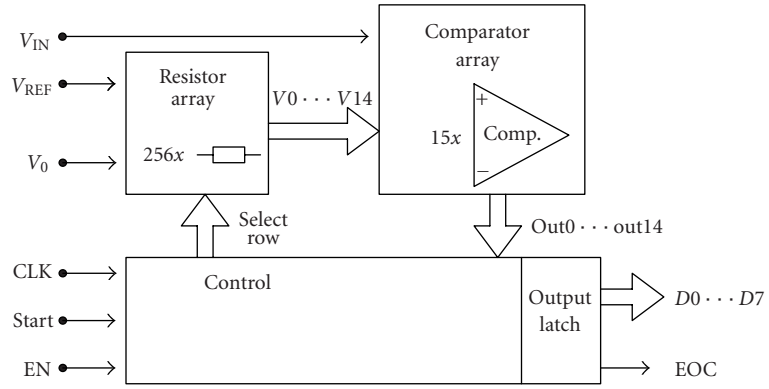

Figure 3: The proposed two-step flash ADC.

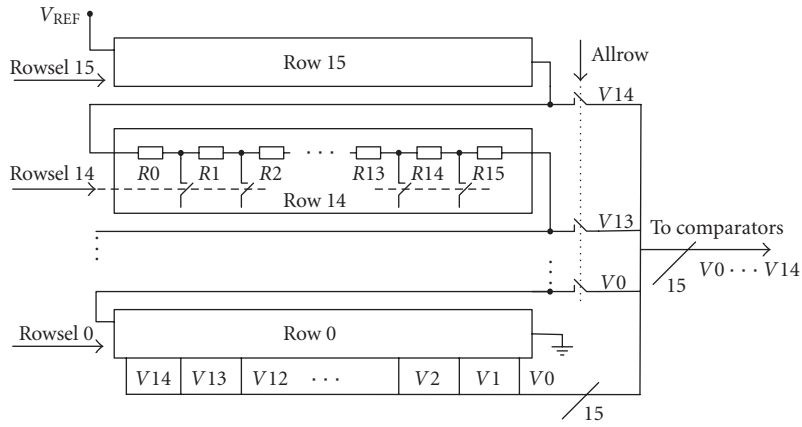

Figure 4: The resistor array.

82.6 Ω, the expected maximum error in the middle of the range is

$$\begin{aligned} \mathrm{INL}_{\mathrm{MAX}} &= \left(\frac{\Delta R}{R}\right)_{\mathrm{MAX}} = 3 \times \sigma_R \\ &= 3 \times \frac{10\%}{\sqrt{128 \times 4 \times 20}} \\ &= 0.3\% = 0.76\,\mathrm{LSB}. \end{aligned} \tag{1}$$

Every effort has been made during layout generation to ensure good resistor matching. There is a ring of dummy resistors and the switches and interconnect wires are placed in a way that guarantees that all resistors are surrounded by identical structures.

The result of (1) well agrees with the static INL measured, shown in Figure 10.

4. COMPARATOR

The comparator performance is of crucial importance for the overall A/D conversion accuracy.

The CMOS inverter [8] is not suitable for high-performance circuits. It features poor power supply rejection and needs too much current in order to attain reasonable speed. Regenerative comparators combine good sensitivity, high speed, and moderate power consumption, but they are not suitable for this particular application because the two comparison steps follow each other immediately, without an auto-zero phase in between.

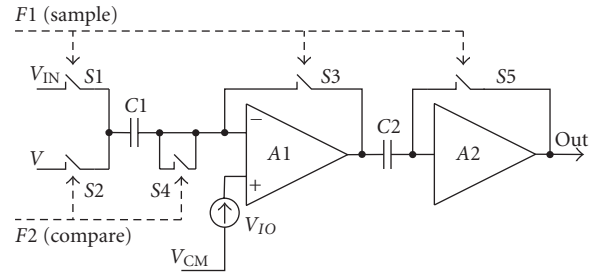

Figure 5: The comparator.

To overcome the above obstacles, a two-stage comparator is used with capacitive coupling (Figure 5). The first stage is an auto-zeroed differential comparator and the second stage is a simple clocked inverter.

During the first step (the sampling phase), switches S1, S3, and S5 are closed; S2 and S4 are open; and the voltage at the output and the inverting input is

$$V_{\mathrm{OUT}}^{I} = V^{-} = (V_{\mathrm{CM}} + V_{\mathrm{IO}\,1}) \times \frac{A_{V1}}{1 + A_{V1}}. \tag{2}$$

Hence the coupling capacitor C1 is charged to

$$V_{C1} = (V_{\mathrm{CM}} + V_{\mathrm{IO}\,1}) \times \frac{A_{V1}}{1 + A_{V1}} - V_{\mathrm{IN}}. \tag{3}$$

Thus each comparator also performs the function of a sample-and-hold circuit. During the subsequent conversion steps, S1, S3, and S5 are open, S2 and S4 are closed, and the output of the comparator is

$$V_{\mathrm{OUT}}^{II} = A_{V1} \times (V_{\mathrm{CM}} + V_{\mathrm{IO}\,1} - V - V_{C1}). \tag{4}$$

After replacing (3) in (4) and rearranging the expression, the output of the first stage can be expressed as

$$V_{\mathrm{OUT}}^{II} = A_{V1} \times (V_{\mathrm{IN}} - V) + \frac{V_{\mathrm{CM}} \times A_{V2}}{1 + A_{V1}} + \frac{V_{\mathrm{IO}} \times A_{V2}}{1 + A_{V1}}. \tag{5}$$

Thus, the output of the first comparator stage is the same as if the input offset voltage were $1 + A_{V1}$ times smaller.

The first comparator stage is shown in Figure 6. The N-MOS differential pair is sized 20.6/1.2 μm (W/L) with load transistors sized 4/1 μm (W/L). The tail current through M5 is 20 μA.

The input offset voltage can be expressed as [7]

$$V_{\mathrm{IO}} = \left(\begin{array}{c} \left(\dfrac{3 \times A_{\mathrm{VTN}}}{\sqrt{W_1 \times L_1}} \right)^2 + \left(\dfrac{gm3}{gm1} \times \dfrac{3 \times A_{\mathrm{VTP}}}{\sqrt{W_3 \times L_3}} \right)^2 \\ + \left(\dfrac{I_{M1}}{gm1} \times \dfrac{3 \times A_{\mathrm{BETAP}}}{\sqrt{W_3 \times L_3}} \right)^2 \end{array} \right)^{1/2}, \tag{6}$$

where A_{VTN} and A_{VTP} are the threshold voltage matching coefficients of the N-MOS and P-MOS transistors, respectively, and A_{BETAP} is the beta matching coefficient of the P-MOS transistors. If the symbols in (6) are replaced with the numbers given in the process specification, (6) can be solved to yield the input offset voltage:

$$V_{\mathrm{IO}} = \left(\begin{array}{c} \left(\dfrac{3 \times 19\,\mathrm{mV} \cdot \mu\mathrm{m}}{\sqrt{20.6\,\mu\mathrm{m} \times 1.2\,\mu\mathrm{m}}} \right)^2 \\ + \left(\dfrac{56\,\mu\mathrm{S}}{176\,\mu\mathrm{S}} \times \dfrac{3 \times 19\,\mathrm{mV} \cdot \mu\mathrm{m}}{\sqrt{4\,\mu\mathrm{m} \times 1\,\mu\mathrm{m}}} \right)^2 \\ + \left(\dfrac{10\,\mu\mathrm{A}}{176\,\mu\mathrm{S}} \times \dfrac{3 \times 2\%}{\sqrt{4\,\mu\mathrm{m} \times 1\,\mu\mathrm{m}}} \right)^2 \end{array} \right)^{1/2}, \tag{7}$$

$$V_{\mathrm{IO}} = 14.45\,\mathrm{mV}.$$

The simulated small-signal gain of the first stage is 42.27 dB (130 V/V) and according to (5), the compensated input offset voltage is reduced to

$$V_{\mathrm{IO}}^{\mathrm{COMPENSATED}} = 14.45\,\mathrm{mV} \times \frac{1}{1 + 130} = 0.11\,\mathrm{mV}. \tag{8}$$

The auto-zeroing technique allows for small-size differential pairs to be used while keeping the overall input-referred offset voltage rather small.

Charge injection in the S3 switch causes two additional error voltages. The first is due to the channel charge injected into the drain and source terminals during switch turn-off. The voltage change at the input of the comparator is

$$\Delta V_{\mathrm{CH}} = -\frac{Q_{\mathrm{CH}}/2}{C_1} = \frac{C_{\mathrm{OX}} W_3 L_3 (V_{\mathrm{DD}} - V_{\mathrm{CM}} - V_{\mathrm{TN}})}{2C_1}. \tag{9}$$

And replacing the actual transistor sizes and voltages, the following value is found for ΔV_{CH}:

$$\Delta V_{\mathrm{CH}} = -\frac{2.76\,\mathrm{fF}/\mu\mathrm{m}^2 \times 0.96\,\mu\mathrm{m}^2 \times 1.64\,\mathrm{V}}{2 \times 1.5\,\mathrm{pF}}, \qquad \Delta V_{\mathrm{CH}} = -1.45\,\mathrm{mV}. \tag{10}$$

The second error voltage is due to the gate-drain overlap capacitance C_{OV} of S3:

$$\Delta V_{\mathrm{OV}} = \Delta V_G \times \frac{C_{\mathrm{OV}}}{C_1 + C_{\mathrm{OV}}} = \frac{-5\,\mathrm{V} \times 0.608\,\mathrm{fF}}{1.5\,\mathrm{pF} + 0.608\,\mathrm{fF}}, \qquad \Delta V_{\mathrm{OV}} = -2.02\,\mathrm{mV}. \tag{11}$$

The S4 dummy switch is included to compensate for the additional charge-injection errors. S4 is controlled by the complementary clock F2. Since the width of S4 equals half the width of S3 and the channel lengths of S3 and S4 are equal, the charges injected in the input of the comparator during commutation are equal in magnitude but with opposite signs and compensate for each other. The F1 and F2 clocks are nonoverlapping, so at no time are the S1, S3, S5, and S2, S4 switches simultaneously open.

As the signal level at the input of the second stage is high enough, no charge injection cancellation is necessary for S5. Moreover, due to the capacitive coupling between the two comparator stages, the input offset voltage of the second stage is cancelled in the same way as the offset of the first stage.

5. THERMOMETER CODER

A simple thermometer coder with bubble error removal is used [5] (Figure 7).

Indeed, in contrast to Figure 1, the input voltage is here applied to the inverting comparators inputs while the reference voltages are connected to the noninverting inputs but this is merely a matter of coding and affects neither the principle of operation nor ADC performance. Ideally, the outputs of the comparators should be a thermometer code with a single transition (e.g., 000011). The thermometer decoder produces a "0" at the transition point …000->111… (Figure 7(a)). However, due to noise or finite comparator speed, a solitary "1" or "0" can sometimes occur near the transition point. There must be at least two 1s above a 0 to determine the transition point. If there is a stray 1or 0, it is suppressed (Figure 7(b)). Indeed, this circuit can only suppress a stray 1 (0) one place away from the transition point. It

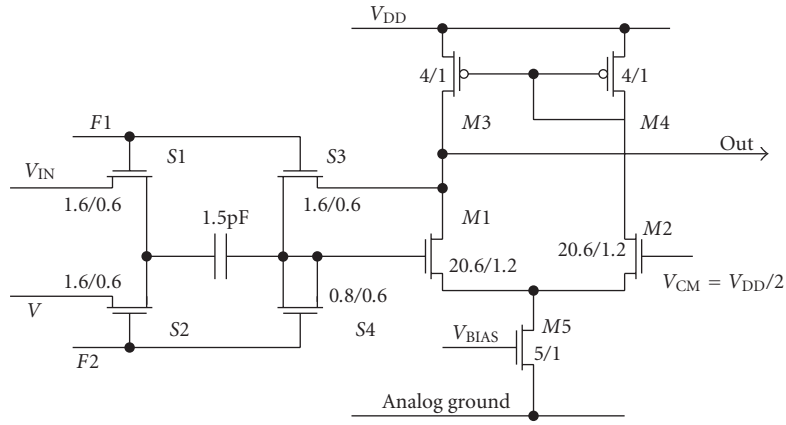

Figure 6: The comparator's first stage.

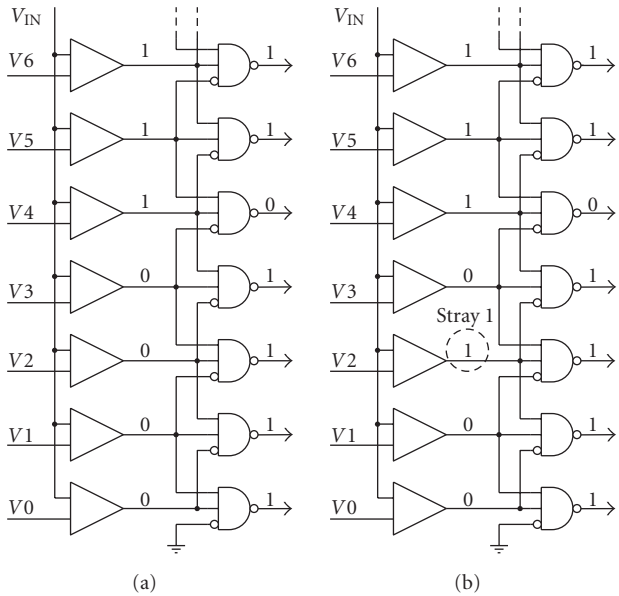

Figure 7: Bubble error removal.

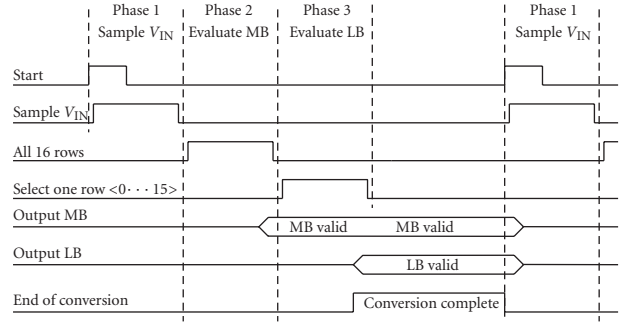

Figure 8: ADC time diagram.

cannot suppress a stray 1 (0) two places away from the transition point. Fortunately, such big errors are quite unlikely to occur.

6. SEMIFLASH ADC OPERATION

Conversion is divided into three phases (Figure 8) initiated by the START signal.

During phase 1 (sample and offset cancellation), the input signal plus input offset voltages are stored in the coupling capacitors (Figure 6: S1, S3, and S5 closed; S2 and S4 open).

During the second phase (coarse conversion), comparators are connected to the fifteen taps between the resistor rows—the four most significant bits are estimated. S1, S3, and S5 are open and S2 and S4 are closed. A comparison is made between the memorized value of V_{IN} and the interrow tap voltages. The control unit decides which row is closest to the memorized input voltage, and this row is to be connected to the comparator bank during the fine conversion phase. At the end of phase 2, the four most significant bits are loaded at the output latch and after they have been memorized, the comparators are disconnected from the row taps.

Finally, in phase 3 (fine conversion), the comparators are connected to the taps in the row which has been selected in phase 2. The resulting thermometer code is decoded and stored as the lower 4 bits in the output latch. At the end of phase 3, an end-of-conversion signal is activated and the data in the output latch is valid and available for reading; comparators switch to sample and offset cancellation mode. The converter remains in this state until a new conversion is initiated. If the START signal is permanently kept high, conversion cycles follow in succession.

7. EXPERIMENTAL RESULTS

The proposed circuit was implemented in standard 0.6 μm double-metal, double-poly CMOS process (Figure 9). At the bottom of the die, the resistor array can be seen with the switches in between the resistors, poly1 resistors are used with N-MOS switches connected to the resistor string taps.

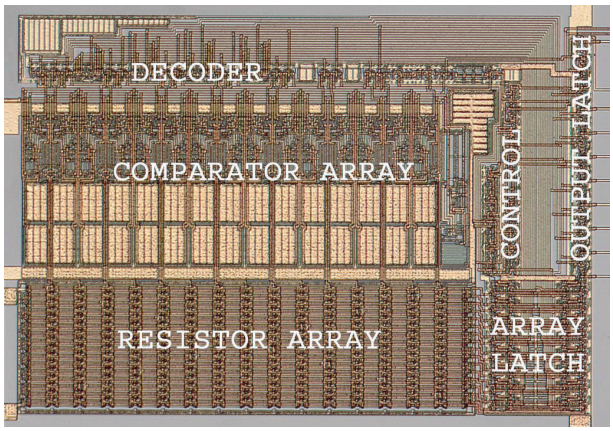

Figure 9: Die photograph.

The use of N-MOS switches limits the reference voltage to 1.25 V. On the right side of the resistor array are the latches that control the switches. Immediately above the resistor array are the comparators. Next to the comparators are the decoders. Standard digital cells from the low-power digital library provided by the silicon foundry have been used to implement the digital circuitry.

Full custom layout for both the digital and the analog part, ensures a low die area, short signal paths, and minimum noise pick-up. Special care has been taken in the layout phase to ensure perfect symmetry and good device matching in the analog part, as well as the reduction of noise pick-up and interference by means of proper floor-planning and guard rings. Bypass CMOS capacitors connected to the supply rails are inserted in the few empty spaces to ensure better power supply decoupling. Experimental results were obtained at a sampling rate of 330 ksamples/s, a supply voltage of 5 V, and a temperature of 25^{o}C. Experiments at 125^{o}C show only negligible changes in the differential nonlinearity (DNL) and integral nonlinearity (INL) curves. The reference voltage is fixed at 1.25 V.

Since all resistors in the string are equal, a systematic offset of 0.5 LSB is observed (not shown in the figures).

The INL versus output code curve (Figure 10) features the bent shape which is typical to resistor strings. The increased differential nonlinearity which is expected in two-step flash converters is only barely noticeable at transitions 15-16; 31-32, 63-64, and so forth (Figure 11). Since both INL and DNL are below 0.5 LSB, the conversion is monotonic.

To estimate the converter's ability to process signals in the real world, some dynamic tests were also performed [9]. Essentially the same acquisition kit was used for both statistical analysis and fast Fourier transform (FFT) analysis.

A sine input wave with a frequency of 10 kHz was applied. Batches of 32 768 samples were collected for statistical analysis and batches of 8 192 samples were collected for FFT analysis. Data were processed by means of Matlab. The DNL obtained through histogram analysis is shown in Figure 12 and the single-tone FFT plot is shown in Figure 13. The noise

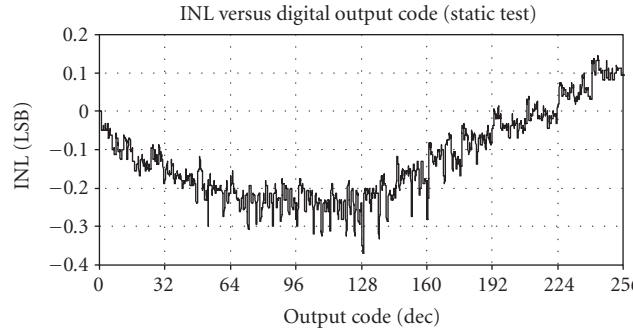

Figure 10: INL measured in static mode.

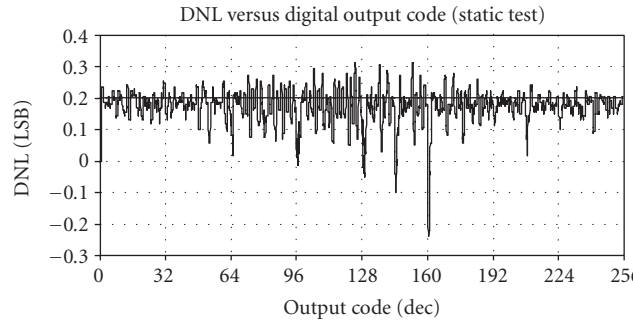

Figure 11: DNL measured in static mode.

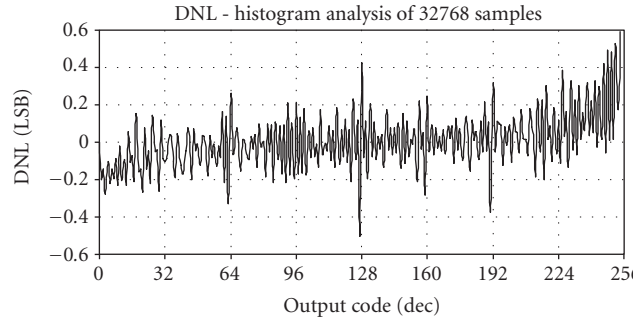

Figure 12: DNL in dynamic mode—histogram analysis of 32 768 samples.

floor in the FFT plot appears to be somewhat elevated due to noise introduced by the test kit itself.

Table 1 summarizes the measured performance of the proposed A/D converter.

There is a clear compromise between speed and consumption—the proposed design has the lowest consumption: a mere 3.4 mW as opposed to 200 mW reported in [1]; 150 mW reported in [3]; and 540 mW reported in [8].

The price paid for the low power is the low conversion rate: 330 kS/s as compared to 16 MS/s in [1] and 1300 MS/s reported in [4].

The differential and integral nonlinearities of 0.3 LSB are half as low as the values of 0.6 LSB and 1 LSB, respectively,

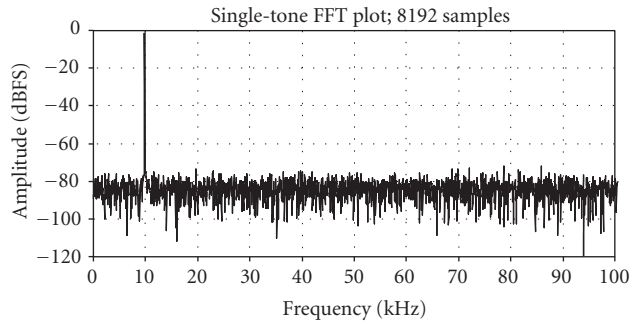

Figure 13: Dynamic test: single tone FFT plot.

Table 1: Measured semiflash ADC performance.

Parameter	Value
Resolution (static)	8 bit
Integral nonlinearity (static)	0.3 LSB
Differential nonlinearity (static)	0.3 LSB
Differential nonlinearity (dynamic)	0.5 LSB
THD	-68 dB
SNDR	46 dB
ENOB	7.3
Conversion rate	330 kS/s
Input capacitance	23 pF
Reference voltage	1.250 V
Load to the reference source	21 kΩ
Size	$550 \times 380\,\mu$m
Supply voltage	5 V
Power consumption	3.4 mW

reported in [1], and close to the values of 0.5 LSB and 0.8 LSB reported in [7].

The proposed design also features the quite small die area—0.21 mm^2 versus 3 mm^2 [1] and 1.2 mm^2 [3].

8. CONCLUSION

An 8-bit semiflash A/D converter has been designed and manufactured in a standard 0.6 μm double-metal, double-poly CMOS process. In contrast to the common approach in the design of semiflash SA/D converters, the emphasis was here put on the ultra-low power consumption rather than on the high speed. The proposed circuit topology has proved to be an effective way to dramatically reduce the power consumption and die area while maintaining high accuracy and low nonlinearity errors. The proposed semiflash A/D converter is very suitable for low-power, mixed-signal applications.

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