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Research Letter

Current Tunnelling in MOS Devices with Al_2O_3/SiO_2 Gate Dielectric

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With the continued scaling of the SiO_2 thickness below 2 nm in CMOS devices, a large direct-tunnelling current flow between the gate electrode and silicon substrate is greatly impacting device performance. Therefore, higher dielectric constant materials are desirable for reducing the gate leakage while maintaining transistor performance for very thin dielectric layers. Despite its not very high dielectric constant (~10), Al_2O_3 has emerged as one of the most promising high-k candidates in terms of its chemical and thermal stability as its high-barrier offset. In this paper, a theoretical study of the physical and electrical properties of Al_2O_3 gate dielectric is reported including I(V) and C(V) characteristics. By using a stack of Al_2O_3/SiO_2 with an appropriate equivalent oxide thickness of gate dielectric MOS, the gate leakage exhibits an important decrease. The effect of carrier trap parameters (depth and width) at the Al_2O_3/SiO_2 interface is also discussed.

1. INTRODUCTION

From the beginning of MOS devices technology, SiO_2 has been used as gate oxide because of its stable SiO_2/Si interface as well as its electrical isolation property. But with the rapid scaling down of CMOS devices, SiO_2 gate oxide thickness reaches its physical limits leading to high leakage current. The SiO_2 gate dielectric thickness is projected to be below 1 nm and the power supply (V_{dd}) should fall within 0.8 and 1.8 V. In this situation, the gate leakage currents due to tunnelling become very high. Therefore, it has become necessary to use high-k gate dielectrics in order to meet the strict requirements on leakage current and equivalent oxide thickness (EOT) such as HfO_2 [1, 2], ZrO_2 [3–6], TiO_2 [7], and Al_2O_3 [8, 9]. Unfortunately, for most high-k materials, the higher dielectric constant comes at the expense of narrower band gap, 5-6 eV [10], that is, lower barrier height for tunnelling and the lower barrier height tends to compensate the benefit of the higher dielectric constant (thicker dielectric layer). Nevertheless, for many high-k materials, the net effect is a reduced leakage current. Needless to say, the search for the appropriate high-k to replace conventional SiO_2-based gate dielectrics is an important task. HfO_2 has emerged as one of the most promising high-k candidates due to its relatively high dielectric constant (~25) and large band gap (~5.8 eV). However, its physical and electrical properties suffer from its crystallisation at high temperature during post deposition annealing. Moreover, HfO_2 is a solid state electrolyte for oxygen at high temperature. Thus, high temperature will lead to fast diffusion of oxygen through the HfO_2 resulting in the growth of uncontrolled low-k interfacial layers (SiO_2) limiting the equivalent oxide thickness (EOT) [11]. Nevertheless, and despite its relatively lower dielectric constant, Al_2O_3 appears as an extremely promising candidate in terms of its chemical and thermal stability as well as its high-barrier offset. Al_2O_3 is also interesting for its high crystallisation temperature and thus it is compatible with conventional process of integrating complementary MOS devices, which involves high temperatures above 1000°C [12]. However, the silicon substrate and high-k interface degrade the electron and hole mobility. Mobility directly affects the drain current of the transistors and therefore switches the speed of the circuits.

In this paper, and to overcome the problem of degradation mobility, we use an extremely thin SiO_2 layer with the high-k dielectric. In this case, achieving a thin EOT is

very challenging. We propose an Al_2O_3/SiO_2 gate dielectric. The SiO_2 layer is needed in order to separate the carrier in MOSFET channel from the electric field fluctuations caused by soft phonons in the dielectric and decreasing the carrier mobility μ. With such double-layer structure, we can make the ratio μ/EOT high enough to guarantee a sufficiently high speed of the device [13]. The physical and electrical properties of based MOS devices are investigated. The effect of carrier trap parameters (depth and width) at the Al_2O_3/SiO_2 interface is also discussed. The paper is organised as follows: after a brief introduction and the description of the modelled structure in Sections 1 and 2, in Section 3, I(V) and C(V) characteristics of MOS devices with Al_2O_3/SiO_2 gate dielectrics are investigated and discussed. We will focus especially on the effect of carrier trap parameters at the Al_2O_3/SiO_2 interface. Conclusions are given in Section 4.

2. MODELLING

So far, some models were proposed to study the tunnelling mechanisms [14–16]. In fact, understanding the carrier transport mechanisms is helpful to study the electrical and reliability characteristics. Furthermore, capacitance-voltage (C-V) measurement is one of the most convenient methods to characterise the MOS structure. Well known and easy to perform, it provides useful information such as flat band, thresholds, substrate doping level, oxide thickness, and interface or oxide trap density.

Within effective-mass approximation, our calculations in this study are based on a self-consistent solution of the Schrödinger and Poisson equations. The quantised energy levels E_i and their corresponding electronic wave functions ψ_i satisfy the Schrödinger equation while the Hartree approximation for the confining potential $V_H(z)$ is obtained by solving the Poisson equation. In the Schrödinger equation,

$$-\frac{\hbar^2}{2}\nabla\left(\frac{1}{m^*(z)}\nabla\Psi_i(z)\right)+V(z)\Psi_i(z)=E_i\Psi_i(z), \quad (1)$$

m^* represents the electron effective mass. The potential $V(z)$ includes the band diagram discontinuities at interfaces between layers $V_0(z)$ and the Hartree term due to the electrostatic potential energy $V_H(z)$. The Poisson equation, which yields the above-mentioned Hartree term, is given by

$$\frac{d}{dz}\left(\varepsilon_0\varepsilon_r(z)\frac{d}{dz}\right)V_H(z)=q[N_D^+-N_A^-+n(z)+p(z)], \quad (2)$$

where q is the electronic charge, $\varepsilon_r(z)$ is the position-dependant dielectric constant, ε_0 is the permittivity of vacuum, N_D^+ and N_A^- refer to the ionised donor and acceptor concentration, and $n(z)$ and $p(z)$ are the free electron and hole concentration, respectively. These free-carrier concentrations are obtained by the following equations:

$$n(z)=\frac{m^*kT}{\pi\hbar^2}\sum_{ie}\ln\left[1+\exp\left(\frac{E_F-E_{ie}}{kT}\right)\right]|\Psi_{ie}(z)|^2,$$

$$p(z)=\frac{m^*kT}{\pi\hbar^2}\sum_{ip}\ln\left[1+\exp\left(\frac{E_{ip}-E_F}{kT}\right)\right]|\Psi_{ip}(z)|^2, \quad (3)$$

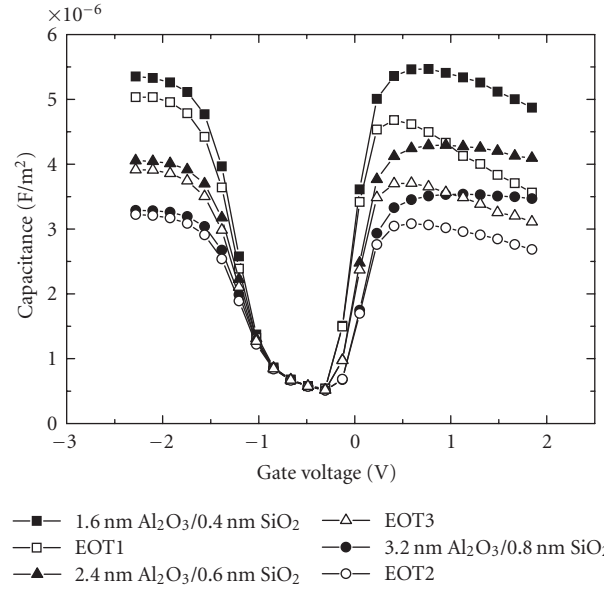

Figure 1: C-V simulations for three different thicknesses of Al_2O_3/SiO_2 stack (solid symbols). For each width, C-V characteristic is also simulated for the same EOT (resp., 1.08 nm, 2.16 nm, and 3.24 nm SiO_2).

where E_{ie} and E_{ih} are the ith eigenvalues for electrons and holes, respectively, and E_F refers to the Fermi level which is determined by solving numerically the electro neutrality equation.

Then, the tunnelling current and the capacitance of the modelled structure are simulated as described in [17]. Numerically, the solution of the one dimensional Schrödinger-Poisson equation is based on a finite difference scheme.

Capacitors with Al_2O_3-based gate dielectric modelled in this paper consist of a p-Si substrate of 100 nm, a stack of (1.6 nm Al_2O_3)/(0.4 nm SiO_2) as gate dielectric, and a 10 nm n-poly Si layer. The conduction band offsets ΔE_c of Al_2O_3, HfO_2, and SiO_2 on Si used in this work are 2.8 eV, 2.0 eV, and 3.1 eV, respectively. The permittivities considered are 24, 10, and 3.9 for HfO_2, Al_2O_3, and SiO_2, respectively. The p-substrate doping is $N_A = 3\times10^{17}$ cm^{-3}. The gate (n+poly Si, $N_D = 1\times10^{20}$ cm^{-3}) is biased from accumulation to inversion regimes. We have taken m^*= 0.17, 0.35, [18] and 0.6 m_0 [19] units for HfO_2, Al_2O_3, and SiO_2, respectively (m_0 is the free-electron mass).

3. RESULTS AND DISCUSSION

Figure 1 represents the capacitance versus the gate voltage for n-MOS modelled structure. C-V curves are shown for different dielectric stacks: Al_2O_3(1.6 nm)/ SiO_2(0.4 nm); Al_2O_3(2.4 nm)/SiO_2(0.6 nm); Al_2O_3(3.2 nm)/SiO_2(0.8 nm). One can note a positive voltage shift (≈200 mV) in the characteristics with the dielectric thickness increase. As it is known, thin oxide permits a decrease of the programming voltage. The capacitance in accumulation and in strong inversion is dominated by the oxide capacitance. In n-MOS, the capacitance value is more thickness sensitive in strong

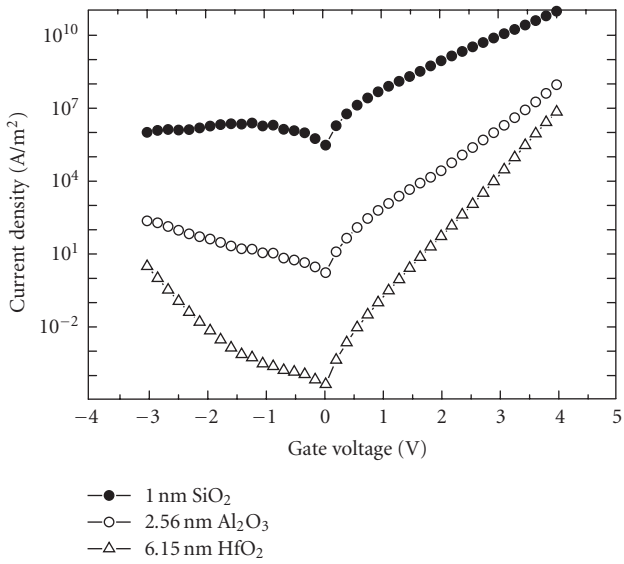

FIGURE 2: I-V simulations on SiO_2 (1 nm), Al_2O_3 (2.56 nm), and HfO_2 (6.15 nm) NMOS barriers (with the same EOT: 1 nm).

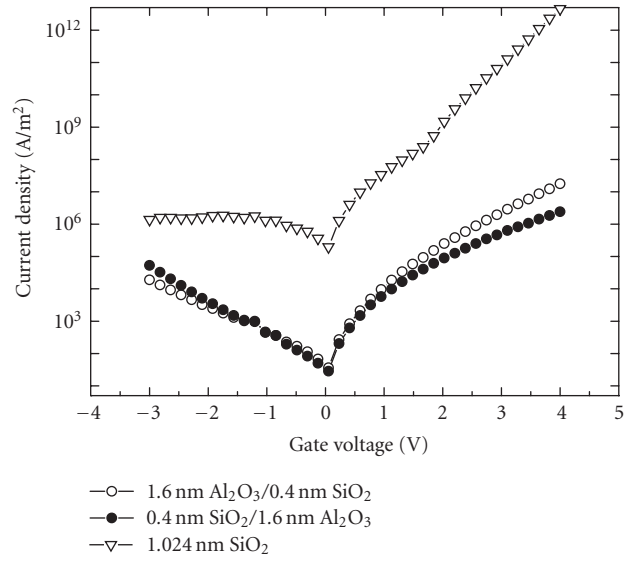

FIGURE 3: I-V simulations on Al_2O_3/SiO_2 and SiO_2/Al_2O_3 dielectric stacks for NMOS with the EOT (1 nm). I-V simulation on Al_2O_3 dielectric is given for comparison.

inversion. We have also simulated the tunnelling current biased in accumulation and inversion regimes with single layer of dielectric. In fact, it has been demonstrated that Al_2O_3 can be deposited uniformly directly on Si without an interlayer [20]. A comparison of Al_2O_3 material with SiO_2 and HfO_2 is given in Figure 2 for the same equivalent thickness (EOT) (t_{SiO_2} = 1 nm, $t_{Al_2O_2}$ = 2.56 nm, and t_{HfO_2} = 6.15 nm). The leakage current in the first structureis lower than that of SiO_2 because of Al_2O_3 constant which is higher than that of SiO_2 [21], though not as much as in the case of HfO_2. Nevertheless, and as shown in Figure 3, the n^+-polysilicon-(1.6 nm Al_2O_3)/(0.4 nm SiO_2)-p-Si structure exhibits two-order magnitude and lower gate leakage than n^+-polysilicon-(0.4 nm SiO_2)/(1.6 nm Al_2O_3)-p-Si and three decades lower than n^+-polysilicon- SiO_2(1.024 nm)-p-Si for the same EOT and for V_g lower than −2 V in the accumulation. In fact, for Al_2O_3/SiO_2 gate dielectrics that have different k values and conduction band offsets, the tunnelling current is lower when the tunnelling occurs firstly in the high-k dielectric film (n^+-polysilicon-Al_2O_3/SiO_2-p-Si) than in the low-k one (n^+-polysilicon-SiO_2/Al_2O_3-p-Si) in the accumulation for gate voltage V_g lower than −2 V. For direct-tunnelling region, similar gate leakage can be obtained for the two stacks. So, the tunnelling current is probably lower than other contributions which appear for high gate voltage.

However, many problems related to electron traps which shift the threshold voltage V_{th} reduce mobility through coulombic scattering and can cause breakdown by forming a conduction path. Then, the device efficiency is considerably reduced. In the purpose of taking into account this phenomenon, we have modelled a trap centred at the Al_2O_3(1.6 nm/SiO_2(0.4 nm) interface by a thin quantum well; we can vary its depth, width, or mass. The origin for depth is taken at the bottom of Si conduction band. Figure 4 depicts the tunnelling current for −2 eV trap depth and widths of 0.1 nm, 0.15 nm, 0.20 nm, and 0.25 nm. The gate

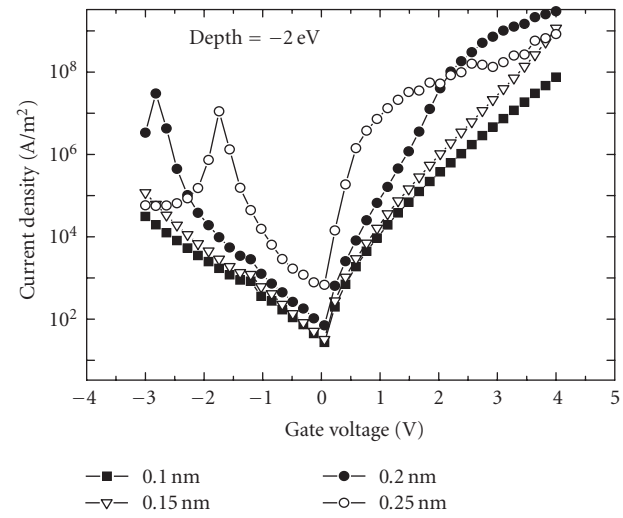

FIGURE 4: I-V simulations on Al_2O_3/SiO_2 dielectric stacks with carrier trap for different trap widths.

current increases with trap thickness due to the higher transparency. However, for high trap width value (0.25 nm), the I-V curve shows a reduction with oscillations due to the existence of a negative resistance. In fact, when the trap thickness increases, we pass progressively from capacity I-V characteristic to tunnel diode. Some of the trapped electrons face a triangular barrier for the emission process, giving rise to an additional peak in the trap occupancy near the gate side of the dielectric. Figure 5(a) compares I-V curves for different trap depths of (−2 eV, −1 eV, and −0.5 eV) with 0.1 nm trap width. As shown, the gate current hardly increases with the trap depth in the accumulation region, in the inversion one; the current has the same value for low gate voltage. When using a higher mass of material constituting the trap, the gate

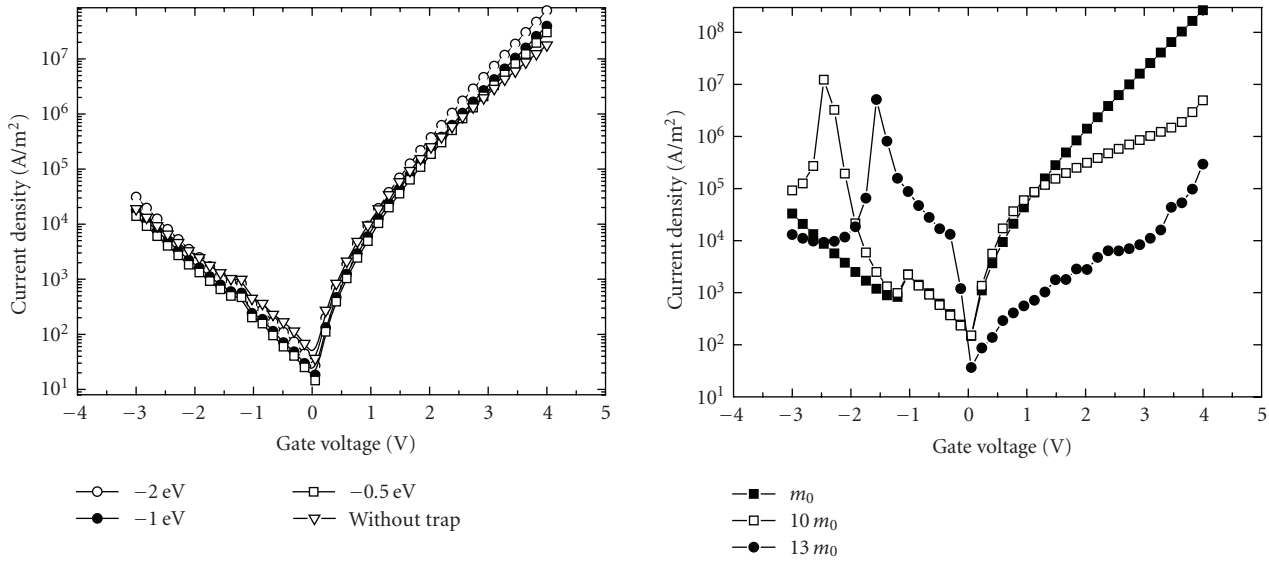

FIGURE 5: I-V simulations on Al_2O_3/SiO_2 dielectric stacks with carrier trap for (a) different depths (−2 eV, −1 eV, −0.5 eV, and without trap) and (b) different masses (m_0, 10 m_0, and 13 m_0) of material constituting the trap.

current increase is more sensitive and a region of negative resistance appears corresponding to an alignment of levels for carrier in the Si region and the trap one (see Figure 5(b)). These oscillations for high bias are due to the fact that in this regime the energy barrier has a triangular shape which gives rise to an oscillating wave function, in contrast to the decaying wave function for a trapezoidal barrier. One can note the kink in I(V) curves for gate voltage $-1\text{V} \leq V_g \leq 0$ with high leakage current values, this is probably due to the generation of carriers in the poly gate.

4. CONCLUSION

In this paper, and to reduce the defect density, an SiO_2 interlayer helps to improve Si-Al_2O_3 interface quality and therefore device characteristics. By using a stack of Al_2O_3/SiO_2 as gate dielectric with an equivalent oxide thickness of 1.024 nm (1.6 nm Al_2O_3 and 0.4 nm SiO_2) of gate dielectric MOS, the gate leakage exhibits an important decrease. In fact, Al_2O_3 exhibits gate leakage much lower than that of conventional SiO_2 of the same equivalent electrical thickness (capacitance) and good interface quality.

In the aim to simulate a realistic device, taking into account the trap carriers at the interface is essential. The gate current seems to be indifferent with the change in trap depth for low masses of material constituting the trap. However, when using higher mass values or larger traps, a large injection current is observed showing oscillations due to the existence of a negative resistance.

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