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*Research Article*

# Built-in Test Enabled Diagnosis and Tuning of RF Transmitter Systems

**Vishwanath Natarajan, Rajarajan Senguttuvan, Shreyas Sen, and Abhjit Chatterjee**

*School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332, USA*

Correspondence should be addressed to Vishwanath Natarajan, vishwa@ece.gatech.edu

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Built-In RF test is a challenging problem due to the need to measure the values of complex test specifications on-chip with the precision of external RF test equipment. BIT techniques are necessary for guiding system adaptation during field operation. Prior research has demonstrated that embedded RF sensors can generate significant information about RF circuit performance. In this paper, we propose a test methodology that enables efficient BIT and BIT-enabled tuning of RF systems. A test generation approach is developed that co-optimizes the applied test stimulus, the type of embedded sensors, and the system response capture mechanisms for maximal accuracy of the BIT procedure. This BIT technique is also used to perform diagnostic testing of the transmitter. The information gathered from diagnosis is used to tune the transmitter for improved performance. Simulation results demonstrate that BIT-assisted diagnosis and tuning can be performed with good accuracy using the proposed methodology.



## 1. INTRODUCTION

Wireless communications for both mobile and in-office (point-to-point communication) applications is undergoing a revolution due to the proliferation of different communication standards spanning diverse communication bandwidths. In addition, to the use of scaled CMOS technologies for high frequency wireless technologies running into the 10's of GHz (seemingly impossible till a few years ago) are posing daunting technological challenges both in design and manufacturing test. A complex multiband, multiradio system may integrate FM radio (100 MHz), RFID (13 MHz), Digital TV (800–1600 MHz), GPS (1.5 GHz), Bluetooth (2.4 GHz), Wi-Fi (2.4–5 GHz), 802.11 (2.4–5 GHz), Wi-Max (2.5–3.5 GHz), and UWB (3–10 GHz) using a combination of multiple RF transceivers and use of *software radio* design principles [1–3] using CMOS RF technology. This integration problem is made worse by the rapid deployment of scaled RF CMOS technologies in high-frequency RF transceivers. As the authors of [4] point out, individual scaled 90 nm CMOS transistors are unconditionally stable above 40 GHz. Hence, matching networks, feedback mechanisms, and loading networks must be designed very carefully to prevent oscillations in high-frequency circuits. In the future, higher speed circuits will be possible with scaled devices. However, the resulting circuits will be increasingly susceptible to manufacturing process variations and coupled noise from various on-chip sources. The former results in RF circuit nonidealities due to nonlinear behavior and mismatch effects. The latter is manifested as signal integrity problems due to

(i) power and ground bounce effects at the package level,
(ii) On-chip substrate coupling noise between digital and analog functions,
(iii) noise induced by electromagnetic radiation, and
(iv) transient errors.

Any combination of the above can degrade overall quality of service (QoS) and cause spectral content to spill over into adjacent communication channels. It is clear that future advanced scaled-CMOS RF front end modules will need to be carefully tested and calibrated to avoid these problems. In addition, to manage device degradation in the field, self-test and self-calibration capability must be designed into the transceiver itself.

In the past, there has been significant work in the area of built-in RF test using embedded sensors. The concept

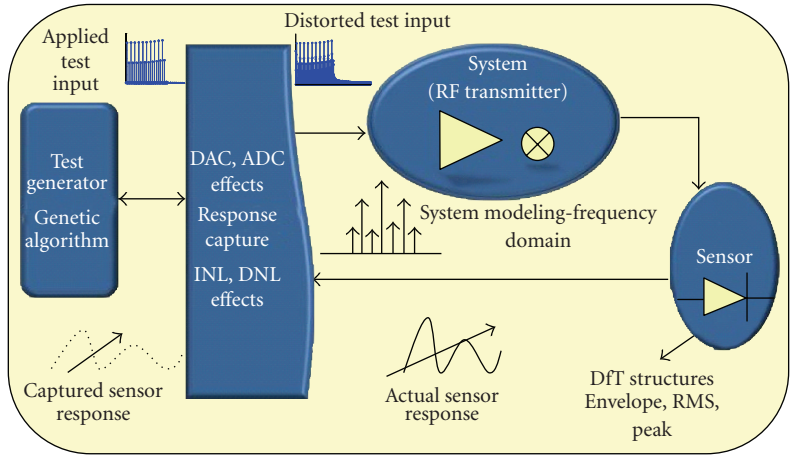


Figure 1: Building blocks of the proposed test simulator.

of *alternate test* has been used to derive compact low-cost test procedures [5–8]. Alternate tests make use of a compact stimulus to estimate multiple specifications of a system with high accuracy using a single data acquisition. The test is designed in such a way that the response of the device under test (DUT) to the applied stimulus is strongly correlated with the test specifications of the DUT of interest under random process variation effects. The procedure allows accurate diagnosis of the DUT's test specifications during field operation without the use of complex RF test instrumentation.

In this work, a formal built-in test methodology for RF systems is proposed that supports diagnosis and tuning of the same. The test framework uses special embedded RF sensors for test response data acquisition from different points of the RF signal path. The proposed methodology determines the *best stimulus to apply* (generated by software running on the transceiver DSP) and the *best embedded sensors* [9–11] *to use* (prior work focused only on one specific sensor type for an application) for high-quality parametric test and diagnosis.

The *impact of the data converters* specific to the RF transceiver being tested is considered in the design methodology. The best sensors to use are those that have the *least* impact on RF DUT performance, while generating the *maximum* amount of test information. The volume of data generated by each sensor and the resulting test time is also considered. Section 2 describes various modeling techniques that underline the design infrastructure. Section 2.4 describes the test generation algorithm that is used to generate a test stimulus that maximizes the test information that can be obtained from the DUT response. The generated test stimulus is stored in the system DSP and used to test the system periodically during system idle time. Section 2.5 presents built-in RF test-assisted diagnosis and tuning techniques that improve the performance of the transmitter. Section 3 presents simulation results for the BIT assisted diagnosis and performance tuning of an RF transmitter. Conclusions and future work are discussed in Section 4.

## 2. MODELING THE COMPONENTS OF THE RF TEST SIMULATOR

The key components of the RF test simulator are shown in Figure 1. The following are key BIT design goals.

(i) Accurate behavioral modeling of all the components of an RF transceiver (mixer, power amplifier, LNA, etc.). This is essential to developing a high-quality built-in test solution as use of behavioral models permits rapid simulation-driven test generation.

(ii) The applied tests are generated by an algorithm that *co-optimizes* the test stimulus, the on-chip test stimulus generation and response capture hardware (test access points, test response sensors) in such a way that the nonidealities of the hardware (linearity, noise) are taken into consideration while searching for the "best" built-in test solution (combination of test stimulus, test access points, and sensors employed for built-in test).

### 2.1. Transmitter modeling

Although, transistor-level simulation of all the submodules yields high accuracy of simulation, long simulation times make this impractical. The primary objective of test generation is to determine the optimal set of test stimuli [12, 13] rather than to verify the functionality of the design.

As long as the behavioral modeling approximations preserve the relative "goodness" of one possible test stimulus versus another, it can be used for fast test generation with little loss in test accuracy as shown in [12, 13].

The underlying assumption is that the variations in specification data and measurement data follow the same statistical trend under behavioral parameter perturbations as they would for transistor level parameter perturbations. Figure 2 shows the modeling approach (similar to that proposed in [12, 13]) employed for the RF system—under-test.

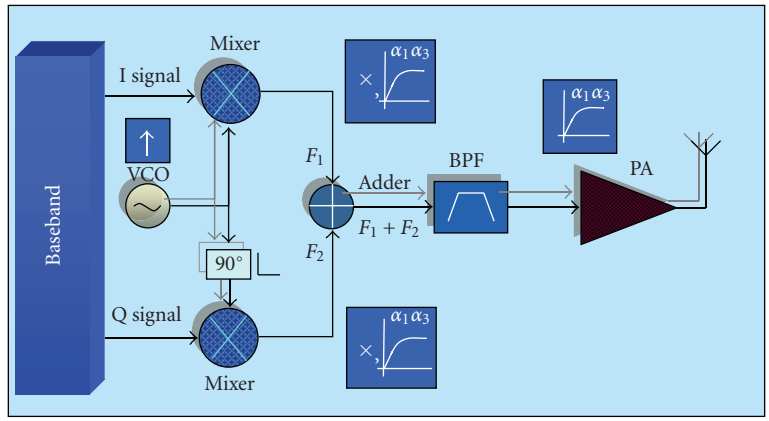


Figure 2: Block diagram of the behavioral model of an RF transmitter.

The behavioral model of each subblock was constructed as follows.

*Filter:* The transfer functions of the bandpass filters of the RF subsystem are realized as linear transfer functions with specified magnitude and phase characteristics.

*Amplifiers:* The amplifiers of the RF subsystem (e.g., LNA) are realized by implementing a nonlinear transfer function of the type

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t), \tag{1}$$

where $\alpha_0$ = DC offset, $\alpha_1$ = small signal gain, $\alpha_2$, $\alpha_3$ = nonlinearity coefficients.

The coefficients are "fitted" to the specified linear (gain) and nonlinear (harmonics and intermodulation terms) effects of the amplifiers concerned. Using the time domain input versus output characteristic as given by (1), the corresponding output frequency spectrum (both magnitude and phase) is computed. In general, the computation complexity is $O(N^3)$, where $N$ is the number of test tones used for test generation/simulation.

*Mixers:* Mixers are modeled as nonlinear transfer functions followed by an ideal multiplier. The nonlinear transfer function is realized in the same manner as discussed earlier for amplifiers. The frequency mixing operation is realized by the multiplication operation

$$y(t) = C \times x_1(t) \times x_2(t), \tag{2}$$

where $C$ represents the conversion gain of the mixer.

*Oscillator:* The peak amplitude value corresponds to the local oscillator frequency; the amplitudes adjacent to the frequencies fall off according to the phase-noise characteristics of the local oscillator.

In the above, the coefficients $\alpha_0$, $\alpha_1$, and so forth that are used to define the linearity of amplifiers are extracted from the input-output ($P_{\text{in}} - P_0$) relationship of the amplifier as determined by transistor level simulation via least squares polynomial fitting. Alternatively, they can also be extracted from the 1 dB compression point and IIP3 specifications of the amplifiers. The relationship between P1 dB and IIP3 can also be used to obtain the behavioral parameters of the subsystems. Equation (3) describes the modeling process mathematically;

$$\alpha_3 = \frac{P_0}{(P_{1\text{dB}}^2 P_{\text{in}}/0.145) + (3P_{\text{in}}/4)}, \qquad \alpha_1 = \frac{\alpha_3 P_{1\text{dB}}^2}{0.145}. \tag{3}$$

### 2.2. Modeling ADC/DAC nonlinearity

The nonlinearities of the ADCs/DACs used for data acquisition and stimulus generation (in production test systems) significantly affect the signal quality of both the applied test stimulus and the observed test response. The capture characteristics are modeled from the specified nonlinear characteristics of the PCI6115 data acquisition card (DAQ) used in the prototype test system. The PCI6115 is used as a low cost replacement for an ATE to transfer test data to the baseband processor (in our case, a PC). The INL and DNL characteristics obtained from the datasheets of the PCI6115 DAQ card are used to characterize the sourcing and digitizing properties of the data acquisition system used in this work. The frequency domain inputs and outputs of the developed digitizer model are shown in Figure 3. It can be observed that the signal quality of the test response is significantly affected by the nonlinearities of the sourcer/digitizer modules.

### 2.3. Modeling test response sensors

In this section, the modeling of three different types of test response sensors has been discussed.

#### 2.3.1. Envelope detector sensor

The envelope detector employed is shown in Figure 4 and its uses as a test response sensor were first proposed by Han and Chatterjee in [14]. This is a common circuit for AM demodulation, composed of a diode, a resistor, and a capacitor. Through proper adjustment of the $RC$ constant value, the requisite envelope detection can be performed. The value of the $RC$ time constant should be such that

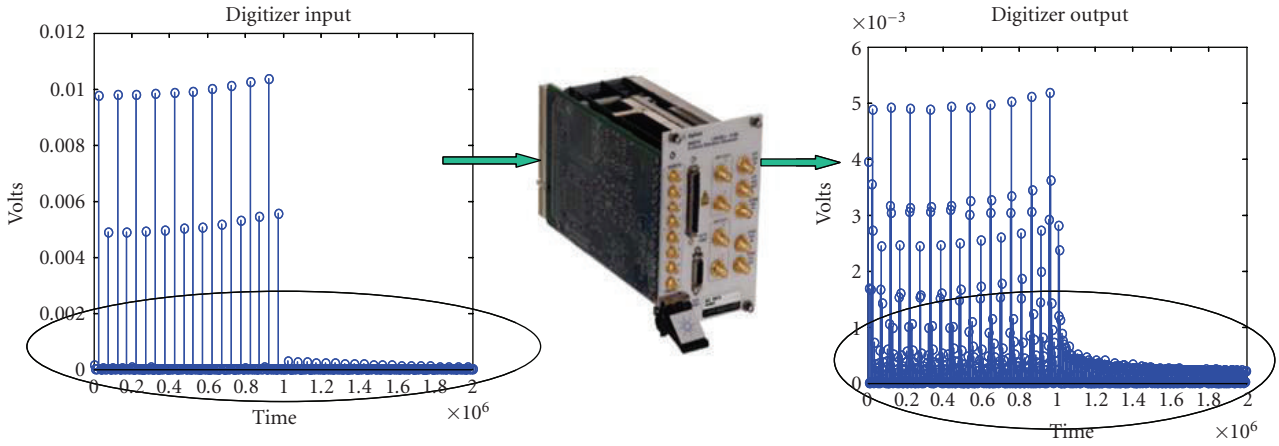


Figure 3: Test response before and after the digitizer module.

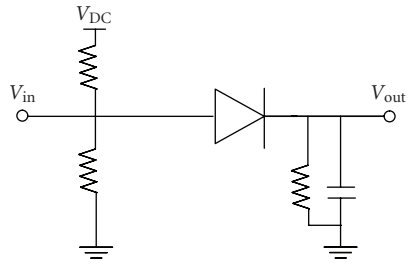


Figure 4: The schematic of the envelope detector.

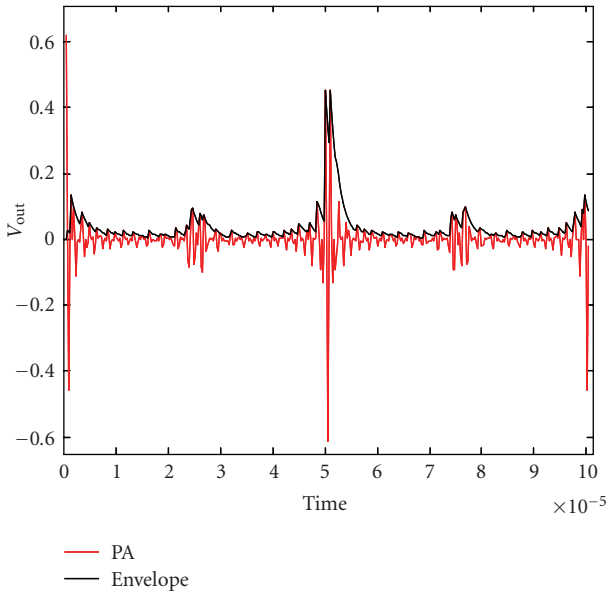


Figure 5: Envelope detector output.

$fo \ll 1/RC \ll fc$. This allows the circuit to track the low-frequency envelope of the RF signal. Considering that the above two frequencies have large separation, the $RC$ time constant can be picked to make the decoded envelope immune to process variations.

A key consideration is the loading of the circuit under test (CUT) by the envelope detector. The input impedance of the envelope detector depends mainly on the bias resistors and the capacitance of the diode. The bias resistors are relatively large compared to the typical 50 Ohm RF matching impedance. During the normal operating mode, the power for the envelope detector can be turned off using a switch [14]. Hence, the diode behaves like an open switch. In general, the capacitance of a diode is several tens of farads. Therefore, the impedance (loading) of the envelope detector has negligible effect on the RF DUT performance. Figure 5 shows the transient output of the envelope detector showing that it follows the RF envelope. The observed output is a transient waveform and hence it has much more information compared to the o/p of RMS or peak detectors. However, this added information comes at the cost of having to process much more data than just single DC RMS or peak values.

### 2.3.2. *RMS detector sensor*

Figure 6 shows the RMS detector circuit [15] used as the test case in this research. Elements L1 and C1 form the matching network, providing a 50 Ohm match at 1.5 GHz.

The low value of S11 for this detector (<−45 dB) results in minimal loading of the RF system. $R_2$ is chosen so that the circuit provides the "true" RMS value of the input signal to the detector. Though it is debated in [16] that this does not achieve true RMS detection, the accuracy achieved is good for the purpose of this work.

The output of the detector for a multitone input stimulus is plotted in Figure 7 for four different specified combinations of input power levels. It is observed that both the DC value as well as the ripple voltage increases with the increase in input power level.

### 2.3.3. *Peak detector*

The conceptual diagram of a standard peak detector is shown in Figure 8. The biasing and matching circuits have not been shown for simplicity. The output is a DC voltage indicating

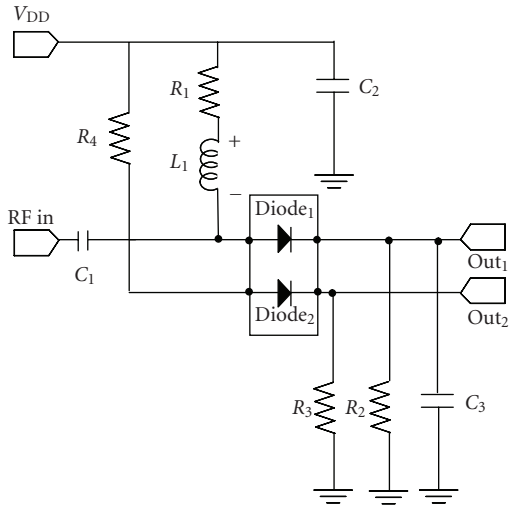


Figure 6: Schematic diagram of the RMS detector.

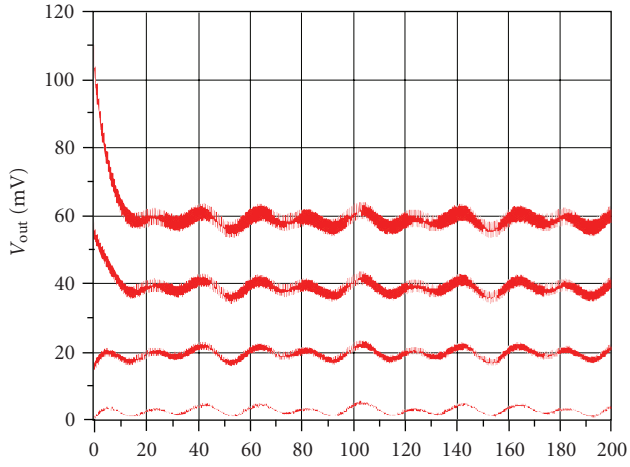


Figure 7: RMS detector output for different power levels of multitone input signal.

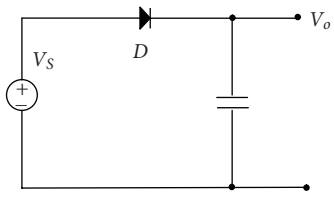


Figure 8: Conceptual diagram of the peak detector.

the peak of the applied voltage. As shown in Figure 8, the voltage $V_o$ takes some time to reach its final value. This transient response is ignored and the final steady-state value is considered as the peak value.

Figure 9 shows the transient output voltage for different power levels of a multitone input signal. The voltage attains its steady-state level after a certain amount of time depending on the input power level. This information is used to model the peak detector.

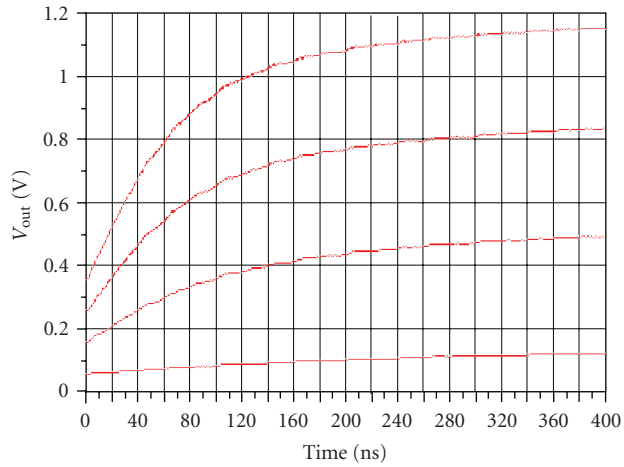


Figure 9: Transient response of the peak detector to multitone input signals of different power levels.

### 2.4. Test generation

Alternate test procedures have been extensively used in the past for analog/RF circuits to accurately predict specifications of interest. In this approach, regression functions such as those generated by MARS [8] are used to build a mapping function between the test response and the DUT specifications using a set of devices with random process variations called the *training set*. During the actual test, trained MARS models are used to predict the specifications of the DUT from the observed test response.

It should be noted here that a *defect filter* is used to screen out devices with catastrophic faults, and only the devices that "pass" the defect filter are considered for this study. This defect filter consists of simple algorithms that analyze the test response of the DUT to determine whether it has characteristics that are different from the "training set" of devices used to build the MARS regression model described earlier. The alternate test quality is highly correlated to the sensitivity of the observed measurement response to changes in the process parameters. For a given DUT, there are several test generation algorithms [17] available for optimizing the input test stimulus. In this work, a genetic algorithm-based test generator (as shown in Figure 10) is used due to the nonlinear nature of the search space to avoid local convergence. An optimized multitone test input is used as the test stimulus of choice. The multitone test stimulus is binary coded to result in a genetic individual of length 100 bits, with each tone represented by a 5 bit gene sequence.

*Crossover* and *mutation* are the two mechanisms by which a new generation of solutions is created [18]. Figure 11 shows an example case of crossover. In crossover, two parent genes are crossed over in an arbitrary fashion defined by the crossover probability to result in a completely new child. In mutation a single bit of the gene sequence is randomly mutated as determined by a mutation probability to result in a new child. These two mechanisms are responsible for the creation of new individuals which in-turn are assessed for their fitness. There is one another mechanism known as

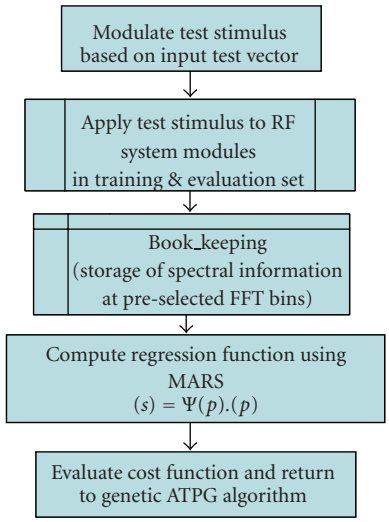


Figure 10: GA-based optimization routine.

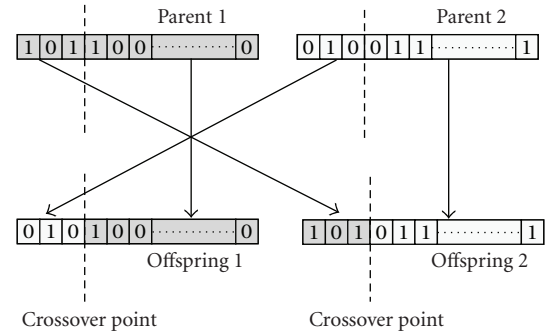


Figure 11: Single-point crossover operation for reproduction in the GA.

elitism in which genes with a particular fitness values are classified as *elite* and are passed on from one generation to another without any crossover or mutation. This ensures that a "minimum" fitness is passed on from one generation of solutions to another. Further insights into the algorithms can be found in [8].

The multitone test stimulus is a carefully crafted test stimulus with selected number of tones and varying amplitude levels. A set of 20 tones are uniformly deployed across a bandwidth of 1 MHz. The amplitude levels are allowed to have 32 ($2^5$) levels of variation ranging from −70 to 10 dBm. Thus, each tone can be coded into a 5 bit gene sequence to result in a 100 bit gene individual. This waveform is then converted to the frequency domain by means of the Fourier transform.

Figure 12 shows the frequency domain representation of two multitone signals with 20 component tones with coherent and noncoherent sampling. The wide-skirts observed in Figure 12 are the outcome of noncoherent sampling of the time domain waveform. Coherency is mathematically represented [19] as follows:

$$\frac{f_{\text{in}}}{f_s} = \frac{n_{\text{window}}}{n_{\text{record}}}, \tag{4}$$

where $f_{\text{in}}$ is the input frequency of the multitone signal; $f_s$ is the sampling frequency; $n_{\text{window}}$ is the number of cycles of the signal that fits in a sampling window; and $n_{\text{record}}$ is the number of data points in the FFT of the signal. The presence of unwanted tones in the test input degrades the test quality significantly. Hence, it is very critical that the multitone is coherently sampled. The genetically optimized waveform is then used to obtain the response of the component receivers. The subsystem specifications are computed by mapping the response to the subsystem specifications using nonlinear regression techniques.

The proposed test simulator as described above is used to evaluate different BIT alternatives. A set of candidate BIT solutions is first selected for evaluation. Each candidate consists of a set of sensors (envelope, rms, or peak) attached to a specified set of nodes (output of mixer or power amplifier). The test generation algorithm produces an optimized test stimulus for each BIT candidate. The BIT candidates are then ranked in order of the accuracy with which the test specifications of the RF DUT can be predicted from the observed test response. Since the hardware cost of each BIT solution is also known, the test designer can then pick the best solution from a cost versus accuracy perspective as desired by the test customer.

### 2.5. Built-in RF test-assisted diagnosis and tuning procedure

The BIT technique evaluated by the test simulator is used to drive diagnosis and tuning procedures for the RF transceiver. The diagnosis and tuning performed here restores the performance of the DUT in the presence of process variation induced performance degradation. Figure 13 describes the proposed approach. A built-in envelope tracking sensor (or other sensors as presented earlier) at the output of the transmitter is used to capture the transmitter response. The envelope detector consumes very little area overhead and is robust to process variations. The sensor captures the envelope of a multisine test stimulus, and "response features" extracted from this envelope are used to track the power and nonlinearity specifications (amplitude and phase distortion) of the power amplifier (PA). The transmitter can be tested during production testing, or while the system is idle (concurrent testing).

The captured response is a low-frequency signal that contains information about the linearity of the PA, is sampled, and fed to the baseband processor. The performance parameters of the transmitter are then predicted accurately from analysis of the obtained response envelope using nonlinear regression mapping functions built from calibration experiments.

The test stimulus is designed to exercise the nonlinearities of the PA. Optimized test stimuli is fed individually to I and Q channels to exercise PA non-linearity. When multiple nonidealities (I/Q mismatch, frequency offset) are present in the transmitter, a test stimulus optimization

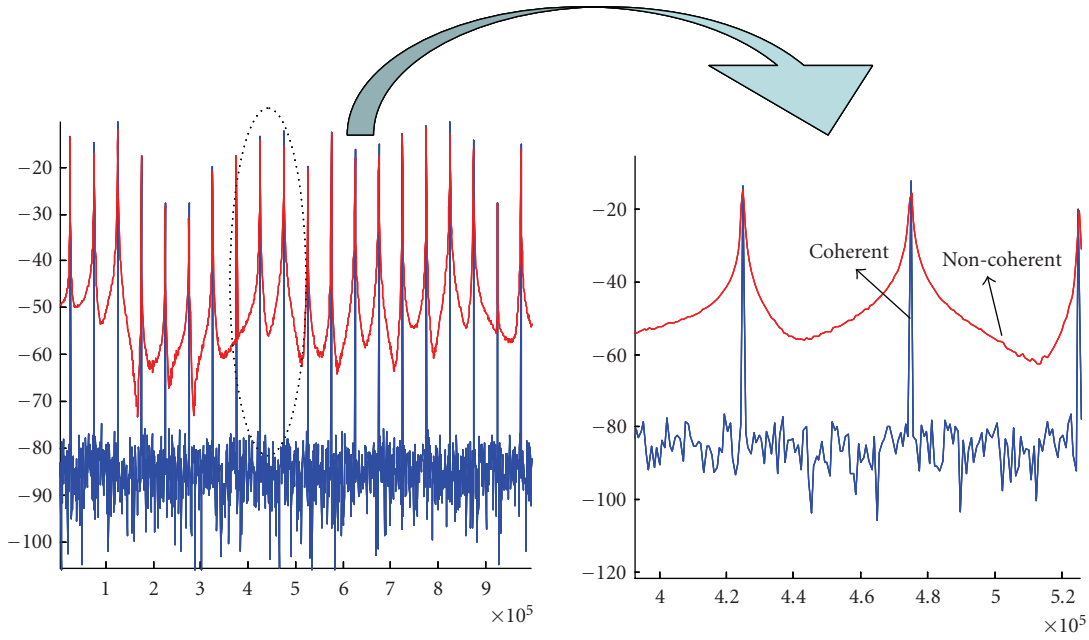


Figure 12: Coherently and noncoherently sampled response.

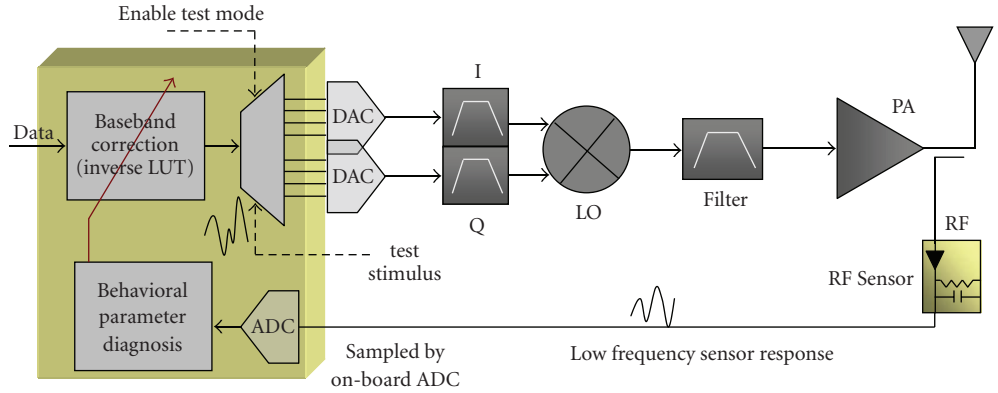


Figure 13: The proposed transmitter diagnostic testing and compensation approach.

algorithm is used to design the test stimulus to increase the accuracy of transmitter specification prediction from the obtained response. Using the captured "response features" of the transmitter, the behavioral performance parameters are predicted. After the PA nonlinearity is determined, an inverse function to the predicted PA transfer characteristics is computed to determine the predistortion coefficients (alpha values) and stored in a lookup table (LUT) in the DSP for correction (tuning). During real-time operation, the input signal to the transmitter instance is predistorted by the corresponding polynomial to tune out the effects of nonidealities present in the transmitter system.

## 3. VALIDATION OF THE PROPOSED METHODOLOGY

The proposed BIT design methodology has been validated on a wireless RF transmitter. The transmitter was modeled as described in Section 2. The proposed test simulator was implemented in Matlab.

### 3.1. BIT evaluation

The test simulator allows evaluation of different choices of test access points (nodes at which test response sensors are inserted) and test response sensors, while taking into account the nonlinearity and noise of the on-chip test response data acquisition and stimulus generation hardware. Optimized tests are generated for each such test configuration using the genetic algorithm-based test generator described earlier and the "best" test configuration (the one that allows the specifications of the DUT to be predicted from the test response with the highest accuracy with minimal hardware cost) is used for on-chip BIT.

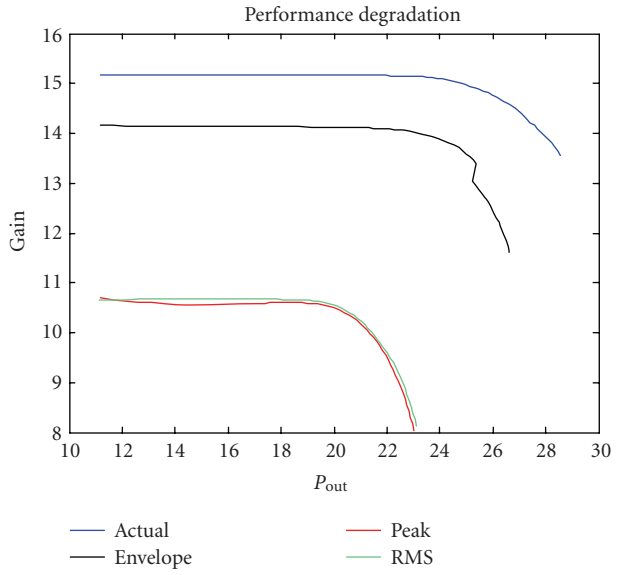


Figure 14: Performance degradation of the power amplifier for three types of sensors.

Table 1: Performance degradation of the power amplifier at 15 dBm output power level.

| Component | Actual | Envelope | Peak | RMS |
|---|---|---|---|---|
| PA | 15.16 | 14.14 | 10.58 | 10.64 |

Table 2: Evaluation of the test quality for three types of DfT solution.

| Error type | Envelope | Peak | RMS |
|---|---|---|---|
| Rms_error | 0.1475 | 0.2 | 0.21 |

#### 3.1.1. Impact of test response sensors on performance of transmitter

For simplicity, the sensors were deployed only at the output of the power amplifier of the RF transmitter. The performance degradation simulation was performed using Agilent Advanced Design System (ADS). The performance degradation plots in terms of the operating *gain* of the transmitter are shown in Figure 14. The results are quantified numerically in Table 1 for a specified level output power level of the transmitter.

It is observed that the envelope detector provides the least performance degradation of 1 dB at an output power of 15 dBm.

#### 3.1.2. Impact of test response sensors on test quality

The quality of the alternate test procedure employed was determined by the accuracy with which the specifications of the DUT could be predicted from the obtained BIT response. The rms prediction error over a large number of sample DUTs was used to quantify the quality of the BIT technique. This is shown in Table 2.

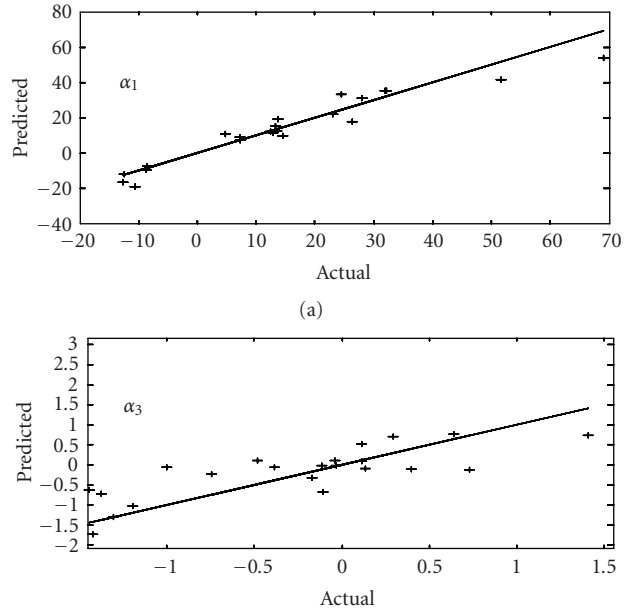


Figure 15: Diagnostic parameter estimation for the evaluated BIT technique.

#### 3.1.3. Sensor selection

In general, the BIT solution that provides the least amount of performance degradation while providing acceptable accuracy of specification prediction from the test response is chosen as the final test solution. The envelope detection sensor attached to the output of the transmitter was found to have the best performance of the three sensors investigated in this work. It is important to note here that the developed tool has the capability to select the best possible DfT solution given an available set of sensors and their designs (e.g., there are many different ways in rms sensor can be designed). In the following, the recommended DfT solution is used to perform diagnostic testing and tuning of the RF transmitter.

#### 3.1.4. BIT-assisted diagnosis of the RF transmitter

The best possible test input as generated by the test simulator for the recommended DfT solution is stored in the system DSP and is used to drive the BIT procedure from the DSP. The behavioral parameters $\alpha_1$ and $\alpha_3$ of (1) are used to characterize the transmitter's performance and are predicted from the obtained BIT response to the applied test stimulus. The developed BIT technique was evaluated on a set of 23 instances of the transmitter. The prediction plots of the diagnostic parameters for the transmitter are shown in Figure 15. As seen from the plots, the parameters are estimated with good accuracy.

#### 3.1.5. Transmitter tuning

Once the polynomial of (1) corresponding to the transmitter is known, a lookup table based inverse correction

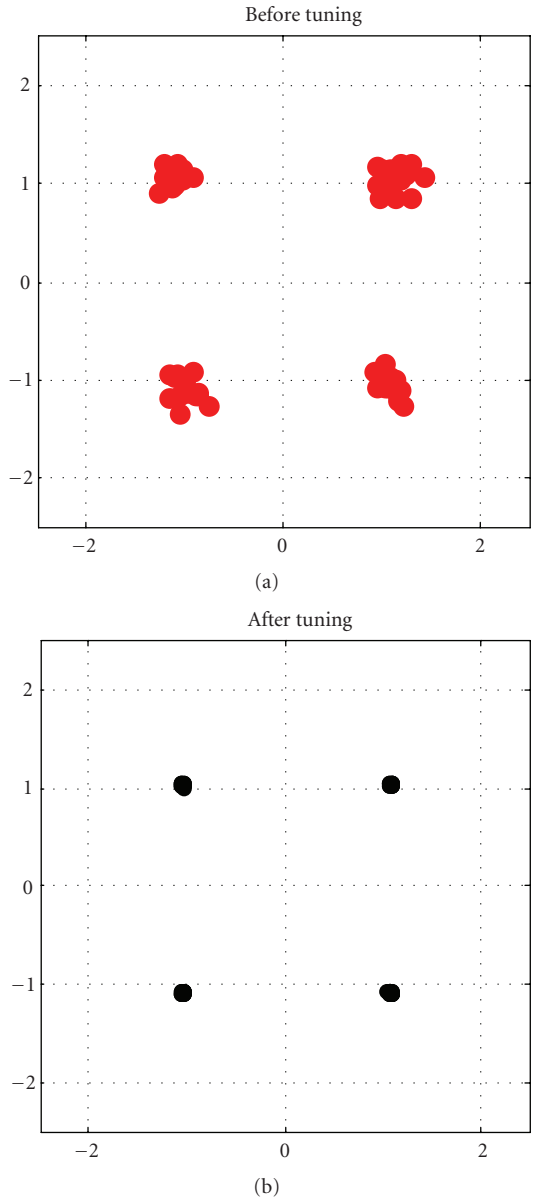


FIGURE 16: OFDM-QPSK constellation plots for a transmitter.

function that predistorts the input of the transmitter to compensate for its intrinsic nonlinearity is used to improve transmitter performance. To evaluate the effectiveness of the tuning procedure, the transmitter was interfaced with a baseband OFDM module and the system was simulated by transmitting QPSK modulated frames. Figure 16 shows the transmitted OFDM-QPSK constellation plots with and without digital predistortion. As observed from the plots, the nonlinear characteristics of the transmitter are compensated accurately (nonlinearity results in a "spread" of each of the four constellation points corresponding to OFDM-QPSK as observed in the left constellation diagram.

Currently, test quality along with the performance degradation of the sensor is used as the primary method for BIT sensor selection. In general, the dynamic range of the sensors, the volume of sensor data generated as well as the complexity of the sensor design and performance (sensor bandwidth and loading of the DUT) will need to be considered as well and can be incorporated easily into the test simulator.

## 4. CONCLUSION AND FUTURE

A methodology for optimizing built-in test infrastructure to diagnose and tune an RF transmitter is presented here. *The evaluated BIT technique* can *accurately diagnose the system performance parameters*. Also, a tuning procedure for digital predistortion is proposed that accurately compensates for system nonlinearities. These results justify the need to co-optimize the DfT structures along with the response capture characteristics to result in a highly accurate BIT. Current work is focused on extending the approach to a complete RF transceiver.

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## REFERENCES

[1] B. Razavi, *RF Microelectronics*, Prentice-Hall, Upper Saddle River, NJ, USA, 1997.

[2] H. Tsurumi and Y. Suzuki, "Broadband RF stage architecture for software-defined radio inhandheld terminal applications," *IEEE Communications Magazine*, vol. 37, no. 2, pp. 90–95, 1999.

[3] R. Bagheri, A. Mirzaei, M. Heidari, et al., "Software-defined radio receiver: dream to reality," *IEEE Communications Magazine*, vol. 44, no. 8, pp. 111–118, 2006.

[4] L. M. Franca-Neto, R. Eline, and B. Balvinder, "Fully integrated CMOS radios from RF to millimeter wave frequencies," *Intel Technology Journal*, vol. 8, no. 3, pp. 241–258, 2004.

[5] S. Bhattacharya, A. Halder, G. Srinivasan, and A. Chatterjee, "Alternate testing of RF transceivers using optimized test stimulus for accurate prediction of system specifications," *Journal of Electronic Testing*, vol. 21, no. 3, pp. 323–339, 2005.

[6] S. Bhattacharya, R. Senguttuvan, and A. Chatterjee, "Production test technique for measuring BER of ultra-wideband (UWB) devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 11, pp. 3474–3481, 2005.

[7] A. Halder and A. Chatterjee, "Test generation for specification test of analog circuits using efficient test response observation methods," *Microelectronics Journal*, vol. 36, no. 9, pp. 820–832, 2005.

[8] J. H. Friedman, "Multivariate adaptive regression splines," *The Annals of statistics*, vol. 19, no. 1, pp. 1–67, 1991.

[9] D. Han, S. Bhattacharya, and A. Chatterje, "Built-in RF transceiver test and diagnosis using transient envelope detection and sampling," in *Proceedings of the IEEE International Mixed-Signal Testing Workshop (IMSTW '06)*, pp. 250–257, Edinburgh, UK, June 2006.

[10] Q. Yin, W. R. Eisenstadt, R. M. Fox, and T. Zhang, "A translinear RMS detector for embedded test of RF ICs," *IEEE Transactions on Instrumentation and Measurement*, vol. 54, no. 5, pp. 1708–1714, 2005.

[11] A. Valdes-Garcia, J. Silva-Martinez, and E. Sánchez-Sinencio, "On-chip testing techniques for RF wireless transceivers," *IEEE Design and Test of Computers*, vol. 23, no. 4, pp. 268–277, 2006.

[12] S. Bhattacharya, G. Srinivasan, S. Cherubal, A. Halder, and A. Chatterjee, "System-level testing of RF transmitter specifications using optimized periodic bitstreams," in *Proceedings of the 22nd IEEE VLSI Test Symposium (VLSI '04)*, pp. 229–234, Napa Valley, Calif, USA, April 2004.

[13] A. Halder, S. Bhattacharya, and A. Chatterjee, "Automatic multitone alternate test-generaton for RF circuits using behavioral models," in *Proceedings of the IEEE International Test Conference (ITC '03)*, pp. 665–673, Charlotte, NC, USA, September-October 2003.

[14] D. Han and A. Chatterjee, "Robust built-in test of RF ICs using envelope detectors," in *Proceedings of the 14th Asian Test Symposium (ATS '05)*, pp. 2–7, Calcutta, India, December 2005.

[15] S. Bhattacharya and A. Chatterjee, "A DFT approach for testing embedded systems using DC sensors," *IEEE Design and Test of Computers*, vol. 23, no. 6, pp. 464–475, 2006.

[16] J. C. Cowles, "The evolution of integrated RF power measurement and control," in *Proceedings of the 12th IEEE Mediterranean Electrotechnical Conference (MELECON '04)*, vol. 1, pp. 131–134, Dubrovnik, Croatia, May 2004.

[17] R. Voorakaranam, S. Cherubal, and A. Chatterjee, "A signature test framework for rapid production testing of RF circuits," in *Proceedings of Design, Automation and Test in Europe Conference and Exhibition (DATE '02)*, pp. 186–191, Paris, France, March 2002.

[18] D. Goldberg, *Genetic Algorithms in Search Optimization and Machine Learning*, Addison Wesley, Reading, Mass, USA, 1989.

[19] Application note, AN1040, A/D and D/A conversion/sampling circuits basestations/wireless infrastructure, Maxim IC.