Review Article

The Achievements and Challenges of Silicon Photonics

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A brief overview of silicon photonics is given here in order to provide a context for invited and contributed papers in this special issue. Recent progress on silicon-based photonic components, photonic integrated circuits, and optoelectronic integrated circuits is surveyed. Present and potential applications are identified along with the scientific and engineering challenges that must be met in order to actualize applications. Some on-going government-sponsored projects in silicon optoelectronics are also described.

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1. INTRODUCTION

We are fortunate in this special issue to have authoritative invited papers written by key contributors to the field silicon-based photonics. It is a pleasure for me to be in the company of these leaders as I write this introductory article. The forward-looking papers here highlight the “technical momentum” that has built up in silicon photonics. They describe discoveries in science and technology that are being made worldwide at an increased rate thanks to the ramped-up investment by industry, universities, and governments [1, 2]. Transitions from “lab-to-fab” are taking place for commercial and military uses. Products are being developed (Luxtera, Kotura, SiLight). This is the beginning of optoelectronic (OE) manufacturing on a much wider scale [3]. My mission here is to give a context or background for the papers. I will review recent achievements in Si-based photonic integrated circuits (PICs) and optoelectronic integrated circuits (OEICs). I will pinpoint important challenges for the emerging OE industry, and I will identify applications that will be actualized if and when those challenges are met.

2. RECENT PROJECTS

Several new and on-going programs related to PICs and OEICs are described in this section. PICs are important in their own right, but the main driver today of the Si photonics field is the quest for low-cost large-scale-integrated OEICs manufactured in state-of-the-art high-volume silicon CMOS foundries (silicon fabs). Potentially, these chips have vast and

highly significant applications which, if implemented, would make those circuits pervasive in our planet.

The essential role that silicon nanophotonics will play in the future is highlighted in a new 2007 initiative on ultraperformance nanophotonic intrachip communication (UNIC) sponsored by the US Defense Advanced Research Projects Agency. The goal is to demonstrate low-power, high-bandwidth, low-latency intrachip photonic communication networks designed to enable chip multiprocessors with hundreds or thousands of compute cores to realize extremely high computational efficiency; a goal that embodies the convergence of computation and communication envisioned by Lionel C. Kimerling. The optoelectronic UNIC project poses a major challenge to the technical community because it will require revolutionary rather than evolutionary advances in science, devices, circuits, and computing systems.

An important investigation of nanoscale devices was made at the March 19-20, 2007 workshop on “very large-scale photonic integration” sponsored by the US National Science Foundation and chaired by Ronging Hui, Usha Varney, and Thomas Koch. Nanophotonic strategies for VLSI were explored, but the path to mass production was not clear. Corporations and universities now engaged in the fledgling OE industry need a cost-effective way to demonstrate and optimize their individual OE prototype chips. For that reason, I and other workshop participants recommended that a government-sponsored national CMOS-photonics User Facility should be set up in the United States to establish a cost-shared “photonics-ready” silicon foundry that will provide application-specific OEIC prototypes for users

throughout the technical community. The proposed user fab would rely upon the SOI photonic-component manufacturing “libraries” that are being developed at BAE Systems, Luxtera, and elsewhere. Both BAE and Luxtera are currently “on track” with their Phase II milestones for DARPA EPIC [1] (www.darpa.mil/MTO/Programs/epic/index.html). I am aware that “serious” OE programs are starting up in France, South Korea, and China, but I don’t have much information on those efforts.

The basic motivation for OE is to attain electronic drivers and controllers that are intimately integrated with their laser diodes, modulators, amplifiers and photodetectors. The larger OE goal is to create greatly improved devices, subsystems, and systems. Silicon of course is not the only OE medium, and silicon OE is currently struggling with the issue of on-chip light sources, a problem solved years ago by the III-V semiconductor laser industry. That is why OE based upon GaAs and InP is likely in the near term to give Si OE strong competition in “small-scale” integration situations, for example, in InP-based 1.55 μm transceivers (Infinera Corporation, Sunnyvale, Calif., USA) where III-V lasers and photodetectors can be integrated monolithically. However, two key advantages of silicon appear in the bigger picture: the very low chip costs that high-volume Si OE production will ultimately give, and the very high level of functionality that Si OE will eventually provide sophistication derived from hundreds or thousands of photonic components integrated on-chip with perhaps a million transistors.

Some of the cutting-edge research topics in Si photonics are nanophotonics, plasmonics [4], photonic crystals, nanomembranes, SiGeSn alloys, commercial manufacturing methods, nonlinear optics, nanoelectrooptical mechanics, and microfluidics. The papers presented at the IEEE LEOS 4th International Conference on Group IV Photonics (Tokyo, September 19-21 2007) give a good indication of the present R&D thrusts of silicon photonics (<http://www.ieee.org/organizations/society/leos/LEOSCONF/GFP2007/index.html>).

The sessions there deal with the Japanese MARAI optical interconnection project, waveguides and filters, OE and III-V hybrid integration, MOEMs and 3D structures, modulators and switches, disruptive materials and process technologies, nonlinear optics and active functions, slow-light devices and passive photonic crystals, light-source materials, light-source devices and structures, and detectors.

The new thrust in group IV nanomembranes, catalyzed by a 2008 AFOSR multiuniversity research initiative (ONR BAA Announcement Number 07-036, Research Opportunity number 10) can yield single-crystal membranes of Si or Ge or layered Group IV heterostructures whose thickness is, for example, in the 5 to 500 nm range. Such membranes could be deployed in flexible intelligent photonics and more generally in all of the applications areas listed below in Section 5.

3. THE LIGHT-SOURCE CHALLENGE

An optical network, whether fiber-optic or on-chip, requires light sources, and an Si OEIC or PIC is incomplete without sources. Because bulk crystalline silicon has inefficient electroluminescence, light sources have been critical issues

for silicon photonics since its inception. For these reasons, the creation of practical silicon light sources is a major, ongoing R&D focus.

Off-chip light sources can be thought of as a “photon supply” or “optical power supply” for the chip. In a particular subsystem or application, the decision about whether to locate the light source on- or off-chip is “situational,” depending upon factors such as heat sinking, average power consumption, energy dissipated per bit per second, cost, and size. Both on- and off-chip solutions have been proposed for intrachip interconnects. The preferred light source is usually (but not always) a laser. The case of a spectroscopic laboratory on a chip [5, 6] presents an exception to the “rule” of laser. There, a spectrally broad source like an on-chip light-emitting diode would be optimum, although a WDM laser array could serve also.

Silicon Raman lasers and amplifiers are certainly useful in silicon photonics, but intense optical pumping is required for these on-chip devices (it takes a laser to make a Raman laser) so the pump is likely to be off-chip and capable of pumping several on-chip gain devices.

Significant Si-based sources are beginning to emerge due to hard work by the technical community. We can divide these sources into those that will be available in five years and those emerging in a year or two. Regarding the integration of on-chip sources, the categories are monolithic and hybrid. These terms are a bit vague: I will interpret the word “monolithic” to mean “entirely within group IV” and “hybrid” to mean “silicon plus III-V” or silicon plus “other” (in other words, heterogeneous integration).

The III-V/Si hybrid source technique of John Bower’s group at UCSB is a very potent short-term solution that provides on-chip evanescently coupled lasers-on-SOI, amplifiers, photodetectors, and modulators created by low-temperature bonding of the PIN III-V components to the top surfaces of the waveguided silicon network. The remaining questions about these hybrids are in the areas of manufacturing and economics. Will the hybrids be viable in a CMOS Fab and will the yields be high? The answers are not known yet.

The US Air Force Office of Scientific Research has a multiuniversity research initiative on electrically pumped silicon-based lasers, an effort in its second year (see http://www.mphotonics.mit.edu/about_mphc/MURI/siliconlasers.php and http://www.asu.edu/news/stories/200603/20060310_MURI.htm). The lasers of the MIT team are either extrinsic or intrinsic. A quantum dot or nanocrystal gain medium within Si is extrinsic, while a tensile-Ge gain medium within an Si/Ge/Si heterostructure is intrinsic. The Arizona State University team utilizes an intrinsic “all in group IV” approach employing intersubband emission in Ge/SiGeSn multiquantum-well structures for the far infrared, and band-to-band emission in GeSn/SiGeSn or Ge/SiGeSn heterostructures for the near/mid infrared. The MIT and ASU intrinsic lasers appear to be CMOS manufacturable. The five-year MURI results will be very important to the SiOE industry if the resulting lasers have adequate efficiency and intensity.

4. THE HIGH-VOLUME CHALLENGE

Job creation and an expanded economic infrastructure will be triggered by sustained growth of the “nascent” silicon optoelectronics industry, growth that would be supported by long-term high-volume markets. A strong industry would provide optoelectronic “hardware for the information age,” thereby benefiting a global society that values “bits more than things” [7]. We examine high-volume SiOE markets in this section.

Which devices will likely be purchased at the rate of ten million units per year? The answer according to the MIT CTR consortium [7] is the transceiver, a Si-based send-and-receive optoelectronic chip. Two fast chips interconnected by a fiber create a duplex fiber-optic communication link that, with near-future technology, is capable of transmitting data at rate anywhere from 1 Gbps up to 100 Gbps, depending upon the sophistication of the chip constituents. If the chip can be manufactured to sell at a price of one dollar per Gbps or less, and if the chip will draw less than 1 mW/Gbps of power, then the transceiver will probably meet the needs of several major markets including: broadband core-, metro- and access-networks (fiber to the home, internet box, Ethernet LAN, FTTX), supercomputers, high-performance computers, enterprise networks, data centers (active cables as computer patch cords; optical interconnects for cabinet to cabinet, board to board, chip to board, and chip to chip), avionics-automotive-shipboard (communication and control links for aircraft, cars and ships), and microwave photonics (optical control of a phased-array antennas). Potentially, there are also huge, pervasive markets for “nanotransceivers” found inside new computer chips where waveguides link CPU cores.

Optics will replace copper if and only if the optics has compelling advantages. If SiOE research and development succeed in making on-chip optical linkages sufficiently fast, small, efficient, cheap, and reliable, then “long” copper paths would be replaced and many millions of such OE chips would appear in next-generation personal computers, notebooks, and gaming boxes (Playstation, Nintendo).

In addition to the DARPA effort mentioned above, the optical interconnect MIRAI project sponsored by Japan’s MITI is making a major R&D investment in the intrachip area [8]. The main objective is ultrafast on-chip global interconnects having a total path length of 5 to 30 mm. A second goal is optical clock distribution. Their optical interconnect approach is quite pragmatic and “wavelength agnostic”; whatever wavelength and technology are cost-effective and work well are appropriate. They will use an off-chip light source (or an off-chip WDM laser array) emitting in the 800 nm range, together with SiON waveguides and Si photodiodes. Modulation will be accomplished by poled PLZT films.

I will conclude this section with some speculations about chip-scale 1550-nm global interconnects and the “not-yet-born” nanolasers that will be necessary to produce them. There are many feasible architectures for an SOI waveguided optical network that gives communication among multiple processor cores on a computer chip. I will illustrate here the

FIGURE 1: Top view of proposed SOI waveguided intrachip photonic interconnect system for global communication among eight cores.

FIGURE 2: Structure of the strip-waveguided group IV nanolasers and nanophotodetectors used in Figure 1.

example of a reconfigurable broadcast network for eight-core interconnection. The four-ring layout of Figure 1 is similar to the WDM- and switched-network geometries that I presented in slides at the high-speed interconnect workshop [9]. In Figure 1, the green octagons are made from Si strip waveguides. Each bus-coupled circular ring (red, orange, green, blue) in Figure 1 is a reconfigurable optical add-drop multiplexer (ROADM) that can be electrically tuned over eight laser wavelengths around 1550-nm. Each PIN laser diode and photodiode in Figure 1 (integrated in a silicon strip waveguide shown as a green line) would use tensile Ge as the gain medium [10]. In [1, Figure 5], I suggested that a carrier-injected lateral superlattice formed within a germanium PIN-diode microring could be the heart of a 1550-nm laser. To attain a smaller-than-ring mode volume in a laser resonator, the Ge nanolasers and the nanoscale Ge photodetectors presented here in Figure 1 would each have an inline Fabry-Perot cavity created by a pair of 1D photonic crystal (PC) “mirrors” in a silicon strip (photonic wire) waveguide as illustrated in the enlarged top view of Figure 2. The resonator, consisting of one or two PC point defects, would have a mode volume of approximately $(\lambda/2n)^3$.

The tapered hole-diameter mirrors in Figure 2 minimize out-of-plane loss and maximize Q as discussed in a “nanolink” patent application [11]. The reflectors in Figure 2 consist of a row of air columns and are equivalent to a set of deeply etched rectangular slots in the SOI strip (a tapered Bragg mirror).

As shown in the detailed views of Figure 3, the tensile-Ge or GeSn parallelepiped (an ultrasmall bulk crystal) is grown selectively within an Si strip trench to form a P-Si/I-Ge/N-Si heterodiode, forward- or reverse-biased, as needed.

FIGURE 3: Closeup views of the Figure 2 resonant lateral PIN Ge-in-Si (or GeSn-in-Si) heterodiode laser (and photodetector) used in the Figure 1 nanophotonic system.

The lateral P-type and N-type silicon “wings” bracketing the Ge create a localized rib waveguide within the strip waveguide, a rib that does not disturb the fundamental guided mode. Addressing the ROADMs in Figure 1 will be discussed elsewhere. Thermal stability is a challenge for any of the resonant devices discussed in this paper.

5. THE DREAM AND CHALLENGE OF HIGH-IMPACT APPLICATIONS

I believe that “well-developed” Si-OEICs will have major impact on global society and commerce. Generally speaking, the Si OE application areas are optical interconnects, sensor technologies for the visible and near-, mid-, and far-infrared [5, 12, 13], signal processing functions, imaging, displays, energy conversion, illumination, optical storage, and gaming. If I look inside of these eight categories, I can identify specific high-impact cases. These are the challenges and opportunities for those of us involved in Si OE:

- (a) *interconnects*: all of the transceiver applications listed above in the high-volume section, electrooptically switched (reconfigured) optical networks;
- (b) *sensors*: infrared spectrometer-on-a-chip, photonic laboratory-on-a-chip for sensing chemical and biological agents, lab-on-a-chip for environmental monitoring or process control or medical diagnosis;
- (c) *signal processing*: wireless mobile multifunction “phone-like” device, optical time-delay beam-steerer for a phased-array microwave antenna, RF-optical receivers for RF spectrum analysis, ultrafast analog-to-digital converters, reconfigurable wavelength-division multiplexers and demultiplexers, reconfigurable optical filters, electronic warfare processors, photonically enhanced microwave and millimeter-wave circuits, optical buffer memories, electrooptical logic that operates on phase-coherent light beams, quantum communication-cryptography-metrology-computing, photonic testing of electronic ICs, bionic
- signal processors; neural network processors; data-fusion chips using inputs from several sensors;
- (d) *imaging*: focal-plane-array imager with integral read-out: infrared-to-visible image converter chip;
- (e) *displays*: chip-scale electrooptical display with integral scanning;
- (f) *energy*: highly efficient group IV photovoltaic solar cells with integral signal processing—perhaps with thin-film supercapacitors for energy storage;
- (g) *illumination*: efficient group IV solid-state lighting devices;
- (h) *optical storage*: read/write chips for ultradense CDs and atom-scale memories;
- (i) *gaming*: ultrafast graphic computation chips for Nintendo and Playstation.

I feel that nonlinear optical effects in group IV PCs and photonic-wire devices will have applications in signal processing. These NLO effects encompass all-optical modulation, all-optical wavelength conversion, electrooptically tuned resonator wavelength conversion, four wave mixing, broadband parametric gain, all-optical signal regeneration, electromagnetically induced transparency, Pockels-effect polymer/Si self-phase modulation, cross-phase modulation, stimulated-Raman slow-light delay lines, temporal pulse compression, and soliton generation. Many of these apply to optical networks.

6. RECENT ACHIEVEMENTS

This section contains a brief sketch of results achieved during the past six months. Most of results streaming out of Europe, North America, and Asia pertain to 1550 nm, but we are beginning to witness progress at longer wavelengths, highlighted here in Sections 6.2 and 6.3. In 2005, I proposed that silicon-integrated optoelectronics could be migrated into the wide, longwave infrared region that stretches from 1.6 to 200 μm . That migration will require innovative components whose dimensions are scaled-up from 1550 nm [12]. In a recent 2008 talk [5], I suggest that the time is ripe for chip-scale LWIR integration.

6.1. Results at 1550 nm

Modeling of an n+-doped layer of tensile Ge [10] predicts strong 1550-nm luminescence because the As doping populates the lower-energy L conduction valley, thereby transferring electrons from “excited L” into the Γ valley that sits at higher energy. Thus strong radiative recombination is obtained. I do not know whether the amount of electron-hole injection in a PNN⁺ diode will be adequate compared to that of a PIN diode. With regard to Sn-alloy emission experiments, the SiGeSn photoluminescence results of ASU [15, 16] are precursors of their electroluminescence studies. Their new SiSn alloy [16] is predicted to have a direct bandgap at 1460 nm when Si_{0.65}Sn_{0.35} is grown lattice-matched upon Ge_{0.88}Sn_{0.12}-buffered silicon.

FIGURE 4: Two designs for an SOI photonic-crystal dual-ring-resonator wavelength-division add-drop multiplexer optimized for (a) backward dropping, (b) forward dropping. (Illustrations taken from [18]).

On the topic of PCs, the first photonic crystal in a film of crystal Ge has been reported [17]. Strong luminescence from a point-defect resonant cavity in a 2D PC slab of GeOI was attained. On the topic of microring resonators, considerable progress has been made as evidenced by an experimental SOI photonic-wire fifth-order filter [14]. An alternative to the SOI strip ring has now surfaced in the form of the SOI 2D photonic-crystal ring resonator (PCRR) presented in [18, 19]. As shown in Figure 4, the dual-ring PCRR has a property not found in photonic-wire rings. It can drop a resonant wavelength in either the forward or the backward direction [18]. Also, the PCRR diameter can be made smaller than that of the microwire without suffering size-dependent losses like those present in the microwire resonators.

6.2. Results at the near and mid infrared

The $3.39\text{ }\mu\text{m}$ midinfrared silicon Raman amplifier reported by Bahram Jalali's group at UCLA represents an important migration of silicon photonics into the 3 to $5\text{ }\mu\text{m}$ atmospheric-transmission window [20]. The room temperature electrically pumped germanium MIS-diode laser developed in the group of Chee-Wee Liu appears to be

a world first [21]. This novel tunneling-injection device utilizes an unstrained bulk Ge crystal with a strip-shaped metal-insulator gate on the Ge top surface, plus a contact on the bottom Ge surface. This multimode laser has output lines from 1600 nm to 2140 nm, and there are temporal instabilities in the laser output associated with local heating under the gate.

I propose improvements to this MIS laser diode laser that would reduce indirect-bandgap effects and would increase infrared mode confinement under the gate without relying upon heating. Since the direct-gap wavelength of a $\text{Ge}_{1-x}\text{Sn}_x$ crystal film moves from 1550 nm in pure Ge to 1900 nm as 5% Sn is added to Ge, and since GeSn can be grown directly upon Si, the improved MIS laser would employ a $\sim 1\text{ }\mu\text{m}$ -high nearly direct GeSn stripe mesa waveguide upon a thin Si substrate. The emission wavelength would be in the 1900 to 2100 nm range. A multi-quantum-well GeSn/Ge active region would lase closer to 1600 nm.

As GeSn technology becomes mature, I feel that several practical GeSn/Si PIN laser diodes and photo diodes will be invented whose wavelengths-of-operation are from 1.8 to $2.5\text{ }\mu\text{m}$. At these near/mid-IR wavelengths, the attenuation of a glass optical fiber is too large for meter-scale transmission,

but the high-speed GeSn-transceiver fiber-optic links would work well over a few cm and fluoride fiber could serve for multimeter links.

6.3. Results at the far infrared

ASU researchers have demonstrated a relaxed-crystal SiGeSn buffer on silicon, offering a template for subsequent MQW epitaxy. This provides a real-world basis for design studies. A quantum-cascade laser design of a strain-free Ge/SiGeSn MQW lattice-matched to the ternary buffer was recently presented by Sun et al. [22]. This conduction intersubband device, a unique advance in Group IV technology, was predicted to have 120 cm^{-1} of gain at the $49\text{ }\mu\text{m}$ wavelength.

Because the deposited material $\text{Ge}_{0.23}\text{Sb}_{0.07}\text{Sn}_{0.70}$ has mid IR and far IR transparency, as well as CMOS compatibility, the low-loss GeSbS waveguides announced by the MIT group [23] appear to be good candidates for silicon-based LWIR on-chip networks.

7. OVERVIEW OF THIS SPECIAL ISSUE

As I read through the invited papers, I was impressed by their depth, diversity, timeliness, and innovation. The main themes of this issue are efficient silicon light sources (Gaburro et al.), optical switching and memory in photonic crystal nanocavities (Notomi et al.), macroporous silicon photonic crystals (Kitzerow et al.), hybrid evanescent III-V integration (Park et al.), light emitters in 3D Si/SiGe nanostructures (Lockwood et al.), chip-scale silicon photonic biosensors (Carracosa et al.), reflective gratings for photonic interconnects (Bidnyk et al.), high-speed waveguided Ge integrated photodetectors (Masini et al.), rare-earth doped silicon nano-emitters (Li et al.), foundry tools for photonic integration on CMOS (Fedeli et al.), gigascale silicon optical modulators (Basak et al.), sub-wavelength grating structures in SOI (Schmid et al.), low-cost silicon photonic links (Luff et al.), ion-implanted optical Bragg filters in SOI (Knights et al.), polarization control via stress induction (Xu et al.), electromagnetic modeling of silicon lasers (Prather et al.), engineering of material-photon interaction (Wada), and active photonic crystal devices for interconnects (Fauchet). The advances reported here lift silicon-integrated photonics to a higher level of capability and lay a foundation for further progress. These advances will help silicon reach preeminence in microphotonics.

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