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*Research Article*

# Large Area Silicon Carbide Vertical JFETs for 1200 V Cascode Switch Operation

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SiC VJFETs are excellent candidates for reliable high-power/temperature switching as they only use *pn* junctions in the active device area where the high-electric fields occur. VJFETs do not suffer from forward voltage degradation, exhibit excellent short-circuit performance, and operate at 300°C. 0.19 $cm^2$ 1200 V normally-on and 0.15 $cm^2$ low-voltage normally-off VJFETs were fabricated. The 1200-V VJFET outputs 53 A with a forward drain voltage drop of 2 V and a specific onstate resistance of 5.4 $m\Omega\,cm^2$. The low-voltage VJFET outputs 28 A with a forward drain voltage drop of 3.3 V and a specific onstate resistance of 15 $m\Omega\,cm^2$. The 1200-V SiC VJFET was connected in the cascode configuration with two Si MOSFETs and with a low-voltage SiC VJFET to form normally-off power switches. At a forward drain voltage drop of 2.2 V, the SiC/MOSFETs cascode switch outputs 33 A. The all-SiC cascode switch outputs 24 A at a voltage drop of 4.7 V.



## 1. INTRODUCTION

Wideband gap semiconductors like silicon carbide (SiC) and the III-IV nitrides are currently being developed for high-power/temperature applications. Silicon carbide (SiC) is ideally suited for power-conditioning applications due to its high saturated drift velocity, its mechanical strength, its excellent thermal conductivity, and its high critical field strength. For power devices, the tenfold increase in critical field strength of SiC relative to Si allows high-voltage blocking layers to be fabricated significantly thinner than those of comparable Si devices. This reduces device onstate resistance, and the associated conduction and switching losses, while maintaining the same high-voltage blocking capability. Figure 1 shows the theoretical specific onstate resistance of blocking regions designed for certain breakdown voltages in Si and 4H-SiC, under optimum punch-through conditions [1]. The specific onstate resistance of 4H-SiC is approximately 400 times lower than that of Si at a given breakdown voltage. This allows for high current operation at relatively low-forward voltage drop. In addition, the wide band gap of SiC allows operation at high temperatures where conventional Si devices fail. Forward voltage drop versus current density of Northrop Grumman's all-SiC vertical junction field effect transistor-(VJFET-) based cascode switch, and those of commercial Si MOSFET, Si IGBT, and Si CoolMOS switches are shown in Figure 2. The SiC switch has a lower voltage drop at a given current density, even at the elevated temperature of 150°C. The low-loss and the high-temperature operational capabilities of SiC devices can potentially eliminate the costly cooling systems present in today's Si based power electronics.

Presently, several SiC devices are being developed for 600 V (1200 V rating) power switching applications. SiC MOS-based devices show promise as normally-off power switches but suffer from low-MOS mobility and native oxide issues that limit reliable operation to below 175°C [2]. Furthermore, several temperature-dependant factors result in a decrease of the SiC MOSFET threshold voltage with temperature. This may lead to unwanted MOSFET turnon at temperatures over 200°C.

The SiC bipolar junction transistor is another normally-off power switching candidate. However, as with all SiC bipolar devices, its long term performance deteriorates due

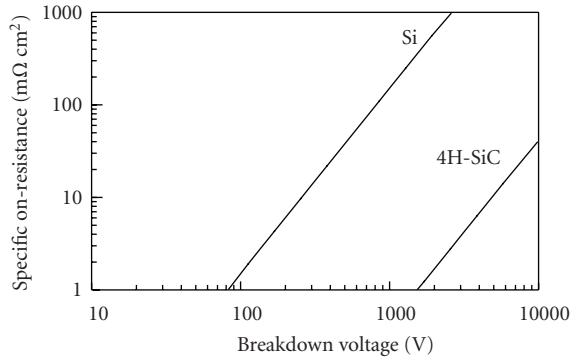


FIGURE 1: Theoretical specific onstate resistance of blocking regions designed for certain breakdown voltages in Si and 4H-SiC, under optimum punch-through conditions.

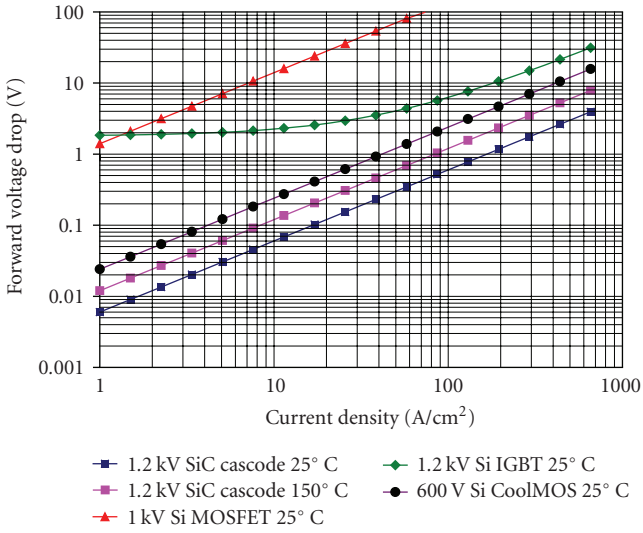


FIGURE 2: Forward voltage drops versus current densities of Northrop Grumman's all-SiC VJFET-based cascode switch and of commercial Si MOSFET, Si IGBT, and Si CoolMOS switches. The SiC switch has a lower measured voltage drop at a given current density, even at the elevated temperature of 150°C.

to forward bias voltage degradation [3]. Also, the BJT is a current controlled device that can require substantial base drive current [4].

The SiC VJFET is a very promising candidate for high-power/temperature switching as it only uses *pn* junctions in the active device area, where the high-electric fields occur, and can therefore fully exploit the high-temperature properties of SiC in a gate voltage controlled switching device. VJFETs for high voltage applications are typically normally-on devices, and an all-SiC normally-off power switch can be implemented by combining a high-voltage normally-on VJFET with a low-voltage normally-off VJFET in the cascode configuration.

In this paper, we review the reliability and high temperature characteristics of $1.25 \times 10^{-3}\,\text{cm}^2$ area unipolar ion-implanted SiC VJFETs. Subsequently, we present the forward

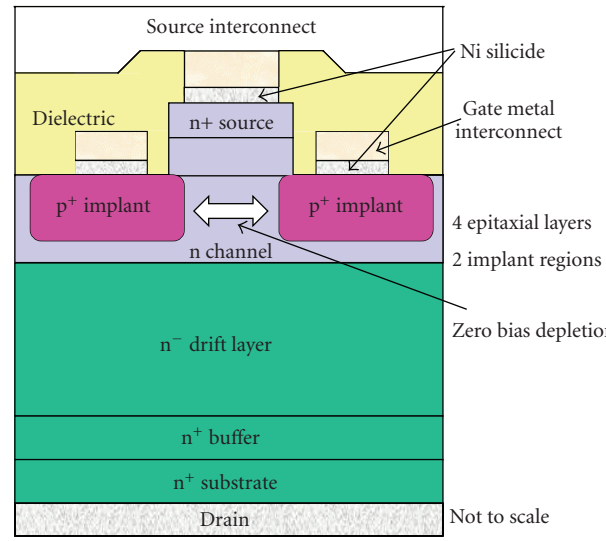


FIGURE 3: Simplified cross-section schematic of a normally-on ion-implanted SiC VJFET. The layer dimensions are not to scale.

current and blocking voltage characteristics of $0.19\,\text{cm}^2$ area 1200 V normally-on and $0.15\,\text{cm}^2$ area low-voltage normally-off SiC VJFETs. The $0.19\,\text{cm}^2$ 1200-V VJFETs have been connected in the cascode configuration with Si MOSFETs and $0.15\,\text{cm}^2$ low-voltage SiC VJFETs to form normally-off power switches.

## 2. SIC VJFET STRUCTURE

A cross-section schematic of a high-voltage *p*+ ion-implanted 4H-SiC VJFET is shown in Figure 3.

The channel layer is doped to low $10^{16}\,\text{cm}^{-3}$, and the drift layer is doped to mid $10^{15}\,\text{cm}^{-3}$. To ensure >1200 V blocking, a 12 $\mu$m drift layer thickness is used. The substrates and epitaxy are grown by commercial vendors. In the on-state, majority carriers (electrons) flow vertically from source to drain. To control the current through the device, the gates are subjected to a voltage, which adjusts the width of the depletion regions between the *p*-type gates in the *n*-type channel. In normally-off VJFETs, the *p*+ implant depletion regions must overlap at 0 V gate bias. Reducing the gate-to-gate spacing leads to higher depletion region overlap and the VJFET blocks increasingly higher drain voltages. For larger gate-to-gate separations, the 0 V gate bias depletion regions do not overlap and the VJFET is normally-on.

As the normally-off VJFET need only block low voltages in cascode switching operation, its drift layer is approximately 2.5 $\mu$m to minimize onstate resistance and losses.

To ensure high-voltage operation with minimum associated onstate resistance, a robust, self-aligned, multiple floating guard-ring edge termination was designed and fabricated. The high-voltage VJFETs (12 $\mu$m drift layer doped at mid $10^{15}\,\text{cm}^{-3}$) exhibited breakdown voltages of up to 2022 V, which corresponds to a record 93% of the calculated 4H-SiC material limit [5]. The measured specific onstate

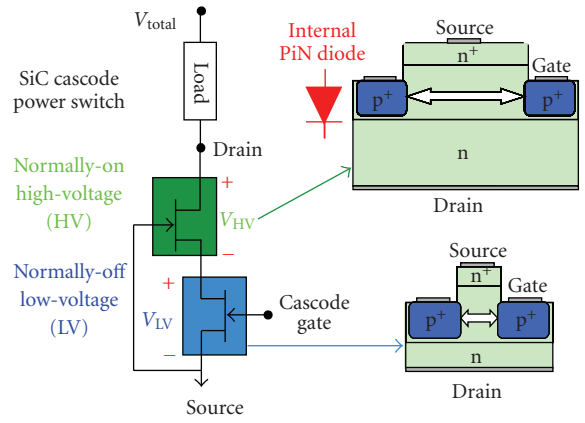


Figure 4: Schematic of Northrop Grumman's all-SiC power switch consisting of high-voltage normally-on and low-voltage normally-off VJFETs connected in the cascode configuration.

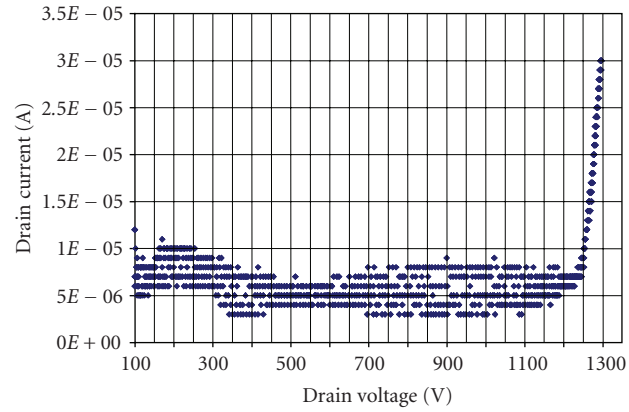


Figure 5: An all-SiC cascode switch blocking 1250 V when normally-off (gate-to-source bias $V_{gs} = 0$ V).

resistance was 2.1 m$\Omega$ cm$^2$, a value close to the theoretical limit of the 4H-SiC material, Figure 1 [6].

Initially, limited by the low 4H-SiC material quality, and the high micropipe defect density in particular, "small" $1.25 \times 10^{-3}$ cm$^2$ area VJFETs were fabricated and paralleled to increase current output. The small area VJFET manufacturing was optimized and high yield with excellent wafer parameter uniformity were achieved [7, 8].

## 3. SIC VJFET CASCODE RELIABILITY AND HIGH-TEMPERATURE OPERATION

To assess the reliability of the $1.25 \times 10^{-3}$ cm$^2$ area VJFETs, the forward voltage drops across the VJFET's gate-to-drain and gate-to-source *pn* junctions were measured at constant junction current densities of 100 A/cm$^2$. After 500 hours of continuous room temperature operation under this DC bias condition, no measurable forward voltage drift was detected [9].

Additionally, 1200 V SiC VJFETs were subjected to short-circuit testing to determine the survivability time prior to the onset of catastrophic device failure. The SiC VJFETs exhibited hold-off times in excess of 1 millisecond, a sixfold improvement over Si MOSFETs of similar voltage rating [9].

To implement all-SiC normally-off power switches, high voltage normally-on and low-voltage normally-off VJFETs were connected in the cascode configuration. A schematic of the cascode switch and its constituent VJFETs are shown in Figure 4. The switches are voltage-driven, and have exhibited excellent power switching characteristics including low onstate resistance, high speed, and low switching losses [10]. A typical breakdown voltage curve of a normally-off (1250 V at $V_{gs}$= 0 V) all-SiC cascode switch is shown in Figure 5.

The cascode switch's internal PiN diode has exhibited a very fast 100 nanoseconds reverse recovery time, Figure 6, which can potentially eliminate the need for external diodes in power switching circuits [11]. A half-bridge inverter was demonstrated using SiC cascode switches with no external

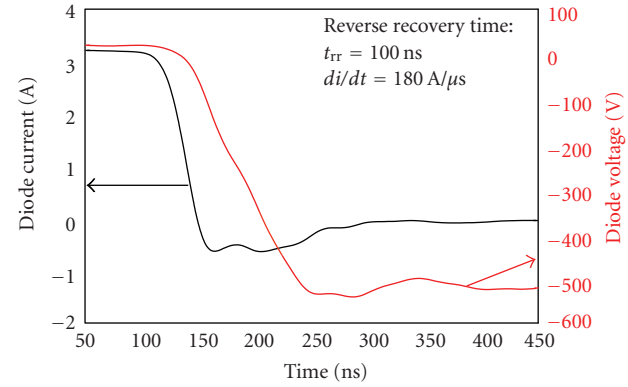


Figure 6: The very fast 100 nanoseconds reverse recovery time of the cascode switch's internal diode.

antiparallel diodes. The inverter consisted of high-side and low-side cascode switches that were pulse-width modulated from a 500 V bus to produce a 60 Hz sinuso at the output [11].

The high-temperature operational capability of SiC VJFETs is crucial in eliminating costly cooling in power systems. To investigate the effect of temperature on blocking voltage, the blocking characteristics of a normally-off VJFET were measured at 25°C and 300°C junction temperatures. At a given gate-to-source bias $V_{gs}$, the blocking voltage decreases with temperature as shown in Figure 7. This is in agreement with theory as the reverse-bias drain-to-source leakage current increases with temperature, due to the higher number of thermally generated carriers. The measurements were performed using a Tektronix 371 A curve tracer. As the 300°C measurement setup required modification of the curve tracer's looping compensation, the 25°C and 300°C leakage current levels cannot be directly compared.

The effect of temperature on the onstate drain current of the cascode switch is illustrated in Figure 8 at junction temperatures of 25°C and 300°C, for gate-to-source biases of 0 to 3 V in steps of 0.5 V.

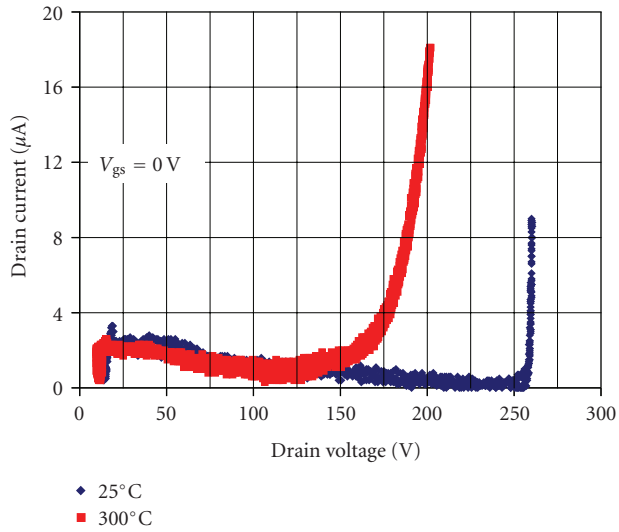


Figure 7: Blocking voltage characteristics of the cascode switch's $N_{off}$ VJFET at 25°C (blue line), and 300°C (red line). The gate-to-source bias is $V_{gs}$ = 0 V.

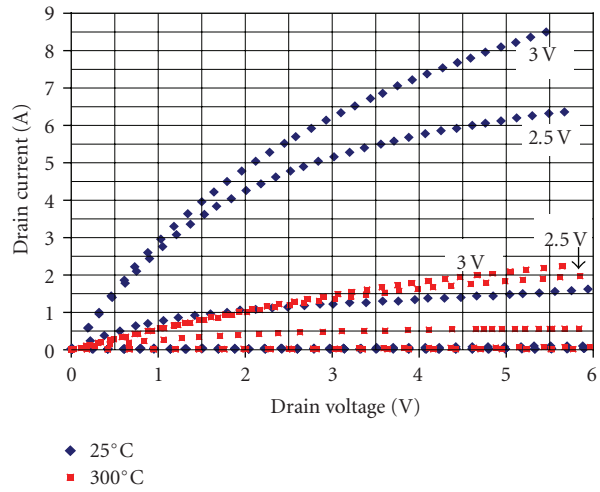


Figure 8: Onstate drain current curves of a 1200 V SiC cascode switch at 25°C (blue) and 300°C (red) junction temperatures. The gate-to-source bias ranges from 0 to 3 V in steps of 0.5 V.

As VJFETs do not have gate oxides, they reliably operate at junction temperatures of 300°C. The measured drop in current with increasing temperature in Figure 8 is in good agreement with the theoretical reduction in SiC electron mobility. As the channel and drift regions are designed independently in VJFETs, the onstate resistance can be tuned for maximum current output [12].

## 4. LARGE AREA VJFETs

To meet the current handling requirements of modern power conditioning systems, 1200 V normally-on VJFETs of 0.19 cm$^2$ area (4.4 mm × 4.33 mm) were manufactured. Excluding the bonding pads and edge termination region,

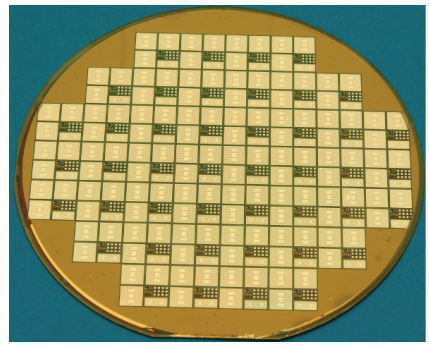

Figure 9: 0.19 cm$^2$ VJFETs fabricated on a 3-inch 4H-SiC wafer.

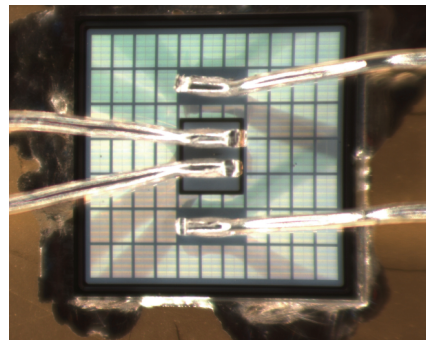

Figure 10: A 0.19 cm$^2$ area VJFET soldered into a package and wire bonded using 10 mil thickness aluminium wires.

the active area as defined by the pn-junctions is 0.143 cm$^2$. A photograph of large area VJFETs fabricated on a 3-inch 4H-SiC wafer is shown in Figure 9.

Large area VJFETs were soldered into packages and wire bonded using thick aluminum wires, Figure 10.

To attain the desirable 1200 V blocking voltage capability, a 12 $\mu$m drift layer with a doping concentration in the mid $10^{15}$ cm$^{-3}$ was used. The blocking voltage characteristics of the 0.19 cm$^2$ VJFET were measured with a Tektronix 371 A curve tracer and are shown as a function of gate voltage in Figure 11. At a gate-to-source bias of −24 V, the VJFET blocks 1680 V at a drain current density of 1 mA/cm$^2$.

Room-temperature pulsed onstate drain current measurements were performed on packaged 1200-V VJFETs (single chip), at a gate bias range of 0 to 3 V in steps of 0.5 V, Figure 12. At a gate bias of 2.5 V, the VJFET's drain current is 40 A with a forward drain voltage drop of 1.5 V and a specific onstate resistance of 5.4 mΩ cm$^2$. The current density is 280 A/cm$^2$, and the power density is 420 W/cm$^2$. The gate current at $V_{gs}$= 2.5 V is 12 mA, which results in a transistor current gain of 3333. At the same gate bias of 2.5 V, the VJFET outputs a drain current of 53 A at a forward drain voltage drop of 2 V. The current density is 371 A/cm$^2$, and the power density is 741 W/cm$^2$, which is within the heat load capability of advanced water-cooled packages [13]. The specific onstate resistance is 5.4 mΩ cm$^2$, and the transistor current gain is 4417. A drain current of 100 A at a forward

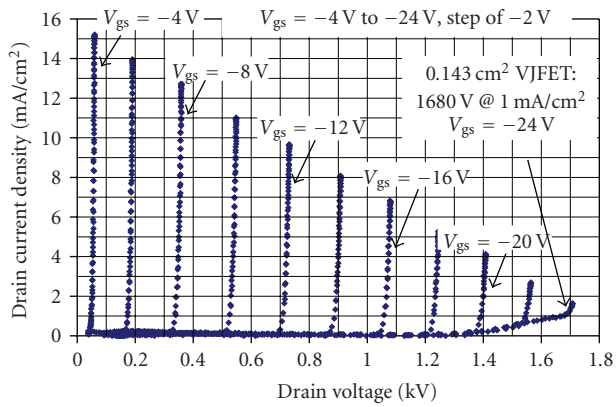


Figure 11: Blocking voltage characteristics of a 0.143 cm$^2$ active area VJFET at gate biases of −4 V to −24 V, in steps of −2 V. At a gate-to-source bias of −24 V and a drain current density of 1 mA/cm$^2$, the VJFET blocks 1680 V.

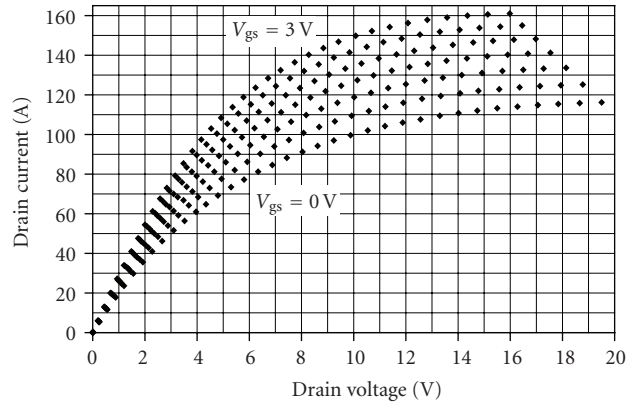


Figure 12: Onstate drain current characteristics versus drain voltage characteristics of a high-voltage 0.143 cm$^2$ active area packaged VJFET, at a gate-to-source bias range of 0 to 3 V in steps of 0.5 V. At a gate-to-source bias of 2.5 V (with a gate current of 12 mA), the VJFET outputs 53 A and 100 A at forward drain voltage drops of 2 V and 4.8 V, respectively.

drain voltage drop of 4.8 V is measured at a gate bias of 2.5 V (gate current of 12 mA).

Finally, a record high onstate current of 161 A is measured at a drain voltage drop of 16 V, for a gate bias of 3 V. Although biasing the gate *pn* junction above its ∼2.7 V built-in potential increases drain current, it can seriously degrade current gain. Therefore, in practical power switching circuits, the gate driver biases the *pn* junction below its built-in potential.

As pointed out earlier and evident from the blocking voltage characteristics presented in Figure 11, the 0.143 cm$^2$ 1200-V VJFET is designed normally-on to minimize onstate resistance and maximize current gain. Presently, inherently safe operation gate-drive circuits are being developed to utilize normally-on SiC VJFETs as power switches [14, 15]. However, most circuit designers require a normally-off SiC-

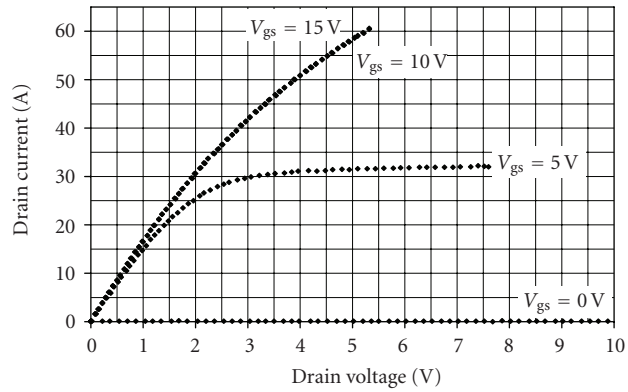


Figure 13: Onstate drain current characteristics of a switch consisting of a single 0.143 cm$^2$ active area 1200-V SiC VJFET connected in the cascode configuration with two paralleled 75-V/97-A commercial silicon MOSFETs. At a MOSFET gate-to-source bias of 15 V, the cascode switch outputs 33 A at a forward drain voltage drop of 2.2 V.

based switch as a direct replacement to silicon MOSFETs or IGBTs. Connecting a high-voltage, low onstate resistance SiC VJFET in the cascode configuration with a low-voltage silicon power MOSFET creates a normally-off power switch with a control characteristic similar to a silicon MOSFET or IGBT [16]. The cascode circuit diagram is similar to the one that appears in Figure 4, with the low-voltage normally-off part being a silicon MOSFET.

In the cascode configuration and with the MOSFET being biased in the on state, the 1200-V SiC VJFET and the Si MOSFET operate in series, with the gate of the 1200-V SiC VJFET automatically biased at a voltage value equal to the negative of the drain-to-source voltage drop across the low-voltage Si MOSFET. In the offstate, the MOSFET's drain-to-source blocking voltage provides the necessary negative gate bias to pinch off the 1200-V SiC VJFET. After the VJFET is pinched off, further increase in reverse voltage at the drain of the cascode is supported by the 1200-V SiC VJFET.

The 1200-V SiC VJFET, whose onstate characteristics appear in Figure 12, was connected in the cascode configuration with two paralleled commercial 75-V/97-A rated silicon MOSFETs.The onstate drain current characteristics versus drain voltage of the resulting cascode switchwere measured at MOSFET gate biases of 0 V, 5 V, 10 V, and 15 V, Figure 13. At a MOSFET gate-to-source bias of 15 V, the cascode switch outputs 33 A at a forward drain voltage drop of 2.2 V. Under these biasing conditions, the gate of the 1200-V SiC VJFET experiences a bias equal to the negative of the measured 0.2 V drain-to-source voltage drop across the MOSFETs. The forward voltage drop across the 1200-V SiC-VJFET component of the cascode switch is 2 V. Its current and power densities are 231 A/cm$^2$ and 462 W/cm$^2$, respectively.

The SiC-VJFET/Si-MOSFET normally-off power switch exploits the high-blocking voltage with low onstate resistance capability of the 1200-V SiC VJFET. However, the Si MOSFET sets an upper limit on temperature operation and introduces gate oxide capacitance. To overcome these

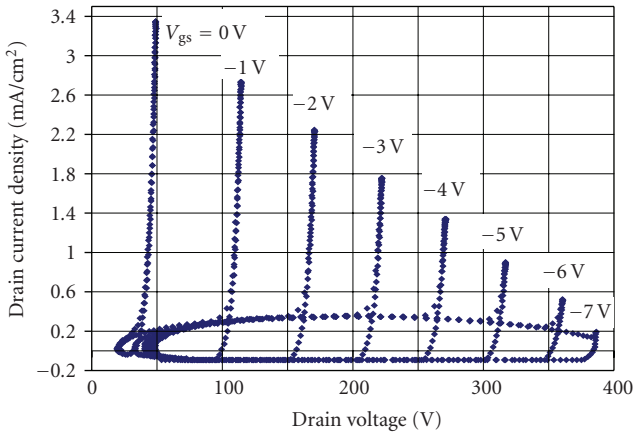


Figure 14: Blocking voltage versus gate bias characteristics of a 0.13 cm$^2$ active area low-voltage normally-off SiC VJFET. At a gate-to-source bias of 0 V and a drain current density of 1 mA/cm$^2$, the VJFET blocks 44 V (normally off to 44 V).

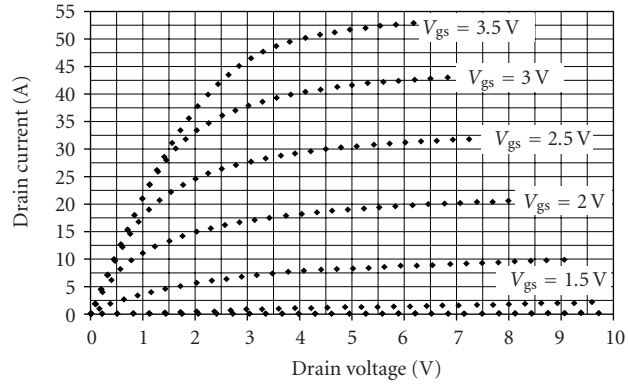


Figure 15: Onstate drain current characteristics versus drain voltage characteristics of a 0.13 cm$^2$ active area low-voltage normally-off packaged VJFET. Gate biases of 0 to 3.5 V were applied, in steps of 0.5 V. At a gate bias of 2.5 V, the VJFET outputs 28 A at a forward drain voltage drop of 3.3 V.

limitations and exploit the high-temperature capability of SiC, a 0.15 cm$^2$ SiC VJFET was fabricated to be used as the low-voltage normally-off component of the cascode switch (Figure 4). Excluding the bonding pads and edge termination regions, the low-voltage normally-off VJFET's pn-junction active area is 0.13 cm$^2$. Its blocking voltage characteristics at different gate biases are demonstrated in Figure 14. The device has a thin 2.5 $\mu$m drift layer to minimize onstate resistance and losses, and blocks 44 V at zero gate-to-source bias with a drain current density of 1 mA/cm$^2$.

Room temperature onstate drain current measurements were performed on the low-voltage normally-off 0.15 cm$^2$ VJFETs at a gate bias range of 0 to 3.5 V, Figure 15.

At a gate bias of 2.5 V, the VJFET's drain current is 28 A with a forward drain voltage drop of 3.3 V and a specific onstate resistance of 15 m$\Omega$ cm$^2$. The current and power densities are 215 A/cm$^2$ and 711 W/cm$^2$, respectively. A drain current of 50 A at a forward drain voltage drop of 4 V is measured at a gate bias of 3.5 V. As the low-voltage VJFET is designed for normally-off operation, it is more resistive than the normally-on 1200-V VJFET of Figure 12, and consequently outputs less current under similar drain biasing conditions.

To implement a 1200 V all-SiC normally-off power switch similar to the one schematically shown in Figure 4, a single 0.143-cm$^2$ 1200-V SiC VJFET was connected in the cascode configuration with a single 0.13 cm$^2$ low-voltage SiC VJFET. Room temperature onstate drain current measurements were performed at cascode gate biases of 0 to 3.5 V, Figure 16.

At a cascode gate bias of 2.5 V, the all-SiC cascode switch outputs 24 A at a forward drain voltage drop of 4.7 V. At this biasing condition, drain voltages of 2.8 V and 1.9 V are dropped across the 1200-V and low-voltage VJFETs, respectively. The current and power densities are 168 A/cm$^2$ and 470 W/cm$^2$ for the 1200-V VJFET, and 185 A/cm$^2$ and 351 W/cm$^2$ for the low-voltage VJFET. In forward cascode operation, the gate of the 1200-V VJFET is biased at a voltage value equal to the negative of the drain-to-source voltage drop across the low-voltage VJFET (Figure 4). Thus, the gate of the 1200-V VJFET is biased at −1.9 V when 4.7 V are dropped across the cascode switch.

In the SiC-VJFET/Si-MOSFETs cascode, a current of 33 A passes through the switch at a forward drain bias of 2.2 V, Figure 13. This is higher than the 24 A current of the all-SiC cascode under similar 1200-V VJFET power density biasing conditions. The mature Si wafer technology allows the fabrication of MOSFETs of a larger size, which minimizes their resistance and voltage drop. Consequently, at a power density of about 470 W/cm$^2$ on the 1200-V VJFET of the cascode, the gate of the 1200-V SiC VJFET is biased at the −0.2 V MOSFET voltage drop in the SiC-VJFET/Si-MOSFETs case, and at the −1.9 V low-voltage VJFET voltage drop in the all-SiC cascode case. This difference in 1200-V VJFET gate bias is responsible for the disparity in cascode current outputs under similar power density biasing conditions. Paralleling multiple low-voltage SiC VJFETs will minimize the voltage drop on the low-voltage portion of the all-SiC cascode switch and lead to higher cascode current output.

Operating the 1200-V SiC VJFET as a switch in an inherently safe gate-drive circuit eliminates the need for a low-voltage normally-off SiC VJFET cascode component. Moreover, in a 1200-V normally-on VJFET switch a gate bias of 2.5 V (12 mA gate current) can be applied, which allows for high-current/high-gain operation with low onstate resistance, Figure 12.

In a cascode switch, the gate of the high-voltage VJFET is biased at a voltage value equal to the negative of the drain-to-source voltage drop across the low-voltage component. Hence, in forward cascode operation, the high-voltage VJFET's gate is always at a negative bias, which lowers current output and increases onstate resistance. To visualize the impact of negative gate bias on the 1200-V VJFET of the cascode, the onstate drain current characteristics of the 0.143-cm$^2$ 1200-V VJFET are plotted at a gate bias range of 0 to −4.5 V in steps of 0.5 V, Figure 17.

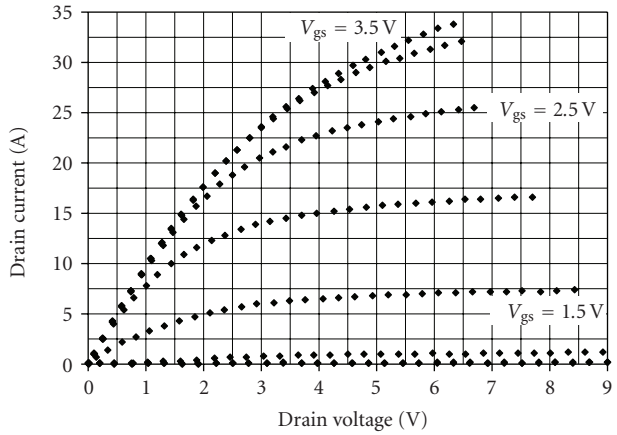


Figure 16: Onstate drain current characteristics versus drain voltage characteristics of an all-SiC cascode switch consisting of a low-voltage 0.13 cm$^2$ active area VJFET and a 1200-V 0.143 cm$^2$ active area VJFET. The measurements were taken at cascode gate biases of 0 to 3.5 V, in steps of 0.5 V. At a cascode gate bias of 2.5 V, the switch outputs 24 A with a forward drain voltage drop of 4.7 V.

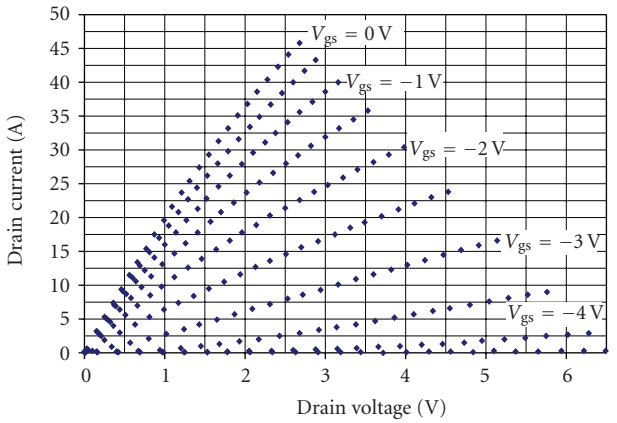


Figure 17: Onstate drain current versus drain voltage characteristics of a 1200-V 0.143-cm$^2$ active area packaged VJFET at a gate bias range of 0 to −4.5 V, in steps of 0.5 V. At a gate-to-source bias of −4.5 V, the VJFET is pinched off and negligible current flows through its drain.

It is evident from Figure 17 that 1200-V VJFET current output decreases nonlinearly with negative bias on its gate. Thus, the voltage drop across the low-voltage cascode component limits the current output of the entire cascode by reverse biasing the gate of the 1200-V VJFET. At −4.5 V gate bias, the VJFET turns off and negligible current flows through its drain.

## 5. CONCLUSION

The SiC VJFET is a very promising candidate for reliable high-power/temperature switching as it only uses *pn* junctions in the active device area where the high-electric fields occur. VJFETs do not suffer from forward voltage degradation, and exhibit holdoff times higher than those of their Si counterparts in short circuit testing. The VJFET based all-SiC normally-off cascode switch's internal diode has exhibited a very fast 100 nanoseconds reverse recovery time, eliminating the need for antiparallel diodes in power switching circuits. VJFETs were successfully operated at 300°C junction temperature. The measured reduction in onstate current is in good agreement with the theoretical reduction in SiC electron mobility.

To meet the current handling requirements of modern power conditioning systems, 1200 V normally-on VJFETs of 0.19 cm$^2$ and low-voltage normally-off VJFETs of 0.15 cm$^2$ areas were fabricated. At a gate bias of 2.5 V, the 1200-V VJFET outputs 53 A with a forward drain voltage drop of 2 V and a specific onstate resistance of 5.4 mΩ cm$^2$. The low-voltage VJFET's drain current is 28 A, at a gate bias of 2.5 V, with a forward drain voltage drop of 3.3 V and a specific onstate resistance of 15 mΩ cm$^2$.

A 1200-V SiC VJFET was connected in the cascode configuration with two commercial Si MOSFETs to form a normally-off power switch. At a MOSFET gate-to-source bias of 15 V, the cascode switch outputs 33 A at a forward drain voltage drop of 2.2 V. To fully exploit the high-temperature capability of SiC in a normally-off power switch, a 0.15 cm$^2$ low-voltage normally-off SiC VJFET was connected with a 0.19 cm$^2$ 1200-V normally-on VJFET in the cascode configuration. At a forward drain voltage drop of 4.7 V, the all-SiC cascode switch outputs 24 A at 2.5 V cascode gate bias. Operating the 1200 V normally-on SiC VJFET as a switch in an inherently safe gate-drive circuit eliminates the need for a low-voltage normally-off SiC VJFET cascode component, and enables high-current/high-gain operation with low voltage drop and low onstate resistance.

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