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Research Article

A Novel Soft-Switching Synchronous Buck Converter for Portable Applications

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This paper proposes a zero-voltage-transition (ZVT) pulse-width-modulated (PWM) synchronous buck converter, which is designed to operate at low voltage and high efficiency typically required for portable systems. A new passive auxiliary circuit that allows the main switch to operate with zero-voltage switching has been incorporated in the conventional PWM synchronous buck converter. The operation principles and a detailed steady-state analysis of the ZVT-PWM synchronous converter implemented with the auxiliary circuit are presented. Besides, the main switch and all of the semiconductor devices operate under soft-switching conditions. Thus, the auxiliary circuit provides a larger overall efficiency. The feasibility of the auxiliary circuit is confirmed by simulation and experimental results.

1. INTRODUCTION

Current trends in consumer electronics demand progressively lower-voltage supplies. Portable electronics equipment, such as laptop computers, cellular phones, and future microprocessor and memory chips, requires low-power circuitry to maximize battery run time. Because of significantly lower conduction losses, synchronous rectifiers are now used in essentially all low-voltage DC power supplies [1–4]. A synchronous rectifier is an electronic switch that improves power-conversion efficiency by placing a low-resistance conduction path across the diode rectifier in a switch-mode regulator. MOSFETs usually serve this purpose.

However, higher input voltages and lower output voltages have brought about very low duty cycles, increasing switching losses and decreasing conversion efficiency. So in this paper, we have optimized the efficiency of the synchronous buck converter by eliminating switching losses using soft-switching technique. The voltage-mode soft-switching method that has attracted most interest in recent years is the zero-voltage transition [5–24]. This is because of its low additional conduction losses and because its operation is closest to the PWM converters. The auxiliary circuit of the ZVT converters is activated just before the main switch is turned on and ceases after it is accomplished. The auxiliary circuit components in this circuit have lower ratings than those in the main power circuit because the auxiliary circuit is active for only a fraction of the switching cycle; this allows a device that can turn on with fewer switching losses than the main switch to be used as the auxiliary switch. The improvement in efficiency caused by the auxiliary circuit is mainly due to the difference in switching losses between the auxiliary switch and the main power switch if it were to operate without the help of the auxiliary circuit. Previously proposed ZVT-PWM converters have at least one of the following key drawbacks. (i) The auxiliary switch is turned off while it is conducting current. This causes the switching losses and EMI to appear, which offsets the benefits of using the auxiliary circuit. In converters such as the ones proposed in [6, 12, 15, 16], the turnoff is very hard. (ii) The auxiliary circuit causes the main converter switch to operate with a higher peak current stress and with more circulating current. This results in the need for a higher current-rated device for the main switch and an increase in conduction losses. The converters proposed in [5, 8, 9, 13, 14, 17] are having high current stresses on the main switch. (iii) The auxiliary circuit

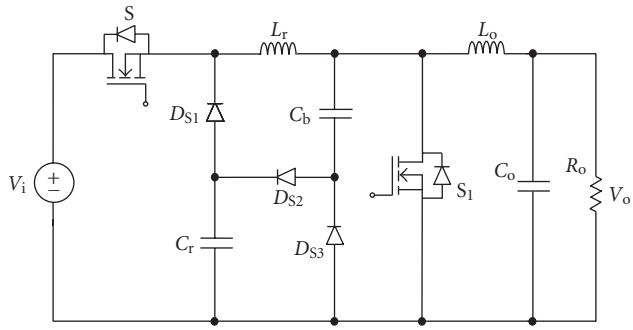

Figure 1: The proposed synchronous buck converter.

components have high voltage and/or current stresses, such as converters proposed in [5, 8, 9, 14, 17]. The converter proposed in [23] reduces the current stress on the main switch, but the circuit is very complex. (iv) In addition, most active circuits are seriously criticized due to their complexity, high cost, difficult control, large circulating energy, excessive voltage and current stresses, and also narrow line and load ranges. Additionally, it has been reported that the passive circuits are cheaper and more reliable and have a higher performance/cost ratio than the active ones [25, 26].

Reducing switching losses for low-power circuit such as synchronous buck is not known to be present in the literatures [1–26]. The converter shown in Figure 1 is designed for a low-voltage, high-current circuit, and it is found to be highly efficient. Hence, this paper presents a new class of ZVT synchronous buck converters. By using a resonant auxiliary network, the proposed converters achieve zero-voltage switching for the main switch and synchronous switch, and zero-current switching for the auxiliary switch without increasing their voltage and current stresses.

The paper is organized as follows. Section 2 gives a short description of the proposed circuit followed by a review of the various modes of operation with their key waveforms and the representation of their equivalent operation modes and analysis. Section 3 presents the design considerations and Section 4 includes basic features of the converter. Section 5 includes simulation and experimental results to illustrate the features of the proposed converter scheme. Section 6 includes some conclusions.

2. THE ZVT-PWM SYNCHRONOUS BUCK CONVERTER

2.1. Circuit description and assumption

The ZVT-PWM synchronous buck converter is shown in Figure 1. It is the combination of the conventional PWM synchronous buck converter and the proposed auxiliary snubber circuit. The auxiliary circuit consists of a resonant inductor L_r, resonant capacitor C_r, a buffer capacitor C_b, and three auxiliary Schottky diodes D_{S1}, D_{S2}, and D_{S3}. Body diodes of main switch S and synchronous switch S_1 are also utilized in this converter.

To analyze the steady-state operations of the proposed circuit, the following assumptions are made during one switching cycle.

(1) Input voltage V_i is constant.
(2) Output voltage V_o is constant or output capacitor C_o is large enough.
(3) Output current I_o is constant or output inductor L_o is large enough.
(4) Output inductor L_o is much larger than resonant circuit inductor L_r.
(5) Resonant circuits are ideal.
(6) Semiconductor devices are ideal.
(7) Reverse recovery time of all diodes is ignored.

2.2. Operation principles and analysis

Based on these assumptions, circuit operations in one switching cycle can be divided into eight stages. The key waveforms of these stages are given in Figure 2 and the equivalent circuit schemes of the operation stages are given in Figure 3. The detailed analysis of every stage is presented as follows.

Mode 1 t_0-t_1. Prior to t_1, the body diode of switch S_1 was conducting, while the main switch S was off. The equations $i_S = 0$, $i_{D1} = I_o$, $i_{Lr} = 0$, $v_{Cr} = 0$, $v_{Cb} = 0$ are valid at the beginning of this stage. At $t = t_0$, the main switch is turned on, which realizes zero-current turn-on as it is in series with the resonant inductor L_r. During this stage, i_{Lr} rises and current i_{D1} through body diode of switch S_1 falls simultaneously at the same rate linearly. The mode ends at $t = t_1$ when i_{Lr} reaches I_o and i_{D1} becomes zero. The body diode D_1 is turned off with ZVS because of C_r and C_b being existent. In this state,

$$\begin{aligned} i_S &= i_{Lr} = \frac{V_i}{L_r}(t - t_0), \\ i_{D1} &= I_o - i_{Lr} = -\frac{V_i}{L_r}(t - t_0) + I_o, \\ t_{01} &= \frac{L_r}{V_i} I_o. \end{aligned} \tag{1}$$

Mode 2 t_1-t_2. The diode D_{S2} starts conducting at the instant when body diode D_1 is turned off. At $t = t_1$, $I_S = i_{Lr} = I_o$, $i_{D1} = 0$, $v_{Cr} = 0$, and $v_{Cb} = 0$. In this interval, resonance occurs with the inductor L_r and capacitors C_r and C_b. This mode ends with C_r charged up to the input voltage V_i;

$$\begin{aligned} i_{Lr}(t - t_1) &= \frac{V_i}{Z_1} \sin \omega_1 (t - t_1) + I_o, \\ v_{Cr}(t - t_1) &= \frac{C_e}{C_r}[- V_i \cos \omega_1 (t - t_1) + V_i], \\ v_{Cb}(t - t_1) &= \frac{C_e}{C_b}[- V_i \cos \omega_1 (t - t_1) + V_i], \end{aligned} \tag{2}$$

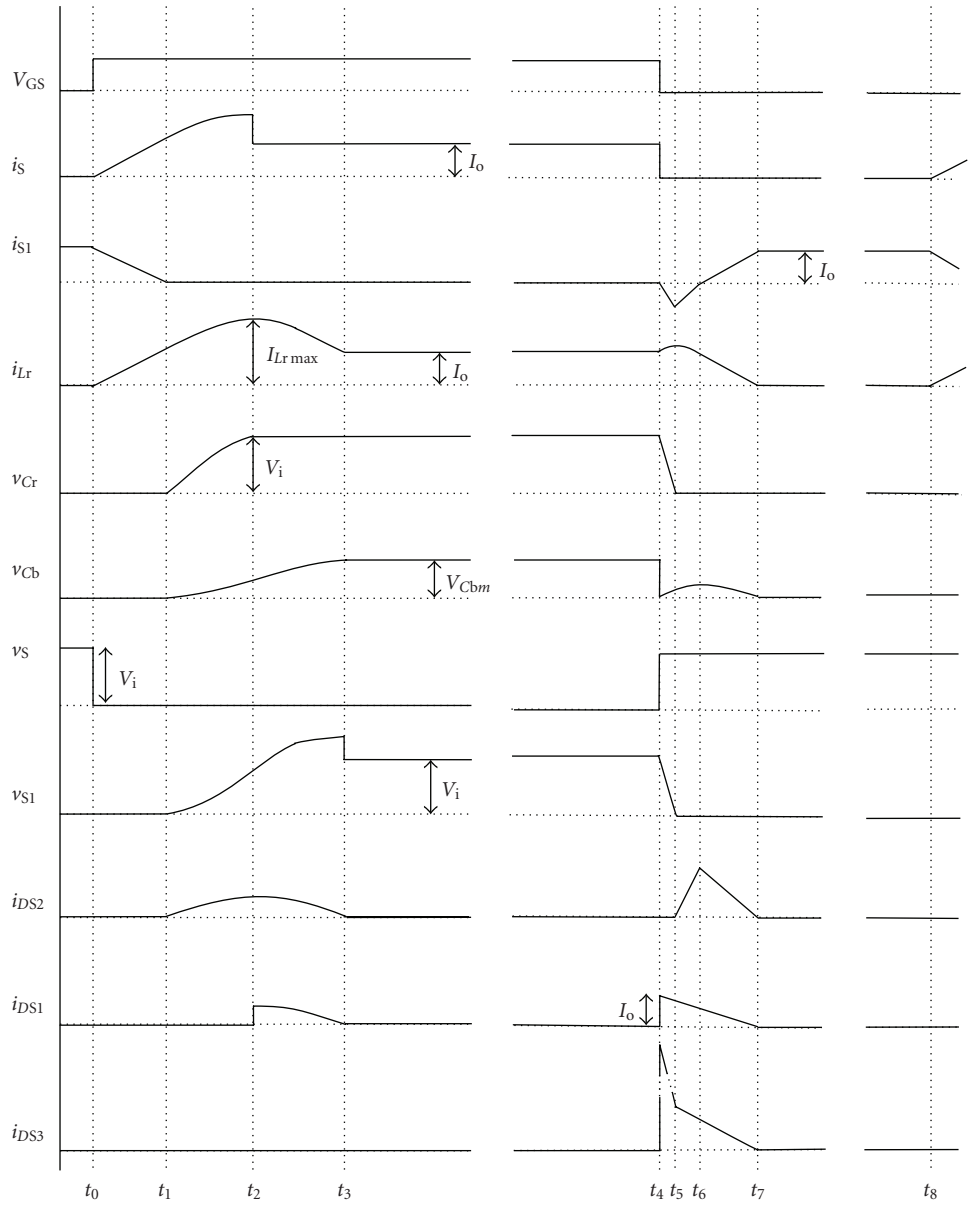

Figure 2: Key theoretical waveforms of the proposed converter.

where

$$C_e = \frac{C_r C_b}{C_r + C_b},$$
$$\omega_1 = \frac{1}{\sqrt{L_r C_e}}, \tag{3}$$
$$Z_1 = \sqrt{\frac{L_r}{C_e}}.$$

The diode D_{S1} is turned on with ZVS at the moment when v_{Cr} becomes V_i. In this state,

$$t_{12} = \frac{1}{\omega_1}\sin^{-1}\left(\frac{C_r}{C_e} - 1\right). \tag{4}$$

Mode 3 t_2-t_3. At $t = t_2$, $i_S = I_o$, $i_{Lr} = i_{Lr\,max}$, $v_{Cr} = V_{Cr\,max} = V_i$, and $v_{Cb} = V_{Cb1}$. When diode D_{S1} turns on, new resonance starts with L_r and C_b. This mode ends when i_{Lr} becomes equal to load current I_o, and C_b is charged up to its maximum voltage V_{Cbm}. Both diodes D_{S1} and D_{S2} are turned off under ZCS due to the existence of L_r. The voltage and current expressions that govern this circuit mode are given by

$$\begin{aligned} i_{Lr}(t - t_2) &= (I_{Lr\,max} - I_o)\cos\omega_2(t - t_2) \\ &\quad - \frac{V_{Cb1}}{Z_2}\sin\omega_2(t - t_2) + I_o, \\ v_{Cb}(t - t_2) &= (I_{Lr\,max} - I_o)Z_2\sin\omega_2(t - t_2) \\ &\quad + V_{Cb1}\cos\omega_2(t - t_2). \end{aligned} \tag{5}$$

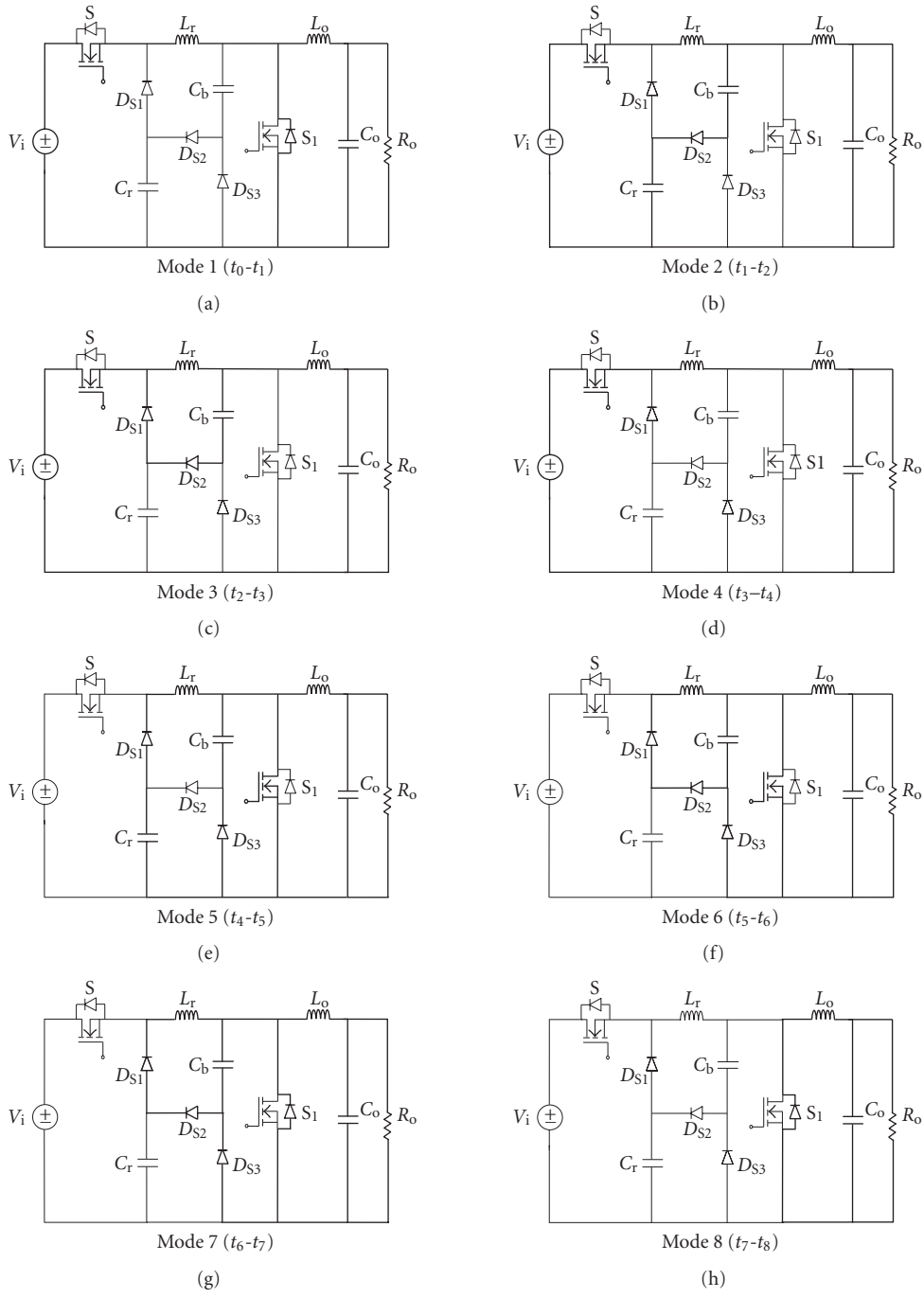

Figure 3: Modes of operation.

The time interval of this stage can be found as follows:

$$t_{23} = \frac{1}{\omega_2}\tan^{-1}\left(\frac{I_{Lr\max} - I_o}{V_{Cb1}}\right), \tag{6}$$

where

$$\omega_2 = \frac{1}{\sqrt{L_r C_b}}, \qquad Z_2 = \sqrt{\frac{L_r}{C_b}}. \tag{7}$$

Mode 4 t_3-t_4. Since both diodes D_{S1} and D_{S2} have been turned off at t_3, now only the main switch S and inductor L_r carry the load current. There is no resonance in this mode and the circuit operation is identical to that of a conventional PWM buck converter. The voltage and current equations for this mode are

$$i_S = i_{Lr} = I_o. \tag{8}$$

Mode 5 t_4-t_5. This mode starts with the initial conditions $i_S = I_o$, $i_{Lr} = I_o$, $v_{Cr} = V_{Cr\max} = V_i$, $V_{Cb} = V_{Cbm}$. The main

switch is turned off under ZVS, and at the same instant, the synchronous switch is turned on under ZCS. Since the synchronous switch S_1 is conducting the voltage across capacitor, C_b is clamped to zero. Resonance occurs with L_r and C_r. The voltage and current equations for this mode are

$$\begin{aligned} v_{Cb}(t-t_4) &= 0, \\ i_{Lr}(t-t_4) &= I_o\cos\omega_3(t-t_4) - \frac{V_i}{Z_3}\sin\omega_3(t-t_4), \end{aligned} \tag{9}$$

$$v_{Cr}(t-t_4) = I_oZ_3\sin\omega_3(t-t_4) + V_i\cos\omega_3(t-t_4). \tag{10}$$

The time duration of this mode can be found as follows:

$$t_{45} = \frac{1}{\omega_3}\tan^{-1}\frac{V_i}{I_oZ_3}, \tag{11}$$

where

$$\begin{aligned} \omega_3 &= \frac{1}{\sqrt{L_rC_r}}, \\ Z_3 &= \sqrt{\frac{L_r}{C_r}}. \end{aligned} \tag{12}$$

This mode ends when voltage across C_r becomes zero. Therefore, the diode D_{S2} turns on under ZVS.

Mode 6 t_5-t_6. In this stage, new resonance takes place through L_r-C_b-D_{S2}-D_{S1}. At $t = t_5$, $i_S = 0$, $i_{Lr} = I_{Lr2}$, $v_{Cr} = 0$, and $v_{Cb} = 0$ are initial conditions for this mode. For this state, the equations are

$$\begin{aligned} v_{Cb}(t-t_5) &= I_{Lr2}Z_2\sin\omega_2(t-t_5), \\ i_{Lr}(t-t_5) &= I_{Lr2}\cos\omega_2(t-t_5). \end{aligned} \tag{13}$$

When i_{Lr} becomes I_o, this mode comes to an end. The time interval for this mode is given as

$$t_{56} = \frac{1}{\omega_2}\tan^{-1}\left(\frac{I_o}{I_{Lr2}}\right), \tag{14}$$

where

$$\begin{aligned} \omega_2 &= \frac{1}{\sqrt{L_rC_b}}, \\ Z_2 &= \sqrt{\frac{L_r}{C_b}}. \end{aligned} \tag{15}$$

Mode 7 t_6-t_7. At $t = t_6$, $i_S = 0$, $i_{Lr} = I_o$, $v_{Cr} = 0$, and $v_{Cb} = V_{Cb2}$ are initial conditions for this mode. As i_{Lr} becomes I_o, synchronous switch is turned off under ZCS. Stored energy of inductor L_r and capacitor C_b is now transferred to load. ON state resistances of diodes and switches are neglected. The voltage and current equations for this mode are given as

$$\begin{aligned} v_{Cb}(t-t_6) &= -\frac{I_o}{C_b}(t-t_6) + V_{Cb2}, \\ i_{Lr}(t-t_6) &= -\frac{V_o}{L_r}(t-t_6) + I_o. \end{aligned} \tag{16}$$

This mode ends when i_{Lr} becomes zero. The interval of this mode is given by

$$t_{67} = \frac{I_oL_r}{V_o}. \tag{17}$$

Mode 8 t_7-t_8. Now the load current will flow through body diode of synchronous switch S_1. During this mode, the converter operates like a conventional PWM buck converter until the switch S is turned on in the next switching cycle. In this mode,

$$i_{D1} = I_o. \tag{18}$$

2.3. Output voltage

The output voltage can be specified by evaluating the energy from the supply, through the input resonant inductor L_r [27]. The output voltage is given by

$$\begin{aligned} V_o &= \frac{V_i}{\tau}\left(\frac{1}{2}t_{01} + t_{12} + t_{23} + t_{45} + t_{56} + t_{67}\right) \\ &= \frac{V_i}{\tau}\left(\begin{aligned} &\frac{1}{2}\frac{I_oL_r}{V_i} + \frac{1}{\omega_1}\sin^{-1}\left(\frac{C_r}{C_e} - 1\right) + \frac{1}{\omega_2}\tan^{-1}\left(\frac{I_{Lr\max} - I_o}{V_{Cb1}}\right) \\ &+ \frac{1}{\omega_3}\tan^{-1}\left(\frac{V_{Cr\max}}{I_oZ_3}\right) + \frac{1}{\omega_2}\tan^{-1}\left(\frac{I_o}{I_{Lr2}}\right) + \frac{1}{2}\frac{I_oL_r}{V_o} \end{aligned}\right). \end{aligned} \tag{19}$$

Since time intervals of Modes 1 and 7 have low value as compared to other terms in the above expression, the first and last terms are neglected for simplification.

Then, the voltage conversion ratio will be

$$\frac{V_o}{V_i} = \frac{1}{\tau}\left(\begin{aligned} &\frac{1}{\omega_1}\sin^{-1}\left(\frac{C_r}{C_e} - 1\right) + \frac{1}{\omega_2}\tan^{-1}\left(\frac{I_{Lr\max} - I_o}{V_{Cb1}}\right) \\ &+ \frac{1}{\omega_3}\tan^{-1}\left(\frac{V_{Cr\max}}{I_oZ_3}\right) + \frac{1}{\omega_2}\tan^{-1}\left(\frac{I_o}{I_{Lr2}}\right) \end{aligned}\right), \tag{20}$$

where $\tau = 1/f_S$, and f_S is the switching frequency.

From the expression, it can be seen that the voltage conversion ratio depends upon switching frequency rather than duty ratio.

3. DESIGN PROCEDURE

Design of conventional PWM converters has been well presented in literatures. Thus, it is more significant to focus on design procedures of the auxiliary circuit. The resonant inductor and resonant capacitor are the most important components when designing the auxiliary circuit. The proposed auxiliary resonant circuit provides soft-switching conditions for the main transistor. The following design procedure is developed considering procedures such as those presented previously in [5–7].

(1) Snubber inductor L_r is selected to permit its current to rise up to at most the maximum output current within t_r time periods, during the turn-on of the main transistor or the turnoff of the synchronous switch. In this case, from (1),

$$\frac{V_i}{L_r} t_r \le I_{o\max} \tag{21}$$

can be written. Here, t_r is the rise time of the main transistor. These equations provide ZCS turn-on for the main transistor and ZVS turnoff for the body diode of synchronous switch.

(2) Snubber capacitor C_r is selected to be discharged from V_i to zero with the maximum output current over at least the time period t_f during the turnoff of the main transistor. For this state, according to (10) and (11),

$$\frac{1}{I_{o\max} Z_3} V_i \ge t_f. \tag{22}$$

Here, t_f is the fall time of the main transistor and

$$Z_3 = \sqrt{\frac{L_r}{C_r}}. \tag{23}$$

(3) Buffer capacitor C_b is selected to be charged from zero up to at most a value decided before, such as half the input voltage. This capacitor takes on the energies that are stored in the snubber inductor during the turnoff of the synchronous switch and charge of the snubber capacitor. This energy balance can be defined as follows:

$$\frac{1}{2} C_r V_i^2 + \frac{1}{2} C_b V_{Cbm}^2 = \frac{1}{2} L_r I_{o\max}^2. \tag{24}$$

The value of C_b is normally larger than the value of C_r. Consequently, the bigger the value of selected C_b is, the lower the value of $V_{Cb\max}$ will be. Moreover, if the value of C_b increases, the voltage across the synchronous switch falls, but the time periods t_{23}, t_{45}, t_{56}, and t_{67} during which the inductor energies are transferred to C_b or the load rise.

4. CONVERTER FEATURES

The features of the proposed soft-switching converter are briefly summarized as follows.

(1) All of the active and passive semiconductor devices are turned on and off under exact ZVS and/or ZCS.
(2) The proposed converter has a simple structure, low cost, and ease of control.
(3) The converter acts as a conventional PWM converter during most of the switching cycles.
(4) The presented snubber cell can be easily applied to the other basic PWM DC-DC converters and to all switching converters.
(5) The proposed converter has a larger total efficiency and a wider load range.

Table 1: Components used in the proposed converter.

Component	Value/model	
	Simulation	Experiment
Main switch (S)	Ideal	IRF1312
Synchronous switch (S_1)	Ideal	IRF1010E
Schottky diode (D_{S1})	Ideal	MBR60L45CTG
Schottky diode (D_{S2})	Ideal	MBR60L45CTG
Schottky diode (D_{S3})	Ideal	MBR60L45CTG
Resonant inductor (L_r)	15 nH	15 nH
Resonant capacitor (C_r)	1 nF	1 nF
Buffer capacitor (C_b)	3.3 nF	3.3 nF
Output capacitor (C_o)	15 μF	15 μF
Output inductor (L_o)	5 μH	5 μH

(6) The main switch and the auxiliary switch are not subjected to additional voltage stresses. Current stress on the main switch is slightly higher, but current stress on the auxiliary switch is within safe limit.

5. SIMULATION AND EXPERIMENTAL RESULTS

A prototype of the proposed converter, as shown in Figure 1, has been built in the laboratory. The newly proposed converter operates with an input voltage $V_i = 12$ V, output voltage $V_o = 3.3$ V, load current of 11 A, and a switching frequency of 500 kHz. The converter is simulated using simulation software PSIM, version 6.0. The major parameters and components are given in Table 1.

Figures 4(a)–4(d) show the simulation results of the proposed converter and Figures 5(a)–5(d) present the experimental results. All the waveforms except the efficiency curve represent a time period of one switching cycle, which is 2 microseconds in this case. The amplitudes are denoted in Figure 4 with each of their waveforms, respectively.

5.1. *Main switch* S

It is noted from Figures 4(a) and 5(a) that the main switch S is turned on under ZCS, and the body diode D_1 of synchronous switch S_1 is turned off under ZVS. The main switch takes the load current and the charging current of the capacitors C_r and C_b. The inductor starts to transfer its stored energy to capacitors C_r and C_b during the turn-on period of main switch. The converter has not exceeded the voltage limits; however, the current stress is slightly higher for a very short period of time. The main switch also switches off under ZVS. The current and voltage wave shapes are identical to theoretical waveforms.

5.2. *Synchronous switch* S_1

After the main switch is turned on under ZCS, the body diode of synchronous switch is turned off under ZVS, which can be observed from Figures 4(b) and 5(b). The synchronous switch is turned on under ZCS when the main

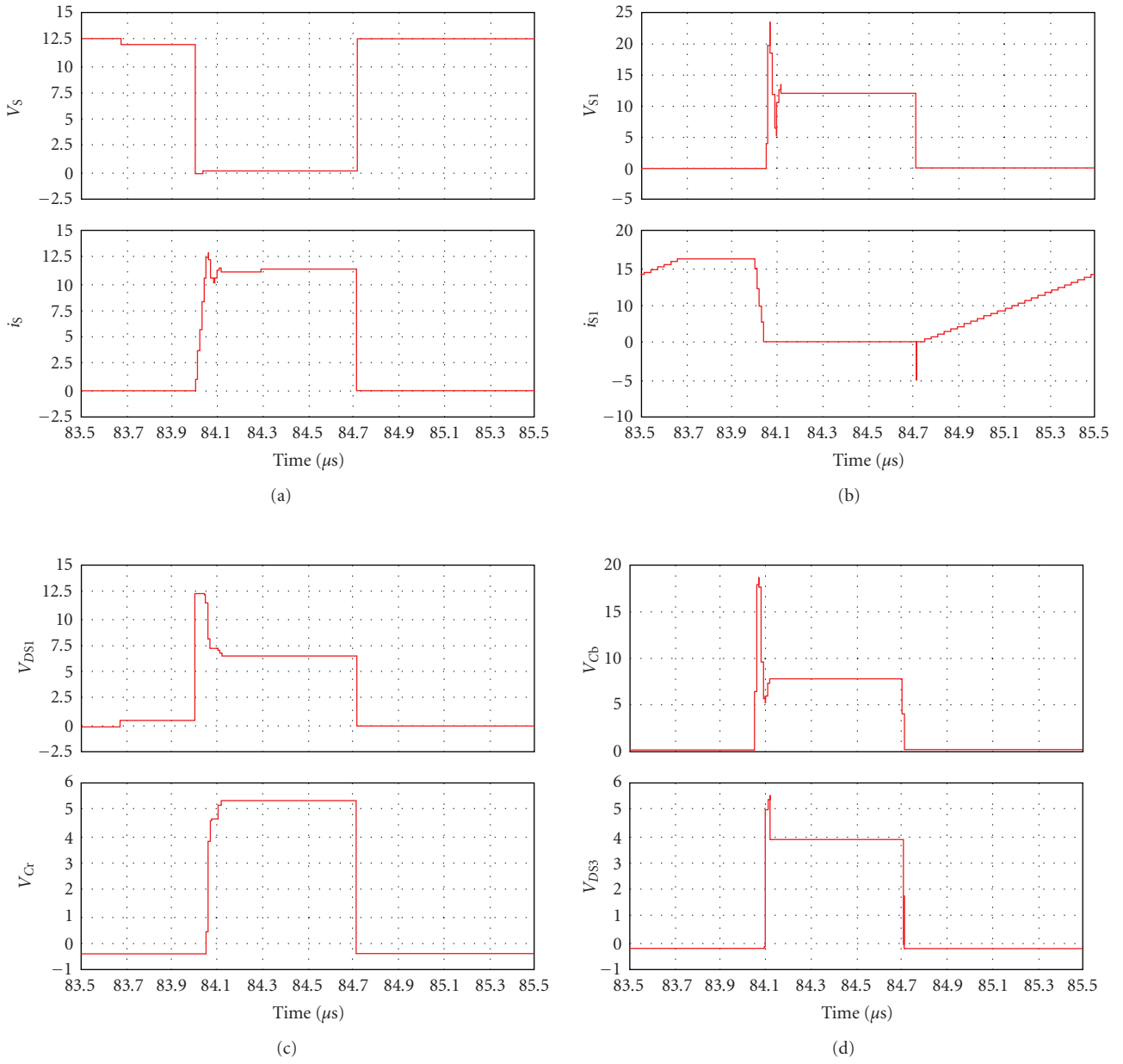

FIGURE 4: Simulated voltage and current waveforms: (a) main switch S: V_S, I_S; (b) synchronous switch S_1: V_{S1}, I_{S1}; (c) diode D_{S1} and capacitor C_r; (d) capacitor C_b and diode D_{S3}.

switch is turned off under ZVS. After the turnoff of the main switch, both capacitors C_r and C_b are discharged. As soon as both capacitors are discharged near zero, the body diode of synchronous switch S_1 is turned on under ZVS. The converter has not exceeded the current limits; however, the voltage stress across the switch is slightly higher for a very short period of time. The synchronous switch operates within the safe limits, and it can be noted here that the conduction period of S_1 is more confining to the design values and it operates at a low power when compared to the other switches. The shapes of the figures are identified to confine much to the theoretical waveforms.

5.3. *Schottky diodes* D_{S1}, D_{S2}, *and* D_{S3}

The Schottky diodes work for a very short period to discharge the resonant capacitors C_r and C_b as can be observed from Figures 4(c), 4(d), 5(c), and 5(d). Moreover, it can be seen that the Schottky diodes D_{S1}, D_{S2}, and D_{S3} operate under soft-switching conditions. The Schottky diodes are turned on and off under ZVS. The conduction of Schottky diodes may cause a considerable drop in output voltage for low-power circuits, but due to the advancement in semiconductor techniques, Schottky diodes are also now available with a low-forward-voltage drop for high-frequency circuits.

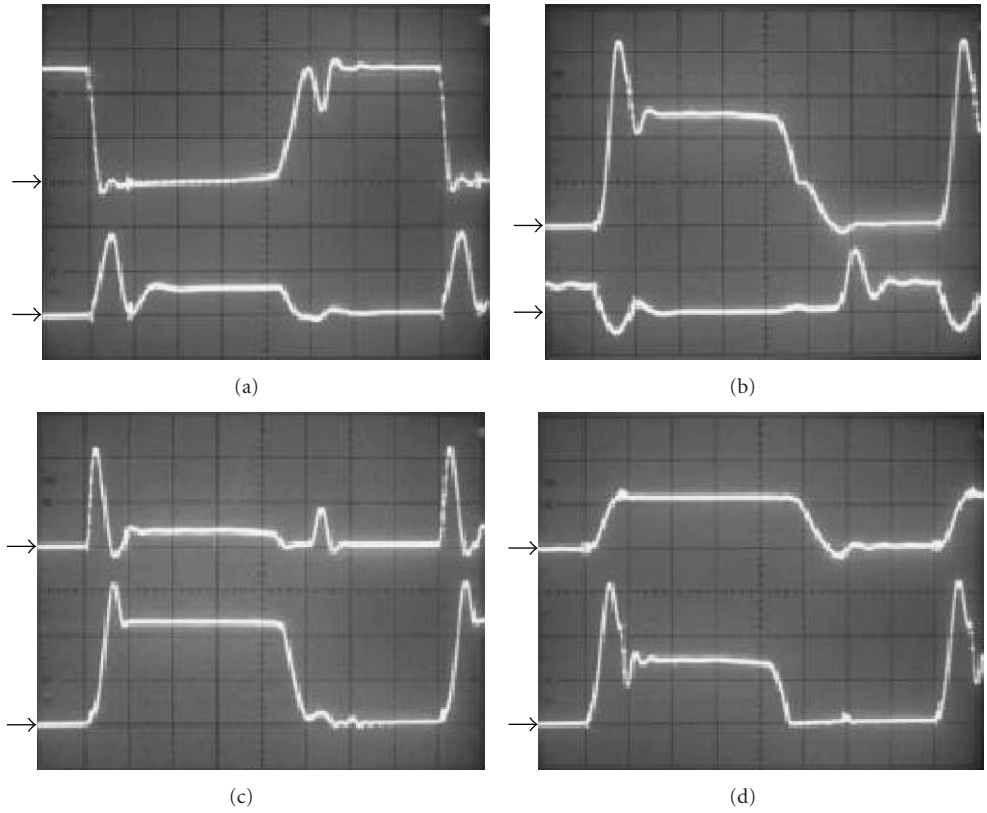

Figure 5: Experimental voltage and current waveforms: (a) main switch S: V_S, I_S (V: 5 V/div, I: 10 A/div, time: 0.2 μs/div); (b) synchronous switch S_1: V_{S1}, I_{S1} (V: 5 V/div, I: 10 A/div, time: 0. 2 μs/div); (c) diode D_{S1} and capacitor C_r: V_{DS1}, V_{Cr} (V: 5 V/div, I: 2 V/div, time: 0. 2 μs/div); (d) capacitor C_b and diode D_{S3}: V_{Cb}, V_{DS3} (V: 5 V/div, I: 2 V/div, time: 0.2 μs/div).

Additionally, during the turn-on and turnoff of main switch S and synchronous switch S_1, a slight overlap occurs between their own voltages and currents. Therefore, the switching losses are zero, but a little additional conduction loss takes place, and so the conduction losses dominate the total loss in the soft-switching converter.

Efficiency curve

From Figure 6, it can be observed that the efficiency values of the soft-switching converter are relatively high with respect to those of the hard-switching converter. The efficiency values towards the minimum output power decrease naturally because the converter is designed for the maximum output current. At 70% output power, the overall efficiency of the proposed converter increases to about 96% from the value of 87% in its counterpart hard-switching converter. The high efficiency concludes the correctness of the design values.

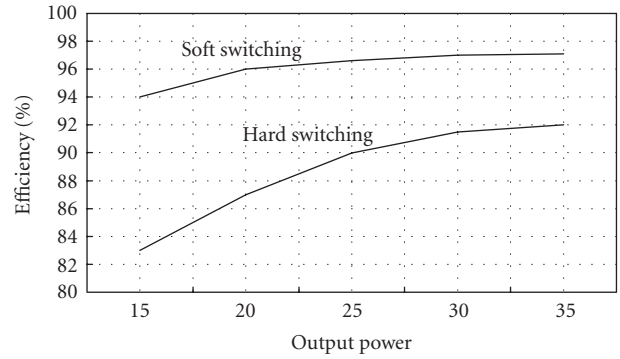

Figure 6: Efficiency curve.

6. CONCLUSION

The concepts of ZVT used in medium and high power were implemented in synchronous buck converter, and it was shown that the switching losses in synchronous buck were eliminated. Besides, the main switch ZCS is turned on and ZVS is turned off. The synchronous switch is also turned on under ZCS and turned off under ZVS. Hence, switching losses are reduced and the newly proposed ZVT synchronous buck is highly efficient than the conventional converter. The additional voltage and current stresses on the main devices do not take place, and the auxiliary devices are subjected to allowable voltage and current values. Moreover, the converter has a simple structure, low cost, and ease of control. A prototype of a 3.3 V, 11 A, 500 kHz system was implemented to experimentally verify the improved performance.

REFERENCES

[1] A. J. Stratakos, S. R. Sanders, and R. W. Brodersen, "Low-voltage CMOS DC-DC converter for a portable battery-operated system," in *Proceedings of the 25th Annual IEEE Power Electronics Specialists Conference (PESC '94)*, vol. 1, pp. 619–626, Taipei, Taiwan, June 1994.

[2] O. Djekic and M. Brkovic, "Synchronous rectifiers vs. Schottky diodes in a buck topology for low voltage applications," in *Proceedings of the 28th Annual IEEE Power Electronics Specialists Conference (PESC '97)*, vol. 2, pp. 1374–1380, St. Louis, Mo, USA, June 1997.

[3] O. Djekic, M. Brkovic, and A. Roy, "High frequency synchronous buck converter for low voltage applications," in *Proceedings of IEEE 29th Annual Power Electronics Specialists Conference (PESC '98)*, vol. 2, pp. 1248–1254, Fukuoka, Japan, May 1998.

[4] M. D. Mulligan, B. Broach, and T. H. Lee, "A constant-frequency method for improving light-load efficiency in synchronous buck converters," *IEEE Power Electronics Letters*, vol. 3, no. 1, pp. 24–29, 2005.

[5] L. Yang and C. Q. Lee, "Analysis and design of boost zero-voltage-transition PWM converter," in *Proceedings of the 8th Annual Applied Power Electronic Conference and Exposition (APEC '93)*, pp. 707–713, San Diego, Calif, USA, March 1993.

[6] G. Hua, C.-S. Leu, Y. Jiang, and F. C. Y. Lee, "Novel zero-voltage-transition PWM converters," *IEEE Transactions on Power Electronics*, vol. 9, no. 2, pp. 213–219, 1994.

[7] A. V. da Costa, C. H. G. Treviso, and L. C. de Freitas, "A new ZCS-ZVS-PWM boost converter with unity power factor operation," in *Proceedings of the 9th Annual Applied Power Electronics Conference and Exposition (APEC '94)*, pp. 404–410, Orlando, Fla, USA, February 1994.

[8] N. P. Filho, V. J. Farias, and L. C. de Freitas, "A novel family of DC-DC PWM converters uses the self resonance principle," in *Proceedings of the 25th Annual IEEE Power Electronics Specialists Conference (PESC '94)*, vol. 2, pp. 1385–1391, Taipei, Taiwan, June 1994.

[9] G. Moschopoulos, P. Jain, and G. Joos, "A novel zero-voltage switched PWM boost converter," in *Proceedings of the 26th Annual IEEE Power Electronics Specialists Conference (PESC '95)*, vol. 2, pp. 694–700, Atlanta, Ga, USA, June 1995.

[10] A. Elasser and D. A. Torrey, "Soft switching active snubbers for DC/DC converters," *IEEE Transactions on Power Electronics*, vol. 11, no. 5, pp. 710–722, 1996.

[11] K. M. Smith Jr. and K. M. Smedley, "A comparison of voltage-mode soft-switching methods for PWM converters," *IEEE Transactions on Power Electronics*, vol. 12, no. 2, pp. 376–386, 1997.

[12] Y. Xi, P. K. Jain, G. Joos, and H. Jin, "A zero voltage switching forward converter topology," in *Proceedings of the 19th International Telecommunications Energy Conference (INTELEC '97)*, pp. 116–123, Melbourne, Australia, October 1997.

[13] C.-J. Tseng and C.-L. Chen, "Nova ZVT-PWM converters with active snubbers," *IEEE Transactions on Power Electronics*, vol. 13, no. 5, pp. 861–869, 1998.

[14] G. Moschopoulos, P. K. Jain, Y.-F. Liu, and G. Joós, "A zero-voltage-switched PWM boost converter with an energy feedforward auxiliary circuit," *IEEE Transactions on Power Electronics*, vol. 14, no. 4, pp. 653–662, 1999.

[15] T.-W. Kim, H.-S. Kim, and H.-W. Ahn, "An improved ZVT PWM boost converter," in *Proceedings of the 31st IEEE Annual Power Electronics Specialists Conference (PESC '00)*, vol. 2, pp. 615–619, Galway, UK, June 2000.

[16] J.-H. Kim, D. Y. Lee, H. S. Choi, and B. H. Cho, "High performance boost PFP (Power Factor Pre-regulator) with an improved ZVT (Zero Voltage Transition) converter," in *Proceedings of the 16th Annual IEEE Applied Power Electronics Conference and Exposition (APEC '01)*, vol. 1, pp. 337–342, Anaheim, Calif, USA, March 2001.

[17] N. Jain, P. Jain, and G. Joós, "Analysis of a zero voltage transition boost converter using a soft switching auxiliary circuit with reduced conduction losses," in *Proceedings of the 32nd IEEE Annual Power Electronics Specialists Conference (PESC '01)*, vol. 4, pp. 1799–1804, Vancouver, Canada, 2001.

[18] M. L. Martins, H. A. Gründling, H. Pinheiro, J. R. Pinheiro, and H. L. Hey, "A ZVT PWM boost converter using an auxiliary resonant source," in *Proceedings of the 17th Annual IEEE Applied Power Electronics Conference and Expositions (APEC '02)*, vol. 2, pp. 1101–1107, Dallas, Tex, USA, March 2002.

[19] C.-M. Wang, "Zero-voltage-transition PWM DC-DC converters using a new zero-voltage-switching PWM switch cell," in *Proceedings of the 25th International Telecommunications Energy Conference (INTELEC '03)*, pp. 784–789, Yokohama, Japan, October 2003.

[20] M. L. Martins, J. L. Russi, H. Pinheiro, J. R. Pinheiro, H. A. Gründling, and H. L. Hey, "Unified design for ZVT PWM converters with resonant auxiliary circuit," *IEE Proceedings: Electric Power Applications*, vol. 151, no. 3, pp. 303–311, 2004.

[21] S. Kaewarsa, C. Prapanavarat, and U. Yangyuen, "An improved zero-voltage-transition technique in a single-phase power factor correction circuit," in *Proceedings of International Conference on Power System Technology (POWERCON '04)*, vol. 1, pp. 678–683, Singapore, November 2004.

[22] M. L. Martins, J. L. Russi, and H. L. Hey, "Zero-voltage transition PWM converters: a classification methodology," *IEE Proceedings: Electric Power Applications*, vol. 152, no. 2, pp. 323–334, 2005.

[23] W. Huang and G. Moschopoulos, "A new family of zero-voltage-transition PWM converters with dual active auxiliary circuits," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 370–379, 2006.

[24] V. Yousefzadeh and D. Maksimović, "Sensorless optimization of dead times in dc-dc converters with synchronous rectifiers," *IEEE Transactions on Power Electronics*, vol. 21, no. 4, pp. 994–1002, 2006.

[25] G. Hua, E. X. Yang, Y. Jiang, and F. C. Lee, "Novel zero-current-transition PWM converters," *IEEE Transactions on Power Electronics*, vol. 9, no. 6, pp. 601–606, 1994.

[26] K. M. Smith Jr. and K. M. Smedley, "Properties and synthesis of passive lossless soft-switching PWM converters," *IEEE Transactions on Power Electronics*, vol. 14, no. 5, pp. 890–899, 1999.

[27] B. W. Williams, "Principles and Elements of Power Electronics, Devices, Drivers, Applications, and Passive Components," 2006.