Research Article

A Novel Soft-Switching Synchronous Buck Converter for Portable Applications

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Received 8 June 2007; Revised 26 October 2007; Accepted 10 December 2007

Recommended by Burak Ozpineci

This paper proposes a zero-voltage-transition (ZVT) pulse-width-modulated (PWM) synchronous buck converter, which is designed to operate at low voltage and high efficiency typically required for portable systems. A new passive auxiliary circuit that allows the main switch to operate with zero-voltage switching has been incorporated in the conventional PWM synchronous buck converter. The operation principles and a detailed steady-state analysis of the ZVT-PWM synchronous converter implemented with the auxiliary circuit are presented. Besides, the main switch and all of the semiconductor devices operate under soft-switching conditions. Thus, the auxiliary circuit provides a larger overall efficiency. The feasibility of the auxiliary circuit is confirmed by simulation and experimental results.

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1. INTRODUCTION

Current trends in consumer electronics demand progressively lower-voltage supplies. Portable electronics equipment, such as laptop computers, cellular phones, and future microprocessor and memory chips, requires low-power circuitry to maximize battery run time. Because of significantly lower conduction losses, synchronous rectifiers are now used in essentially all low-voltage DC power supplies [1–4]. A synchronous rectifier is an electronic switch that improves power-conversion efficiency by placing a low-resistance conduction path across the diode rectifier in a switch-mode regulator. MOSFETs usually serve this purpose.

However, higher input voltages and lower output voltages have brought about very low duty cycles, increasing switching losses and decreasing conversion efficiency. So in this paper, we have optimized the efficiency of the synchronous buck converter by eliminating switching losses using soft-switching technique. The voltage-mode soft-switching method that has attracted most interest in recent years is the zero-voltage transition [5–24]. This is because of its low additional conduction losses and because its operation is closest to the PWM converters. The auxiliary circuit of the ZVT converters is activated just before the main switch is turned on and ceases after it is accomplished. The auxiliary circuit components in this circuit have lower ratings than those in the main power circuit because the auxiliary circuit is active for only a fraction of the switching cycle; this allows a device that can turn on with fewer switching losses than the main switch to be used as the auxiliary switch. The improvement in efficiency caused by the auxiliary circuit is mainly due to the difference in switching losses between the auxiliary switch and the main power switch if it were to operate without the help of the auxiliary circuit. Previously proposed ZVT-PWM converters have at least one of the following key drawbacks. (i) The auxiliary switch is turned off while it is conducting current. This causes the switching losses and EMI to appear, which offsets the benefits of using the auxiliary circuit. In converters such as the ones proposed in [6, 12, 15, 16], the turnoff is very hard. (ii) The auxiliary circuit causes the main converter switch to operate with a higher peak current stress and with more circulating current. This results in the need for a higher current-rated device for the main switch and an increase in conduction losses. The converters proposed in [5, 8, 9, 13, 14, 17] are having high current stresses on the main switch. (iii) The auxiliary circuit
To analyze the steady-state operations of the proposed circuit, the following assumptions are made during one switching cycle.

1. Input voltage $V_i$ is constant.
2. Output voltage $V_o$ is constant or output capacitor $C_o$ is large enough.
3. Output current $I_o$ is constant or output inductor $L_o$ is large enough.
4. Output inductor $L_o$ is much larger than resonant circuit inductor $L_r$.
5. Resonant circuits are ideal.
6. Semiconductor devices are ideal.
7. Reverse recovery time of all diodes is ignored.

2.2. Operation principles and analysis

Based on these assumptions, circuit operations in one switching cycle can be divided into eight stages. The key waveforms of these stages are given in Figure 2 and the equivalent circuit schemes of the operation stages are given in Figure 3. The detailed analysis of every stage is presented as follows.

**Mode 1 $t_0$-$t_1$.** Prior to $t_1$, the body diode of switch $S_1$ was conducting, while the main switch $S$ was off. The equations $i_S = 0$, $i_{D1} = I_o$, $i_{Lr} = 0$, $v_{C1} = 0$, $v_{C2} = 0$ and $v_{CB} = 0$ are valid at the beginning of this stage. At $t = t_0$, the main switch is turned on, which realizes zero-current turn-on as it is in series with the resonant inductor $L_r$. During this stage, $i_{Lr}$ rises and current $i_{D1}$ through body diode of switch $S_1$ falls simultaneously at the same rate linearly. The mode ends at $t = t_1$ when $i_{Lr}$ reaches $I_o$ and $i_{D1}$ becomes zero. The body diode $D_1$ is turned off with ZVS because of $C_r$ and $C_b$ being existent. In this state,

\[
i_S = i_{Lr} = \frac{V_i}{L_r} (t-t_0),
\]

\[
i_{D1} = I_o - i_{Lr} = \frac{V_i}{L_r} (t-t_0) + I_o,
\]

\[
t_0 = \frac{L_r}{V_i} I_o.
\]

**Mode 2 $t_1$-$t_2$.** The diode $D_{S2}$ starts conducting at the instant when body diode $D_1$ is turned off. At $t = t_1$, $i_S = i_{Lr} = I_o$, $i_{D1} = 0$, $v_{C1} = 0$, and $v_{CB} = 0$. In this interval, resonance occurs with the inductor $L_r$ and capacitors $C_r$ and $C_b$. This mode ends with $C_r$ charged up to the input voltage $V_i$;

\[
i_{Lr} (t-t_1) = \frac{V_i}{Z_1} \sin \omega_1 (t-t_1) + I_o,
\]

\[
v_{C1} (t-t_1) = \frac{C_r}{C_r} \left[ - V_i \cos \omega_1 (t-t_1) + V_i \right],
\]

\[
v_{CB} (t-t_1) = \frac{C_b}{C_b} \left[ - V_i \cos \omega_1 (t-t_1) + V_i \right],
\]
Figure 2: Key theoretical waveforms of the proposed converter.

where

\[ Ce = \frac{C_r C_b}{C_r + C_b}, \]
\[ \omega_1 = \frac{1}{\sqrt{L_r C_e}}, \]
\[ Z_1 = \frac{I_r}{\sqrt{C_e}}. \] (3)

The diode \( D_{S1} \) is turned on with ZVS at the moment when \( v_{Cr} \) becomes \( V_i \). In this state,
\[ t_{12} = \frac{1}{\omega_1} \sin^{-1} \left( \frac{C_r}{C_e} - 1 \right). \] (4)  

Mode 3 \( t_2-t_3 \). At \( t = t_2 \), \( i_S = I_o \), \( i_{Lr} = i_{Lr\text{max}} \), \( v_{Cr} = V_{Cr\text{max}} = V_i \), and \( v_{Cb} = V_{Ch1} \). When diode \( D_{S1} \) turns on, new resonance starts with \( L_r \) and \( C_b \). This mode ends when \( i_{Lr} \) becomes equal to load current \( I_o \), and \( C_b \) is charged up to its maximum voltage \( V_{Chm} \). Both diodes \( D_{S1} \) and \( D_{S2} \) are turned off under ZCS due to the existence of \( L_r \). The voltage and current expressions that govern this circuit mode are given by

\[ i_{Lr}(t - t_2) = (I_{Lr\text{max}} - I_o) \cos \omega_2 (t - t_2) - \frac{V_{Ch1}}{Z_2} \sin \omega_2 (t - t_2) + I_o, \]  
\[ v_{Cb}(t - t_2) = (I_{Lr\text{max}} - I_o) Z_2 \sin \omega_2 (t - t_2) + V_{Ch1} \cos \omega_2 (t - t_2). \] (5)
The time interval of this stage can be found as follows:

\[ t_{23} = \frac{1}{\omega_2} \tan^{-1} \left( \frac{L_r \text{max}}{I_o V_{C_{b1}}} \right), \]

where

\[ \omega_2 = \frac{1}{\sqrt{L_r C_b}}, \]

\[ Z_2 = \frac{T_r}{C_b}. \]

Mode 4 \( t_3-t_4 \). Since both diodes \( D_{S1} \) and \( D_{S2} \) have been turned off at \( t_3 \), now only the main switch \( S \) and inductor \( L_r \) carry the load current. There is no resonance in this mode and the circuit operation is identical to that of a conventional PWM buck converter. The voltage and current equations for this mode are

\[ i_S = i_{L_r} = I_o. \]

Mode 5 \( t_4-t_5 \). This mode starts with the initial conditions

\[ i_S = I_o, i_{L_r} = I_o, v_{C_T} = V_{C_{T_{\text{max}}}} = V_i, V_{C_b} = V_{C_{b_{\text{max}}}}. \]

The main
switch is turned off under ZVS, and at the same instant, the synchronous switch is turned on under ZCS. Since the synchronous switch \( S_1 \) is conducting the voltage across capacitor, \( C_b \) is clamped to zero. Resonance occurs with \( L_r \) and \( C_r \). The voltage and current equations for this mode are

\[
v_{CB}(t - t_4) = 0, \quad i_{Lr}(t - t_4) = I_o \cos \omega_3(t - t_4) - \frac{V_i}{Z_3} \sin \omega_3(t - t_4), \\
v_{Cr}(t - t_4) = I_o Z_3 \sin \omega_3(t - t_4) + V_i \cos \omega_3(t - t_4).
\]

(9)

(10)

The time duration of this mode can be found as follows:

\[
t_{45} = \frac{1}{\omega_3} \tan^{-1} \frac{V_i}{I_o Z_3},
\]

(11)

where

\[
\omega_3 = \frac{1}{\sqrt{L_r C_r}}, \quad Z_3 = \frac{I_r}{\sqrt{L_r C_r}}.
\]

(12)

This mode ends when voltage across \( C_b \) becomes zero. Therefore, the diode \( D_{S2} \) turns on under ZVS.

Mode 6 \( t_5-t_6 \). In this stage, new resonance takes place through \( L_r-C_b-D_{S2}-D_{S1} \). At \( t = t_5 \), \( i_{L_1} = I_{L12} \), \( v_{Cr} = 0 \), and \( v_{CB} = 0 \) are initial conditions for this mode. For this state, the equations are

\[
v_{CB}(t - t_5) = I_{L12} Z_3 \sin \omega_2(t - t_5), \quad i_{Lr}(t - t_5) = I_{L12} \cos \omega_2(t - t_5).
\]

(13)

When \( i_{Lr} \) becomes \( I_o \), this mode comes to an end. The time interval for this mode is given as

\[
t_{56} = \frac{1}{\omega_2} \tan^{-1} \left( \frac{I_o}{I_{L12}} \right),
\]

(14)

where

\[
\omega_2 = \frac{1}{\sqrt{L_r C_b}}, \quad Z_2 = \frac{I_r}{\sqrt{L_r C_b}}.
\]

(15)

Mode 7 \( t_6-t_7 \). At \( t = t_6 \), \( i_{L_1} = 0 \), \( i_{Lr} = I_o \), \( v_{Cr} = 0 \), and \( v_{CB} = V_{C2} \) are initial conditions for this mode. As \( i_{Lr} \) becomes \( I_o \), synchronous switch is turned off under ZCS. Stored energy of inductor \( L_r \) and capacitor \( C_b \) is now transferred to load. ON state resistances of diodes and switches are neglected. The voltage and current equations for this mode are given as

\[
v_{CB}(t - t_6) = -\frac{I_o}{C_b}(t - t_6) + V_{C2}, \quad i_{Lr}(t - t_6) = -\frac{V_o}{L_r}(t - t_6) + I_o.
\]

(16)

This mode ends when \( i_{Lr} \) becomes zero. The interval of this mode is given by

\[
t_{67} = \frac{I_o L_r}{V_o}.
\]

(17)

Mode 8 \( t_7-t_8 \). Now the load current will flow through body diode of synchronous switch \( S_1 \). During this mode, the converter operates like a conventional PWM buck converter until the switch \( S \) is turned on in the next switching cycle. In this mode,

\[
i_{D1} = I_o.
\]

(18)

2.3. Output voltage

The output voltage can be specified by evaluating the energy from the supply, through the input resonant inductor \( L_r \) [27]. The output voltage is given by

\[
V_o = \frac{V_i}{\tau} \left[ \left( \frac{1}{\omega_1} \sin^{-1} \left( \frac{C_i}{C_e} - 1 \right) \right) + \frac{1}{\omega_2} \tan^{-1} \left( \frac{I_{L12} - I_o}{V_{CH1}} \right) \right],
\]

(19)

\[
+ \left( \frac{1}{\omega_3} \tan^{-1} \left( \frac{V_{C2} \max}{I_o Z_2} \right) + \frac{1}{\omega_4} \tan^{-1} \left( \frac{I_o}{I_{L12}} \right) + \frac{1}{\omega_5} \tan^{-1} \left( \frac{I_o}{V_o} \right) \right).
\]

Since time intervals of Modes 1 and 7 have low value as compared to other terms in the above expression, the first and last terms are neglected for simplification.

Then, the voltage conversion ratio will be

\[
\frac{V_o}{V_i} = \frac{1}{\tau} \left[ \left( \frac{1}{\omega_1} \sin^{-1} \left( \frac{C_i}{C_e} - 1 \right) \right) + \frac{1}{\omega_2} \tan^{-1} \left( \frac{I_{L12} - I_o}{V_{CH1}} \right) \right],
\]

(20)

where \( \tau = 1/f_s \), and \( f_s \) is the switching frequency.

From the expression, it can be seen that the voltage conversion ratio depends upon switching frequency rather than duty ratio.

3. DESIGN PROCEDURE

Design of conventional PWM converters has been well presented in literatures. Thus, it is more significant to focus on design procedures of the auxiliary circuit. The resonant inductor and resonant capacitor are the most important components when designing the auxiliary circuit. The proposed auxiliary resonant circuit provides soft-switching conditions for the main transistor. The following design procedure is developed considering procedures such as those presented previously in [5–7].
(1) Snubber inductor $L_s$ is selected to permit its current to rise up to at most the maximum output current within $t_r$ time periods, during the turn-on of the main transistor or the turnoff of the synchronous switch. In this case, from (1),

$$\frac{V_i}{I_{o \text{max}}} t_r \leq I_{o \text{max}}$$

(21)

which can be written. Here, $t_r$ is the rise time of the main transistor. These equations provide ZCS turn-on for the main transistor and ZVS turnoff for the body diode of synchronous switch.

(2) Snubber capacitor $C_s$ is selected to be discharged from $V_i$ to zero with the maximum output current over at least the time period $t_f$ during the turnoff of the main transistor. For this state, according to (10) and (11),

$$\frac{1}{I_{o \text{max}}} \frac{V_i}{Z_3} \geq t_f.$$  

Here, $t_f$ is the fall time of the main transistor and

$$Z_3 = \sqrt{\frac{L_s}{C_s}}.$$  

(23)

(3) Buffer capacitor $C_b$ is selected to be charged from zero up to at most a value decided before, such as half the input voltage. This capacitor takes on the energies that are stored in the snubber inductor during the turnoff of the synchronous switch and charge of the snubber capacitor. This energy balance can be defined as follows:

$$\frac{1}{2} C_s V_i^2 + \frac{1}{2} C_b V_{\text{chm}}^2 = \frac{1}{2} L_s I_{o \text{max}}^2.$$  

(24)

The value of $C_b$ is normally larger than the value of $C_s$. Consequently, the bigger the value of selected $C_b$ is, the lower the value of $V_{\text{chm}}$ will be. Moreover, if the value of $C_b$ increases, the voltage across the synchronous switch falls, but the time periods $t_{23}$, $t_{45}$, $t_{56}$, and $t_{67}$ during which the inductor energies are transferred to $C_b$ or the load rise.

4. CONVERTER FEATURES

The features of the proposed soft-switching converter are briefly summarized as follows.

(1) All of the active and passive semiconductor devices are turned on and off under exact ZVS and/or ZCS.

(2) The proposed converter has a simple structure, low cost, and ease of control.

(3) The converter acts as a conventional PWM converter during most of the switching cycles.

(4) The presented snubber cell can be easily applied to the other basic PWM DC-DC converters and to all switching converters.

(5) The proposed converter has a larger total efficiency and a wider load range.

(6) The main switch and the auxiliary switch are not subjected to additional voltage stresses. Current stress on the main switch is slightly higher, but current stress on the auxiliary switch is within safe limit.

5. SIMULATION AND EXPERIMENTAL RESULTS

A prototype of the proposed converter, as shown in Figure 1, has been built in the laboratory. The newly proposed converter operates with an input voltage $V_i = 12$ V, output voltage $V_o = 3.3$ V, load current of 11 A, and a switching frequency of 500 kHz. The converter is simulated using simulation software PSIM, version 6.0. The major parameters and components are given in Table 1.

Figures 4(a)–4(d) show the simulation results of the proposed converter and Figures 5(a)–5(d) present the experimental results. All the waveforms except the efficiency curve represent a time period of one switching cycle, which is 2 microseconds in this case. The amplitudes are denoted in Figure 4 with each of their waveforms, respectively.

5.1. Main switch $S$

It is noted from Figures 4(a) and 5(a) that the main switch $S$ is turned on under ZCS, and the body diode $D_1$ of synchronous switch $S_1$ is turned off under ZVS. The main switch takes the load current and the charging current of the capacitors $C_s$ and $C_b$. The inductor starts to transfer its stored energy to capacitors $C_s$ and $C_b$ during the turn-on period of main switch. The converter has not exceeded the voltage limits; however, the current stress is slightly higher for a very short period of time. The main switch also switches off under ZVS. The current and voltage wave shapes are identical to theoretical waveforms.

5.2. Synchronous switch $S_1$

After the main switch is turned on under ZCS, the body diode of synchronous switch is turned off under ZVS, which can be observed from Figures 4(b) and 5(b). The synchronous switch is turned on under ZCS when the main

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Table 1: Components used in the proposed converter.

<table>
<thead>
<tr>
<th>Component</th>
<th>Value/model</th>
<th>Simulation</th>
<th>Experiment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main switch ($S$)</td>
<td>Ideal</td>
<td>IRF1312</td>
<td></td>
</tr>
<tr>
<td>Synchronous switch ($S_1$)</td>
<td>Ideal</td>
<td>IRF1010E</td>
<td></td>
</tr>
<tr>
<td>Schottky diode ($D_{3s}$)</td>
<td>Ideal</td>
<td>MBR60L45CTG</td>
<td></td>
</tr>
<tr>
<td>Schottky diode ($D_{3b}$)</td>
<td>Ideal</td>
<td>MBR60L45CTG</td>
<td></td>
</tr>
<tr>
<td>Schottky diode ($D_{3s}$)</td>
<td>Ideal</td>
<td>MBR60L45CTG</td>
<td></td>
</tr>
<tr>
<td>Resonant inductor ($L_o$)</td>
<td>15 nH</td>
<td>15 nH</td>
<td></td>
</tr>
<tr>
<td>Resonant capacitor ($C_o$)</td>
<td>1 nF</td>
<td>1 nF</td>
<td></td>
</tr>
<tr>
<td>Buffer capacitor ($C_b$)</td>
<td>3.3 nF</td>
<td>3.3 nF</td>
<td></td>
</tr>
<tr>
<td>Output capacitor ($C_i$)</td>
<td>15 μF</td>
<td>15 μF</td>
<td></td>
</tr>
<tr>
<td>Output inductor ($L_o$)</td>
<td>5 μH</td>
<td>5 μH</td>
<td></td>
</tr>
</tbody>
</table>
switch is turned off under ZVS. After the turnoff of the main switch, both capacitors \( C_r \) and \( C_b \) are discharged. As soon as both capacitors are discharged near zero, the body diode of synchronous switch \( S_1 \) is turned on under ZVS. The converter has not exceeded the current limits; however, the voltage stress across the switch is slightly higher for a very short period of time. The synchronous switch operates within the safe limits, and it can be noted here that the conduction period of \( S_1 \) is more confining to the design values and it operates at a low power when compared to the other switches. The shapes of the figures are identified to confine much to the theoretical waveforms.

5.3. **Schottky diodes** \( D_{S1}, D_{S2}, \) and \( D_{S3} \)

The Schottky diodes work for a very short period to discharge the resonant capacitors \( C_r \) and \( C_b \) as can be observed from Figures 4(c), 4(d), 5(c), and 5(d). Moreover, it can be seen that the Schottky diodes \( D_{S1}, D_{S2}, \) and \( D_{S3} \) operate under soft-switching conditions. The Schottky diodes are turned on and off under ZVS. The conduction of Schottky diodes may cause a considerable drop in output voltage for low-power circuits, but due to the advancement in semiconductor techniques, Schottky diodes are also now available with a low-forward-voltage drop for high-frequency circuits.

![Simulated voltage and current waveforms: (a) main switch S: \( V_S, I_S \); (b) synchronous switch S1: \( V_{S1}, I_{S1} \); (c) diode \( D_{S1} \) and capacitor \( C_r \); (d) capacitor \( C_b \) and diode \( D_{S3} \).](image-url)
Figure 5: Experimental voltage and current waveforms: (a) main switch $S$: $V_S$, $I_S$ ($V$: 5 V/div, $I$: 10 A/div, time: 0.2 μs/div); (b) synchronous switch $S_1$: $V_{S1}$, $I_{S1}$ ($V$: 5 V/div, $I$: 10 A/div, time: 0.2 μs/div); (c) diode $D_{S1}$ and capacitor $C$: $V_{DS1}$, $V_{C}$ ($V$: 5 V/div, $I$: 2 V/div, time: 0.2 μs/div); (d) capacitor $C_b$ and diode $D_{S3}$: $V_{Cb}$, $V_{DS3}$ ($V$: 5 V/div, $I$: 2 V/div, time: 0.2 μs/div).

Additionally, during the turn-on and turnoff of main switch $S$ and synchronous switch $S_1$, a slight overlap occurs between their own voltages and currents. Therefore, the switching losses are zero, but a little additional conduction loss takes place, and so the conduction losses dominate the total loss in the soft-switching converter.

**Efficiency curve**

From Figure 6, it can be observed that the efficiency values of the soft-switching converter are relatively high with respect to those of the hard-switching converter. The efficiency values towards the minimum output power decrease naturally because the converter is designed for the maximum output current. At 70% output power, the overall efficiency of the proposed converter increases to about 96% from the value of 87% in its counterpart hard-switching converter. The high efficiency concludes the correctness of the design values.

**Figure 6: Efficiency curve.**

6. **CONCLUSION**

The concepts of ZVT used in medium and high power were implemented in synchronous buck converter, and it was shown that the switching losses in synchronous buck were eliminated. Besides, the main switch ZCS is turned on and ZVS is turned off. The synchronous switch is also turned on under ZCS and turned off under ZVS. Hence, switching losses are reduced and the newly proposed ZVT synchronous buck is highly efficient than the conventional converter. The additional voltage and current stresses on the main devices do not take place, and the auxiliary devices are subjected to allowable voltage and current values. Moreover, the converter has a simple structure, low cost, and ease of control. A prototype of a 3.3 V, 11 A, 500 kHz system was implemented to experimentally verify the improved performance.
REFERENCES


