Research Article

Local Biasing and the Use of Nullator-Norator Pairs in Analog Circuits Designs

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A new technique is presented for biasing of analog circuits. The biasing design begins with local biasing of the nonlinear components (transistors), done according to the pre-specified operating points (OPs) and for the best performance of the circuit. Next, the transistors are replaced with their linear models to perform the AC design. Upon finishing with the AC design we need to move from the local biasing to global (normal) biasing while the OPs are kept unchanged. Here fixators—nullators plus sources—are shown to be very instrumental and with norators—as the place holders for the DC supplies in the circuit—they make pairs. The solution of the circuit so prepared provides the DC supplies at the designated locations in the circuit. The rules to engage in circuit analysis with fixator-norator pairs are discussed, and numerous pitfalls in this line are specified. Finally, two design examples are worked out that clearly demonstrate the capability and power of the proposed technique for biasing any analog circuit.

1. Introduction

Biasing of large and complex analog circuits has always been a great challenge for the designers. The challenge is normally in two areas. First, to get the number of iterations minimized and make the convergence possible and quick; second, to move to the right regions of operations for the active components so that the output signals could get far from being distorted or clipped. Both problems become complex as the number of active devices increases, the design requirements become tighter, and more efficient designs are in demand. One difficulty appears to be the lack of separation between the linear and nonlinear components in the circuit during the process. Traditional biasing techniques deal with the circuit as a whole, with no break or circuit partitioning; hence, the complexity quickly increases as the circuit grows [1, 2].

Recently a new biasing technique has been introduced that somewhat breaks the tradition [3–5]. It starts with biasing nonlinear components (say transistors) individually and makes each transistor to become DC isolated and to operate at its own selective operating point (OP). Here each transistor is biased locally without interfering with other

components in the circuit. A major advantage in using this technique is to deal with nonlinearity locally and to avoid any nonlinear operation in the original circuit, as a whole. One may even claim zero nonlinearity being involved in this situation. This is because biasing individual transistors to operate at their desired OPs is just a matter of local sourcing.

In the method presented by Verhoeven et al. [3] the design of amplifiers is carried out linearly and in AC domain. Here the circuit biasing—performed at the end of the design—is reduced to just the transistors' biasing, which is again a local sourcing of the transistors, so that they can get to the OPs intended for each without being interfered by other DC sources. This technique makes each transistor DC isolate and it uses controlled sources for local adjustments. Although the controlled sources are later removed but initially they cause timely iterations until they are eliminated. In [4] this author presents a somewhat similar biasing method, called “local biasing.” Despite the technique used in [3], here no controlled source is used for the biasing purposes. In addition, it is shown in [3, 4] that in each locally biased port only one DC source delivers power to the device and the other source is sitting idle. As demonstrated, this property helps to cut down the number of biasing sources

in the circuit by half, and the other half can be replaced with coupling capacitors. This is of course for the case that the biasing voltage sources are sitting idle. Similarly, in the case of the current sources delivering zero power inductors can replace them.

With all advantages and tremendous simplifications that the local biasing offers for biasing complex analog circuits [4, 5], one major difficulty still remains to be addressed. The question is how to deal with those “scattered supplies” used in the circuit due to the local biasing? As expected, each bipolar transistor needs four (voltage and current) sources to get locally biased. There are known circuit techniques [3, 6] that are used to deal with the problem. The method proposed by Verhoeven et al. [3] uses shifts and other source transfer techniques to reduce the sources and push them to specific locations [6]. Techniques such as voltage dividing, source shifting, and current sourcing, and mirroring help to reduce the number of DC supplies and push them to the right locations in the circuit. As expected, the method is more gradual and long and tedious procedures used often reduce the attraction and practicality of these methods. In addition, by implementing these procedures, there is no guaranty to ensure an optimal or a desirable solution.

In our methodology we are offering a new source transformation technique that despite the conventional one it does the entire process in a single step. We may begin the design of an analog circuit by choosing a desirable circuit topology, first. In case the design uses discrete components the nonlinear components (transistors) represent the drivers that must be biased to selected OPs. Now, because the regions of operations for the drivers are specified we can simply replace the transistors by their small signal linear models, bypass the entire nonlinearity, and go directly for the design of the (linearized) AC circuit. Note that because no DC analysis is attempted yet then no DC supplies are specified. Indeed in our methodology the circuit biasing is pushed to the end and it begins when the AC design is successfully completed, and the regions of operations (or simply OPs) for the drivers are specified, for maximum output swings and minimum distortions.

On the other hand, if the target circuit is an integrated circuit then we are facing with two types of nonlinear components: the drivers and the supporting components, such as current sources, current mirrors, and active loads. Similar to the previous case here we also start the design for AC signals. We replace the drivers with their small signal linear models at the desired Ops, and the other nonlinear supporting components are also replaced with their linearized equivalent impedances for small signals (such as a dynamic load resistance r_o), as specified by the design criteria.

Up to this point, the process of analog circuit design has followed a conventional routine. We still need to know how to design the biasing of the circuit to fulfill the following two conditions: (i) have the DC (voltage) supplies with specified values located at their selective locations in the circuit, and (ii) have the drivers, as well as the supporting components, biased at their selective OPs. In most cases the location of supplies, such as V_{CC} and V_{DD} , and their

values are predetermined for the design. In such cases the question is how to fulfill both set of requirements: (i) have the DC power supplies with specified values and specified locations in the circuit, and (ii) achieve the AC design requirements without any nonlinear iterations and with minimum design efforts? As discussed earlier, one way to do this is to design for the AC case first with the load and node impedances required for the design and do the biasing later. Traditional biasing methods start with fixed supplies at fixed locations in the circuit; whereas our method is to start biasing the individual transistors and move the biasing sources to the desired locations later. With the first method nonlinearity is unavoidable and because of the fixed AC models of the transistors fulfilling all design specifications is hard and time consuming. However, the difficulty with the individually biasing the transistors is to end up with too many (voltage and current) sources in the circuit, and unless we move all the sources to one or two designated locations, for the DC supplies, the job is incomplete. Again, what makes the proposed technique more attractive is the fact that in one step this move takes place and those one or two supplies get replaced for all the sources used for the individual transistors biasing. This certainly eliminates all those conventional source reduction and transformation as well.

The tool we are going to use to achieve our goal is fixator-norator pair (*this is similar to nullor pair except that a fixator-norator pair can accept sources*). It is shown that while the use of fixators helps to keep the critical biasing specs unchanged the matching norators actually find the values and the locations of the DC supplies. As it is shown, the use of fixator-norator pairs (or actually nullor pairs) is temporary here. The pair actually works as a catalyst and get removed from the circuit after the DC supplies are allocated. This suggests that, there is no need to replace the norators with actual devices (such as Op-Amps or OTAs). In fact, because of the temporary nature of the nullor pairs ideal controlled sources of type VCVS, VCCS, C CVS, and CCCS with high gains, approaching infinity, will perfectly do the job.

The use of nullor pair in analog designs has been very extensive [7–9]. Telelo-Cuautle also introduces biasing techniques for amplifiers at nullor levels [10, 11]. These techniques use nullor pairs and their governing rules to simplify the biasing. The pairs are then replaced with transistors or Op-Amps for the final design. Haigh, Clarke, and Radmore introduce a new framework for linear active circuits that use a special type of limit variable in the circuit admittance matrix. This variable being initially finite can approach infinity resembling high gain Op-Amps or transistors as nullors [12–14]. Claudio Beccari [15] also uses the nullor concept eloquently to find and allocate the transmission zeros in a circuit.

The method proposed in this paper is using nullor pairs (in form of fixator-norator pairs) quite differently. The pairs are used as tools to reallocate the DC supplies and conduct the DC power to the transistors and then disappear. It is only during the circuit analysis and simulation that, in a fixator-norator pair, the fixator is used to sense certain specified current or voltage (OP) in the circuit. This sensing then tries

FIGURE 1: Port nullification procedure.

to control a voltage across or a current through the associated norator. As a result, the voltage or current found for each norator is, in fact, an indication that indeed a DC (voltage or current) supply exists at the location that has caused the biasing. We repeat this for all critical ports (with biasing specified) until all supplies are allocated.

The rest of the materials in this paper are arranged as follows. Section 2 is on fixator-norator pairs. The behavior and properties of fixators and norators are discussed here. Local biasing is reviewed in Section 3. Models of locally biased MOS and bipolar transistors are given in this section. The use of fixator-norator pairs in global biasing of analog circuits is investigated in Section 4. Rules governing the fixators and norators are also discussed here. Section 5 is on implementation aspects of fixator-norator pairs for biasing. An algorithm, developed in this section, provides a systematic procedure into the design of biasing for analog circuits. Two examples are worked out in Section 6 that use the methodology introduced here as the basis for the biasing design of analog circuits. Finally, Section 7 concludes our discussions on analog circuit design with emphasis on biasing.

2. Nullification and Fixators

First we need to define some terms that are used in this paper [4]. Also, all our discussions here apply to DC signals and biasing, unless stated otherwise.

2.1. Nullification

Null port. consider two powered networks. (a *powered network* is a network with at least one power supply). N_1 and N_2 connected through a port $k(v_k, i_k)$. Port $k(v_k, i_k)$ is said to be null if both voltage v_k and current i_k are zero.

Port nullification. consider two powered networks N_1 and N_2 connected through a port $j(v_j, i_j)$. Port $j(v_j, i_j)$ is nullified if it is augmented, from both sides (N_1 and N_2), by current sources i_j and voltage sources v_j so that a null port $k(v_k, i_k)$ is created as a result, as shown in Figure 1.

Apparently, there will be no change in the currents and voltages within both networks N_1 and N_2 if we disjoint the two networks at port $k(v_k, i_k)$ and connect each to a nullator, as illustrated in Figure 2. This results in a new finding as follows.

FIGURE 2: Two networks N_1 and N_2 disjointed at port $k(v_k, i_k)$ and each terminated by a nullator.

FIGURE 3: (a) Voltage Fixator; (b) current Fixator; (c) the symbol.

2.2. Fixator and Fixator Modeling.

Fixator. a two-terminal component (a component here can be of any size two terminal network). in a circuit is called a Fixator if both voltage across the component terminals and the current through the component represent two independent sources.

One way to create a fixator with voltage V and current I is to have a nullator parallel with a current source I and in series with a voltage source V , as depicted in Figures 3(a) and 3(b). Note the difference between the two fixators $Fx(V, I)$ and $Fx(I, V)$. In $Fx(V, I)$ the voltage source V provides (or consumes) power and the current source I is sitting idle; whereas, in $Fx(I, V)$ the current source I provides (or consumes) power and the voltage source V is sitting idle.

Now, referring to Figure 2, we realize that both ports in networks N_1 and N_2 are terminated with Fixators. This leads to the following property.

Property 1. Consider two powered networks N_1 and N_2 connected through a port $j(v_j, i_j)$, and no other external component is connected to N_1 or N_2 . There will be no (current or voltage) change in the network N_2 if N_1 is replaced with a fixator $Fx(v_j, -i_j)$, as shown in Figure 4. Similarly, there will be no change in the network N_1 if N_2 is replaced with a fixator $Fx(v_j, i_j)$.

Before we move on, it is important to compare the fixator $Fx(v_j, -i_j)$, replacing N_1 in Figure 4, with N_1 Thevenin or Norton equivalent circuits, which also can replace N_1 . This topic is fully discussed in [16] and it is briefly given here. In fact, instead of replacing N_1 with its Thevenin or Norton model we can alternatively replace it with a more generalized model known as nH (nullified Hybrid) model [16], where instead of one, voltage or current, source an nH-model has

FIGURE 4: Network N_2 terminated with a Fixator.

one voltage and one current source combined as shown in Figure 5(a). It is easy to show that both Thevenin and Norton equivalent circuits are in fact two special cases of nH-models [16] for a two-terminal network. Note also that an nH-model can model a nonlinear two-terminal network as well, as represented in Figure 5(b). Now, we are closer to the result we aimed at! In comparing the network N_2 in Figure 5(b) with that in Figure 2 we realize that the only difference between the two is that in Figure 2 the network N_1 , with no source, is replaced with a nullator. This may look rather strange and seems to violate the circuit (KVL and KCL) laws! However, it makes sense if we consider the situation as a “snap shot” of the circuit. Here is the difference: the circuit in Figure 5 allows us to change the component values inside N_2 and observe the changed made at the port J, where as in Figure 2, we are not allowed to make any changes inside N_2 that causes V_j or I_j to change. By the way, this means that changes inside N_2 that do not affect the port values are allowed. One may then ask, how can we change the component values inside N_2 and still use Figure 2 for modeling with the expectation that V_j and I_j remain unchanged (*we are of course talking about nonseparable networks here*)? The answer to this question is as follows. When we change the component values inside N_2 and expect not to change anything at the port J then we need to have another component, $p(V_p, I_p)$, inside N_2 with unspecified voltage and current so that the changes, expected to appear at the port J, are “transferred” into the changes in V_p and I_p . This component, p , is called norator. Therefore, to have the circuit laws in place the fixators (nullators) and norators must appear in pairs in a circuit.

2.3. Rules Governing Fixators and Norators. Here are some of the useful properties of fixators and norators. First, notice that a nullator is a special case of a fixator represented by $Fx(0, 0)$, where both the device voltage and current are zero. Therefore, like nullators, fixators must pair with norators in order to have computational stability in a circuit. We should also remember that a fixator represents a current source and a voltage source combined. For instance, a current source in series with a fixator may violate the KCL, and a voltage source in parallel with a fixator may violate the KVL. In general, a cutset of fixators with or without current sources may violate the KCL and a loop of fixators with or without voltage sources may violate the KVL. Here are some other properties of the pair, as discussed in [17]

- (i) The power consumed in a fixator $Fx(V, I)$ is $P = V * I$.
- (ii) A resistance R in series with a $Fx(V, I)$ is absorbed by the fixator and the fixator becomes $Fx(V_1, I)$, where $V_1 = V + R * I$. A resistance R in parallel with a $Fx(V, I)$ is absorbed by the fixator and the fixator becomes $Fx(V, I_1)$, where $I_1 = I + V/R$.
- (iii) A current source I_s in parallel with a $Fx(V, I)$ is absorbed by the fixator and the fixator becomes $Fx(V, I_1)$, where $I_1 = I + I_s$.
- (iv) A voltage source V_s in series with a $Fx(V, I)$ is absorbed by the fixator and the fixator becomes $Fx(V_1, I)$; where $V_1 = V + V_s$.
- (v) A current source in series with a norator absorbs the norator; a voltage source in parallel with a norator absorbs the norator. In addition, a current source in parallel with a norator is absorbed by the norator; a voltage source in series with a norator is absorbed by the norator.
- (vi) A resistance in series or in parallel with a norator is absorbed by the norator.
- (vii) A norator in series with a fixator $Fx(V, I)$ becomes a current source I ; a norator in parallel with a fixator $Fx(V, I)$ becomes a voltage source V .

3. Local Biasing

Local biasing (LB). A port is locally biased if it is nullified. Likewise, a network or a component is locally biased if all its ports are nullified.

Apparently, local biasing of a network or a component is not unique. A port can be locally biased for any selection of an OP on its characteristic curve. This is also true for a component with multiple ports. Evidently, connecting a locally biased device to a network with no DC (voltage or current) supply does not change the biasing condition of the device. This simply means that a locally biased device does not need any external DC supply to keep it operating, while still responding normally to any AC signal.

Note that when we locally bias nonlinear components in a circuit, we in fact replace the DC power supplies with local sources that are only responsible to provide biasing/power to individual devices. This certainly gives a choice to a circuit designer to select his/her own operating regions for nonlinear devices in the circuit and bias them on spot without going through timely iterations, typically required for nonlinear designs. In fact when all the transistors are locally biased there is no need to have DC supply for the rest of the circuit (*diodes and other nonlinear components may also be present in a nonlinear circuit, but for simplicity we refer all to transistors*). Therefore, by replacing the transistors with their linear models the circuit becomes entirely linear suitable for AC design. In addition, as discussed in [5], having local biasing reduces the DC power consumption to its minimum, and just enough to bias the transistors individually. This means that the signals in the rest of the circuit always remain AC and unaffected.

FIGURE 5: (a) nH-model for linear N_1 ; (b) nH-model for non-linear N_1 .

Another important property of the local biasing is its locality and the possibility of (DC) circuit partitioning (divide and conquer) without affecting the integrity and the operation of the AC circuit. The local biasing allows the designer to locally tune the circuit and make changes in the operating regions of individual devices or a local subcircuit without disturbing the rest of the circuit. There are number of applications using this property of the local biasing, such as replacing some faulty transistors with new ones, and even with different types of transistors, for instance, changing BJTs to MOS transistors or vice versa.

Another application of the local biasing is in local testing and debugging of a complex circuit. For example, consider the circuit in Figure 6(a), where the MOS transistor M is malfunctioning because its output OP, at $Q(V, I)$, is at the wrong place on the characteristic curve (Figure 6(b)). To correct the situation we need to move the OP to the right on the curve, positioning it at $Q_1(V+dV, I+dI)$ as indicated in Figure 6(b). Here the local biasing will help us by augment M with two difference sources dV and dI , as shown in Figure 6(c), which causes the OP of the transistor to move from Q to Q_1 without affecting the rest of the circuit. Later, we may need to get rid of the sources, dV and dI , and move them inside N to get integrated with the rest of the DC supplies in the network, but that is a separate issue.

3.1. Component Biasing. Within the three major semiconductor components p - n junction diodes are one-port devices. Bipolar-junction Transistors are generally considered two-ports, but they can be turned into two one-port devices if Ebers-Moll or the Transport large signal model [1] is used. MOS transistors are considered three-port devices but only four sources are used to locally bias the device. This is because for the drain-source we need both I_D and V_{DS} sources to nullify the port; whereas for the gate-source and the substrate-source we only need V_{GS} and V_{BS} to nullify the ports, respectively. Figure 7 illustrates both an nMOS and a pMOS locally biased; however, for simplicity we are going to drop the substrate effect, V_{BS} , later in our discussion. Similarly, Figure 8 shows an npn and a pnp transistors locally biased.

4. Global Biasing

With all advantages of the local biasing, one major difficulty remains unsolved, and that is the “scattered supplies”

throughout the circuit. Although through circuit manipulations such as current mirroring, voltage dividing and source transformation the problem may be reduced to certain degrees but overall the problem of the scattered supplies in large circuits makes the design difficult, inefficient, costly, and mostly impractical.

In our approach, the problem is dealt with in a single step without any iteration or source shifting and transforming. In our design procedure we go through two major steps. In the first step we translate the design specs into the transistors’ OPs using the local biasing. Then using the transistors’ linear models we perform the linearized circuit design for AC signals. In the second step we try to remove the scattered sources caused by the local biasing and replace them with regular DC supplies in the circuit. Property 2 is very instrumental in this approach.

Property 2. A locally biased component within a network N can be removed and be replaced with nullators, one for each port, without affecting the DC currents and voltages within the network N .

Note that locally biasing of a component produces zero voltages and currents at its ports without affecting its internal currents and voltages. This simply means that, in an analog circuit when certain components are locally biased they can be separated and removed from the main circuit without imposing any change on the circuit operation or on the biasing conditions of those components themselves, provided that each disjointed port, from both sides is connected to a nullator (Figure 2). In addition, applying Property 2 to a nonlinear circuit removes the nonlinearities (transistors) from the circuit and makes them perform linearly.

4.1. Port Modeling with Fixators. Now, we are ready to go one step further by introducing Property 3.

Property 3. A two-terminal component in a circuit (linear or nonlinear), such as a p - n junction diode, that is biased by current I_D and exhibits a junction voltage V_D can be replaced with a fixator $Fx(I_D, V_D)$ without causing any change in the currents and voltages within the rest of the circuit.

Property 3 directly results from Property 1. Note that $Fx(I_D, V_D)$ models a diode only when the diode is in a

FIGURE 6: Partially locally biasing an MOS in a circuit.

FIGURE 7: Locally biased (a) NMOS, and (b) PMOS transistors.

FIGURE 9: Fixator models of nMOS and pMOS transistors when globally biased for V_{GS} (V_{SG}), V_{DS} (V_{SD}), I_D , and V_{BS} (V_{SB}). Both symbolic and expanded versions are shown.

FIGURE 8: Locally biased (a) NPN, and (b) PNP transistors.

circuit and globally (not locally) biased with I_D and V_D . Property 3 can also be extended to include the components with multiple ports such as bipolar and MOS transistors. Figure 9 shows the fixator models of nMOS and pMOS transistors when they are globally biased for V_{GS} (V_{SG}), V_{DS} (V_{SD}), I_D , and V_{BS} (V_{SB}). Likewise, Figure 10 depicts the fixator models of npn and pnp transistors when they are globally biased for V_{BE} (V_{EB}), V_{CE} (V_{EC}), and I_C . Note that, similar to Property 2, applying Property 3 to a nonlinear circuit removes the nonlinearities (transistors) and makes the circuit perform linearly.

There is a clear distinction between Property 2 and Property 3 however. Property 2 shows how we can remove a locally biased port (component) and replace it with a nullator; whereas, Property 3 makes us replace a globally biased port (component) with a fixator. For Property 2 there is no DC power external to the locally biased components to worry about; whereas Property 3 indicates that there must be DC sources external to the components that provide the biasing for them. Where are these sources in the circuit!? So we need to concentrate more on Property 3 now. What is missing is how to produce the global biasing, capable of producing fixators—biased components—that follow the design specs (OPs).

Indeed the job turns out to be already resolved. Earlier we discussed the problem in a previous section; that is, for each fixator we need to assign one norator inside the (linear) circuit. We can assume that this norator acts as a placeholder for a DC supply in the circuit. What this basically means is that, when we replace a transistor with its fixator model, in exchange we are getting a ticket to assign a DC source in the circuit wherever we like, provided that this DC source is “reachable” by the fixator. This is indeed how the fixators

FIGURE 10: Fixator models of npn and pnp transistors when globally biased for V_{BE} (V_{EB}), V_{CE} (V_{EC}), and I_C (the expanded versions not shown).

(globally biased transistors) can manage to have the DC supplies in the circuit in the designated locations. We still need one more step to go! Up to this point the norators—the matching partners of the fixator-norator pairs—can be assigned to the locations that are reserved for the global DC supplies. But we still need to find the values of those supplies. This is done through the circuit analysis created up to this point. The circuit here is a linear circuit with fixator-norator pairs; there is no DC supply in the circuit except each fixator does represent a fixed voltage and a fixed current source (*in partial DC biasing design cases it is possible to have DC supplies as well as fixator-norator pairs in the circuit*). When the circuit analysis is complete each norator in the circuit can be replaced either (i) with a voltage source equivalent to the voltage across the norator, or (ii) with a current source equivalent to the current through the norator.

This study still needs to address two questions. First, what can we do if the DC supplies (mainly the voltage sources) so obtained are beyond the conventional and standard values—12 V, 5 V, 3.3 V, and so on? In case of smaller voltage values techniques such as voltage dividers can help. For larger values, however, the solution may get more involved. An adjustment in the “power conducting” resistors is one possibility to do the job. Linearity scaling and other linear methods are also useful to adjust the supplies to the conventional values. The second question deals with having the number of fixators and norators unequal. Typically the number of fixators exceeds the number of norators. For example, for a three-stage amplifier with three driver transistors we might have as many as six fixators; whereas one power supply, V_{CC} , can be represented by only one norator. There are different approaches to handle this problem, and some are still under investigation. One approach is to assume multiple virtual supplies that can later be easily combined into one or two actual supplies. Another approach is to reduce the number of fixators by removing “noncritical” ones from the list.

In general there are two ways we can think of a good biasing design for an analog circuit. One way is to take care of each and every individual transistor in a circuit and bias it to operate at its best OP. With this approach we definitely need as many fixators as there are ports for the nonlinear devices. A second approach, however, is to classify the nonlinear ports as “critical” (*a port is critical if the port voltage or its current must meet the design specifications*) and “noncritical” ports, and assign fixators only to those critical ports. We will be more covering this subject in the next section.

5. Implementation

Design of high performance analog circuits can be a complex and often a multistage processes—typically noise, distortion, gain, bandwidth, and biasing. One approach to simplify the design and cut loops and feedbacks between the stages is to use as much orthogonally between stages as possible [3]. In our proposed method, this orthogonally is practiced between the circuit performances and the biasing of the components, or simply between AC and DC circuit designs. The first task is to design for the circuit performances, mainly noise, signal power, and bandwidth [3]. In this study, we only deal with the biasing part of the design. A full discussion on the performance design can be found in [3].

We can in fact start with a certain circuit topology suitable for our design, then select regions of operations for the transistors so that the design requirements can be fulfilled. After designing the circuit for AC signals the time comes to bias the circuit with DC supplies (voltages and currents) so that those selected operating regions, and therefore, the design requirements are best met. Section 5.1 provides a systematic procedure to do the circuit biasing using the proposed new approach.

5.1. Algorithm 1. Preparation. given the design specification, we begin with the performance design by selecting a working circuit topology. We then choose the right OPs for the drivers so that we can best meet the design requirements. In the next step, we replace all the transistors with their small signal linear models so that the entire circuit becomes linearly ready for the AC design. Upon the completion of the performance (AC) design, we begin doing the biasing design as follows.

- (1) Assign one fixator, carrying the biasing spec, to each “critical” transistor port. Also assign one norator to each to-be-specified DC supply in the circuit. If they do not match, reduce the number of critical ports so that the number of the fixators and norators becomes equal.
- (2) Next, pair each norator with a fixator in the circuit. This step is rather critical and needs some care (see “Singularity and Circuit Divergence”). In general, any pair must work (although may not be optimal), except for the cases where a fixator is not sensitive to the changes in the norator.
- (3) Assign one controlled source to each pair of fixator-norator. It is permissible to assume an ideal controlled source with very high gain; this is because these controlled sources will disappear later, leaving the DC supplies behind. A controlled source can be of type VCVS, VCCS, CCCS, or CVC; the choice depends on the sensitivity issue, stated in step 2.
- (4) Solve the linear circuit equations so prepared and the DC solution (simulation) provides the currents and voltages for the circuit components including those for the norators, represented by the controlled sources.

- (5) Remove all the controlled sources from the circuit and replace each with either a voltage source, V_j , or a current source, I_j , where V_j and I_j are the voltage and current found for the controlled source (norator).

Now that we are done with the biasing design there are still issues that must be dealt with before we leave the subject. First, as mentioned earlier, the equivalency of number of fixators (nullators) and norators is necessary to solve the circuit equations but it is not sufficient. The issue is related to the independency of the circuit (KCL and KVL) equations. As we discussed in Section 2, a fixator carries the properties of a voltage source and a current source combined; therefore, it cannot be in a loop with voltage sources, neither it can be in a cutset of current source.

The second problem is the fact that with each transistor added to the circuit at least two fixators (for input and output ports) are added to the linear circuit; whereas the number of supplies are usually much more limited. One way to deal with this problem is to have a selective number of the (transistor) ports to be critical; only those that directly reflect on the performance and effectiveness of the design. For example, we may consider the output voltage swing of an amplifier as a critical component of the design for reducing the distortion. Similarly, we may assume the input stage of an amplifier as a critical stage for noise reduction. As another example, suppose we are designing a multistage amplifier where the first stage is presumably going to be a preamp and the possibility is that the voltage swing for this stage may stay within, say 100 mV. Therefore, as long as the (driver) transistor operates in the active region the chances are that it may always stay in that region, even during the AC operation; hence, this transistor may be labeled as noncritical. Now, it is a matter of the designer skill to separate critical ports from those non-critical ones and assign fixators only to those critical.

Another solution to the problem is to prioritize. A skilful designer can always prioritize the design specs so that the most critical criteria come first and he/she can stop when the numbers match the number of unknown supplies. There are also ways to increase the number of norators to match the number of fixators. For instance, in designing a multistage amplifier with only one DC power supply, say V_{DD} , we can initially start with multiple supplies—one for each stage, for example—and then combining to one by doing certain adjustments. Techniques such as using voltage dividers and current mirrors can also help in increasing the number of norators.

Another issue in the circuits with fixator-norator pairs is, in fact, the lack of sufficient sensitivity between the fixator and the norator in a pair. If a variation in a norator does not reach to the corresponding fixator in a pair the link is lost. For example, if there is no feedback from the output stage to the input stage, in a multi-stage amplifier, then a fixator at the input stage (say, V_{BE} of the input driver) cannot pair with a norator at the output stage. In addition, if a norator and a fixator are placed in a positive feedback loop divergence might happen. This subject is discussed next.

FIGURE 11: Initial configuration of an MOS feedback amplifier.

5.2. Singularity and Circuit Divergence. There is a word of cushion here; our experiments show that in large circuits with numerous critical specs, and hence numerous fixator-norator pairs, there is a possibility that singularity or circuit divergence might happen. In a way, the problem is related to the independency in the circuit equations (KVL and KCL), and possible inequality that might happen between the number of independent norators and fixators, although they might have originally set equal. The problem is often caused by violating the rules for norators and fixators, explained in Section 2. For example, a fixator should be treated as both a voltage source and a current source; therefore, it cannot be in a loop of all fixators and voltage sources; or a fixator cannot be in a cutset of all fixators and current sources. Other difficulties may be the lack of enough sensitivity between a fixator and a norator in a pair. If a change in a norator does not reach to the corresponding fixator the link is broken. For example, in a design, if there is no feedback from the output stage to the input stage, then a fixator at the input stage (say V_{GS} of the input driver) cannot pair with a norator at the output stage. Finally, if a fixator and a norator are positioned in a positive feedback loop divergence might happen.

6. Examples

The following examples demonstrate the biasing design flow for two cases. Example 1 is a two-stage MOS amplifier with feedback where the biasing of both transistors is specified for the design. Example 2 is also a two-stage BJT differential amplifier with feedback, entirely designed in [3].

Example 1. Consider a two-stage MOS amplifier with feedback [2], shown in Figure 11. The schematic provides the topology of the design but the circuit values are left to be specified. We start the design by selecting the desirable OPs for the MOS transistors to meet the design specs. The selected values for V_{GS} , V_{DS} , and I_D , for both transistors, are provided in Table 1 (for simplicity the body effect is ignored).

FIGURE 12: The linear DC modeling of the amplifier, using the fixator-norator modeling concept for the MOS transistors.

TABLE 1: Specified design values for the MOS transistors.

Devices	V_{GS}	I_D	V_{DS}
M_1	2.0 V	140 μ A	1.9 V
M_2	-1.7 V	-120 μ A	-2.7 V

Given the selected OPs our next job is to create fixator models that represent fixed OPs for the transistor port (Alg.#1). These models are then substituted for the transistors in the circuit changing it to a linear circuit (Figure 12). The next step is to identify the locations of the DC supplies for the general biasing. These locations could be anywhere in the circuit as long as the sensitivity issue (discussed in Section 5) is taken care of. However, looking at Figure 11 we realize that the supplies' locations, namely, V_{DD} , V_{SS} , V_{GG} , and I_S , are already determined; hence, only their values remain to be evaluated. To do this we assign one norator to each supply location, as indicated in Figure 12. Note that it so happens that the number of fixators and norators match in this case and no other supply is present in the circuit. This is a special case of "total" circuit biasing (Alg.#2).

We are now ready to solve the linear circuit with fixator-norator (or rather nullor) pairs. SPICE cannot directly solve the circuit equations with nullors; but if we carefully replace each pair with an ideal high-gain dependent source the simulator solves the circuit equations and provides the currents and voltages for the elements in the circuit, including those for the norators (Alg.#3). Note that the use of high-gain dependent source for this purpose is just temporary (for the lack of nullor model representation in the simulator) and do not appear in the actual design. After the voltages and currents for the norators are found it is then our choice to replace each with either a voltage source or a current source (Alg.#4).

Up to this point the biasing design is theoretically over; however, at this stage we may need to reassign or adjust other circuit parameters such as the power-conducting resistor values (conducting the DC power to the transistors) in the circuit. This is often required in cases when the DC voltage supplies, resulted from the circuit simulation, are not within the conventional rating.

Another point of caution is that this fixator modeling of transistors is developed only for DC biasing. Thus, for AC analysis and design of analog circuits we still need to replace the transistors with their linear small signal models. The advantage of fixator modeling, however, is that it directly targets specified OPs for the devices; hence, to get the linear models for the transistors all we need is to refer to the device characteristics at those OPs.

Next, for the resistor values $R_1 = 10$ K, $R_2 = 50$ K, $R_3 = 15$ K, $R_4 = 3$ K, and $R_5 = 20$ K we simulate the design using WinSPICE. A part of the simulation code is shown below with high gain dependent sources.

```

vdn 7 52 1.9
Vgn 3 32 2.9
vdp 8 62 2.7
vgp 72 7 1.7

in 7 5 140u
ip 8 6 120u
fs 5 53 vnd 1000MEG
hgg 3 0 vng 1000MEG
hss 2 0 vpd 1000MEG
hdd 1 0 vpg 1000MEG

```

Note that eight distinct values for the fixators are provided (two zeros are not shown). For the norators, the first one is a CCCS and the next three are C CVS, all with gain of 10^9 . The result of the simulation is also given below.

```

TEMP = 27 deg C
DC analysis... 100%%
v(1) = 5.140025e+00 VDD
v(2) = 5.100133e+00 VSS
v(3) = 4.040102e+00 VGG
vis#branch = 4.399384e-05 IS
WinSpice 1 ->

```

Evidently, with slight adjustments to the resistors that conduct DC current to the transistors (R_1 to R_5) we can get $V_{DD} = 5$ V, $V_{SS} = 5$ V, $V_{GG} = 4$ V and, $I_S = 44$ μ A for this design (Alg.#5). This completes the DC biasing of the feedback amplifier. Finally, the MOS transistors must be sized to deliver the currents required. For fixed $L = 2$ μ m and with a simple calculation we get $Wn = 20$ μ m and $Wp = 60$ μ m for the transistors.

FIGURE 13: A three-stage amplifier topology after going through the performance AC design [3].

Example 2. This example presents a negative feedback amplifier, fully explained in [3]. Figure 13 shows a schematic of the amplifier after it has gone through the performance design in the three areas: noise reduction, clipping/distortion reduction, and high loop-gain-poles-product (*for details please refer to Chapter 10 in [3]*). To perform the biasing of the circuit we need to first specify the values for the DC supplies and their locations in the circuit. Next, we need to select the OPs for the transistors so that they can fulfill the design specs. For the actual power supplies, we choose two DC sources of 4 V and $-4V$, as selected in [3]. For other components conducting the DC power to the drivers we notice from the amplifier performance design (Figure 13) that the followings must be taken care of.

- (i) The emitters of Q_1 and Q_2 must be driven by a high impedance current source, I_e .
- (ii) The base of Q_2 must be driven by a low impedance voltage source, V_{b2} .
- (iii) The collector of Q_1 can be driven directly by V_{CC} .
- (iv) The collector of both Q_2 and Q_3 must be driven by high impedance current sources I_{S2} and I_{S3} , to maximize the gain.
- (v) The base current of Q_1 can be provided through a feedback resistor R_f (*the resistance R_f is in the bias loop and part of a required AC filter*).

For this particular design we choose the collector-emitter voltages of the transistors (v_{ce2} and v_{ce3}) as the “critical” design values, except for V_{ce1} of Q_1 , which is “non-critical,” directly connected to V_{CC} . Also all three collector currents i_{c1} , i_{c2} , and i_{c3} are also considered “critical. Table 2, columns 1 and 2, provides all five critical values for the OPs and also all five fixators that keep the critical values fixed during the design (Alg.#1). Column 3 shows the matching norators replaced with appropriate voltage source, current sources and one with feedback resistor (Alg.#2). Figure 14 is extracted from Figure 13 after the fixator-norator pairs, specified in Table 2, are added to the circuit.

Below is a piece of the WinSPICE program code simulating the DC biasing of the amplifier. Note that each fixator-norator pair is simulated by a very high gain controlled source (namely, VCVS, CCVS, VCCS, CCCS, and VCCS in sequence) (Alg.#3).

TABLE 2: Bias design specs and fixator-norators.

Critical specs	Fixator representations	Norator representations
$I_{C1} = 0.1 \text{ mA}$	$\text{Fx}(0, 0.1 \text{ mA})$	R_f
$V_{CE2} = 0.67 \text{ V}$	$\text{Fx}(0.67 \text{ V}, 0)$	V_{B2}
$I_{C2} = 0.5 \text{ mA}$	$\text{Fx}(0, 0.5 \text{ mA})$	I_E
$V_{CE3} = 2.2 \text{ V}$	$\text{Fx}(2.2 \text{ V}, 0)$	I_{S3}
$I_{C3} = 3.6 \text{ mA}$	$\text{Fx}(0, 3.6 \text{ mA})$	I_{S2}

TABLE 3: Component values for the specified biasing.

$R_f = 1.53 \text{ MEG}\Omega$
$V_{B2} = 0.677 \text{ V}$
$I_E = 0.607 \text{ mA}$
$I_{S3} = 3.601 \text{ mA}$
$I_{S2} = 0.523 \text{ mA}$

ic1	2	a	DC	1.0e-04
e1	4	51	a	2
vce2	c	7	DC	0.67
hb2	Vb2	0	vce2	1000MEG
ic2	3	c	DC	0.5m
ge	7	11	3	c
vce3	e	0	DC	2.2
fc3	21	4	vce3	1000MEG
ic3	4	e	DC	3.6m
gc2	12	3	4	e

The results from the WinSPICE simulation are shown and listed in Table 3 (Alg.#4).

```

TEMP = 27 deg C
DC analysis... 100%
(v(4)-v(5))/vf#branch = 1.528640e+06
vb2 = 6.770538e-01
ve#branch = 6.068945e-04
vs3#branch = 3.601024e-03
vs2#branch = 5.229127e-04
WinSpice 6 ->

```

Finally, we remove the controlled sources (representing the fixator-norator pairs) from the circuit and replace each with the computed voltage source, current sources, and one feedback resistance (Alg.#5). The final amplifier so designed is depicted in Figure 15 (*for simplicity the current sources are presented in their ideal form in Figure 12. A detailed current sourcing and mirroring can be found in [3]*). As expected, the resulted DC sourcing matches with those in [3]; here obtained much quicker.

FIGURE 14: The three stage amplifier with fixator-norator pairs indicating the biasing design specs.

FIGURE 15: The three stage amplifier with complete biasing.

6.1. Some Potential Impacts of the Proposed Methodology. (this Discussion Was Suggested by One of the Reviewers.)

We believe that the proposed methodology will have a tremendous impact to the research, to circuit designers, and to analog circuit design as a whole. The changes and effects are shown to be so vast and extensive that it can be interpreted as the beginning of a new era in analog circuit designs. Here are some of the evidences, discussed earlier.

- (i) No matter how complex, the nonlinearity in analog designs is entirely removed and is placed on the linearized equivalent circuit.
- (ii) If selected, each transistor (nonlinear component) is individually biased to the selective and desirable OPs.
- (iii) It is shown that local biasing minimizes the DC power consumption in the circuit. In general, the methodology can be used to reduce the DC power consumption.
- (iv) The proposed method is not a destructive one. A mixture of the traditional and the new method is possible for the design, and in fact is recommended for circuit modification and debugging.

This is just the beginning of the change; because we are only dealing with DC analysis and design of analog circuits. The possibility of applying the methodology, such as fixator-norator pairs, in AC design of analog circuits is quite high, and under investigation.

What it brings for a designer is simplicity, time, and management. It brings simplicity because no matter how complex the circuit might be it can be linearized. The designer can save time because by linearization he/she has entirely removed the nonlinear iterations from the operations, typically needed for nonlinear circuits. The designer is in full control and management because he/she is not facing with a complex network of mixed linear and nonlinear components but individual transistors to assume the right OPs, getting the liner models for the transistors and finally solve for the entire linear circuit for results. Because of the exact and selective environment provided the designer is capable to accurately calculate for possible distortions, noise, bandwidth, power, and other design attributes.

The impact on the research and on analog circuit design as a whole is also very high and promising. As mentioned earlier, work still has to be done on the AC aspects of the design using the new methodology. Getting “scattered supplies” within the circuit to move them to the designated locations with assigned values, in a single step, is by itself a great achievement and worth pursuing further.

Another important feature of the proposed methodology is its unrestricted use of the special biasing for any type of analog circuits. As we have always referred to “analog circuit,” the method is applicable to any kind of analog circuit, such as amplifiers, filters, oscillators, and modulators. For example, consider designing a single frequency oscillator for a specified frequency, quality factor, gain, noise control, port impedances, and so on. The task of the designer starts with design of the linear equivalent circuits for the oscillator; including the tank circuit, tuned amplifier, and the buffers. Certainly, the linear equivalent models are substituted for each and every nonlinear component in the circuit until the linear circuit is fully designed, simulated, and verified to meet the specs. Now it is time to do the biasing! As discussed earlier, this phase of the design is in two parts: (i) local biasing of the nonlinear components to meet the “critical” specifications, and (ii) using fixator-norator pairs to move

the scattered sources to those locations designated for the power supplies for the oscillator.

7. Conclusion

A new approach is presented for the biasing design of analog circuits. The main features of this approach are (i) circuit linearization for the design; (ii) individual component biasing; (iii) DC power reduction; (iv) full management of the design to meet the specifications. With specified operating points selected for the driving transistors and fixing them during the design process we can get the supplies needed for the biasing and at the locations designated by the designer. In this approach, the fixators (nullators plus sources) are used to keep the critical biasing values unchanged; whereas the norators are used to allocate the DC supplies, or adjust and modify their values if necessary. It is important to note that the use of fixator-norator pair in the present method is temporary; the pairs disappear after the actual supplies are substituted for the norators. Two design examples are worked out, which clearly demonstrate the power and simplicity of the methodology.

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References

- [1] R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design*, McGraw-Hill, New York, NY, USA, 3rd edition, 2008.
- [2] R. J. Baker, *CMOS, Circuit Design, Layout, and Simulation*, IEEE Press, Wiley Interscience, New York, NY, USA, 2nd edition, 2008.
- [3] C. J. Verhoeven, A. van Staveren, G. L. E. Monna, M. H. L. Kouwenhoven, and E. Yildiz, *Structured Electronic Design: Negative-Feedback Amplifiers*, Kluwer Academic Publishers, Dordrecht, The Netherlands, 2003.
- [4] R. Hashemian, "Analog circuit design with linearized DC biasing," in *Proceedings of IEEE International Conference on Electro Information Technology*, pp. 285–289, East Lansing, Mich, USA, May 2006.
- [5] R. Hashemian, "Designing analog circuits with reduced biasing power," in *Proceedings of the 13th IEEE International Conference on Electronics, Circuits, and Systems (ICECS '06)*, pp. 1069–1072, Nice, France, December 2006.
- [6] T. L. Pillage, R. A. Rohrer, and C. Visweswariah, *Electronic Circuit & System Simulation Methods*, McGraw-Hill, New York, NY, USA, 1995.
- [7] R. Kumar and R. Senani, "Bibliography on Nullor and their applications in circuit analysis, synthesis and design," in *Analog Integrated Circuit and Signal Processing*, Kluwer Academic Publishers, Dordrecht, The Netherlands, 2002.
- [8] H. Schmid, "Approximating the universal active element," *IEEE Transactions on Circuits and Systems II*, vol. 47, no. 11, pp. 1160–1169, 2000.
- [9] E. Tlelo-Cuautle, M. A. Duarte-Villaseñor, C. A. Reyes-García, et al., "Designing VFs by applying genetic algorithms from nullator-based descriptions," in *Proceedings of the European Conference on Circuit Theory and Design (ECCTD '07)*, pp. 555–558, Seville, Spain, August 2008.
- [10] E. Tlelo-Cuautle and L. A. Sarmiento-Reyes, "Biasing analog circuits using the nullor concept," in *Proceedings of the Southwest Symposium on Mixed-Signal Design (SSMSD '00)*, San Diego, California, USA, February 2000.
- [11] E. Tlelo-Cuautle, "An efficient biasing technique suitable for any kind of the four basic amplifiers designed at nullor level," in *Proceedings of IEEE International Symposium on Circuits and Systems*, vol. 3, pp. 535–538, Phoenix, Ariz, USA, May 2002.
- [12] D. G. Haigh, T. J. W. Clarke, and P. M. Radmore, "Symbolic framework for linear active circuits based on port equivalence using limit variables," *IEEE Transactions on Circuits and Systems I*, vol. 53, no. 9, pp. 2011–2024, 2006.
- [13] D. G. Haigh and P. M. Radmore, "Admittance matrix models for the nullor using limit variables and their application to circuit design," *IEEE Transactions on Circuits and Systems I*, vol. 53, no. 10, pp. 2214–2223, 2006.
- [14] D. G. Haigh, "A method of transformation from symbolic transfer function to active-RC circuit by admittance matrix expansion," *IEEE Transactions on Circuits and Systems I*, vol. 53, no. 12, pp. 2715–2728, 2006.
- [15] C. Beccari, *Transmission Zeros*, Dipartimento di Electronica, Turin Institute of Technology, Turino, Italy, 2001.
- [16] R. Hashemian, "Hybrid equivalent circuit, an alternative to thevenin and norton equivalents, its properties and applications," in *Proceedings of IEEE International Midwest Symposium on Circuits and Systems*, Cancun, Mexico, August 2009.
- [17] R. Hashemian, "Local biasing and the use of nullator-norator pairs in analog circuits designs," in *Proceedings of the Midwest Symposium on Circuits and Systems*, pp. 466–469, Knoxville, Tenn, USA, August 2008.