

Research Article

Design and Realization of GaAs Digital Circuit for Mixed Signal MMIC Implementation in AESA Applications

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A complete design flow starting from the technological process development up to the fabrication of digital circuits is presented. The aim of this work is to demonstrate the GaAs Enhancement/Depletion (E/D) double stop-etch technology implementation feasibility for digital applications, aimed at mixed signal circuit integration. On the basis of the characterization of small E/D devices with different Gate peripheries, developed by the SELEX-SI foundry, and the analysis of several GaAs-based logical families, the most suitable logic for the available technology has been selected. Then, simple test vehicles (level shifters, NOR logic gates and D Flip-Flops) have been designed, realized, and measured to validate the design strategy applied to the GaAs E/D process. These logical circuits are preliminary to the design of a more complex serial-to-parallel converter, to be implemented onto the same chip together with RF analog blocks, such as stepped attenuators and phase shifters.

1. Introduction

Today's high-performance radar systems, such as SAR and AESA systems, exploit complex antenna arrays to perform the beam forming and steering functions by means of electronic control. Such systems are involved in a large variety of applications, both civilian and military in nature, or in research activities of scientific interest such as remote sensing and Earth observation. Such radar systems typically need a huge number of active radiating elements, each equipped with a Transmit/Receive (T/R) module. First examples of T/R modules [1, 2] consist of multifunction chips performing RF signal low noise and high power amplification, operating mode selection by RF switches, together with phase and amplitude signal conditioning. The latter functionalities, analog in nature, are digitally controlled, and the trend is toward increasing the resolution and the precision of the signal conditioning, attained by increasing the number of phase-shifting or attenuating cells. Such requirement naturally implies the increase in the number of digital controls to be fed into the single T/R module: for a typical 6-bit control (amplitude and phase) and separate

architecture, the resulting number of bits is 13, leading to 26 digital lines (the required value and its opposite). Such high number of control lines for each module is typically generated by an on-board Silicon dedicated chip, wired to the GaAs analog functionalities and mounted/interconnected on an insulating substrate.

The need for reducing T/R modules' weight and size, led to the investigation for fully integrated implementation of T/R modules, or at least to minimize the number of different chips composing the module. The adoption of the so-called "Core Chip" approach, practically consists in grouping all the main T/R modules' control and low level amplification functionalities in a single GaAs chip, resulting in a major breakthrough in terms of easy integration, size, and assembly criticalities. The highest level of integration achieved in a Core Chip design is in the digital control circuits implementation within RF analog blocks, forming mixed signal MMICs [3–6]. However, due both to the lack of p-type FETs and a native stable GaAs oxide, complementary devices are not available in GaAs technology. For this reasons, in recent years BiCMOS SiGe technology was adopted to

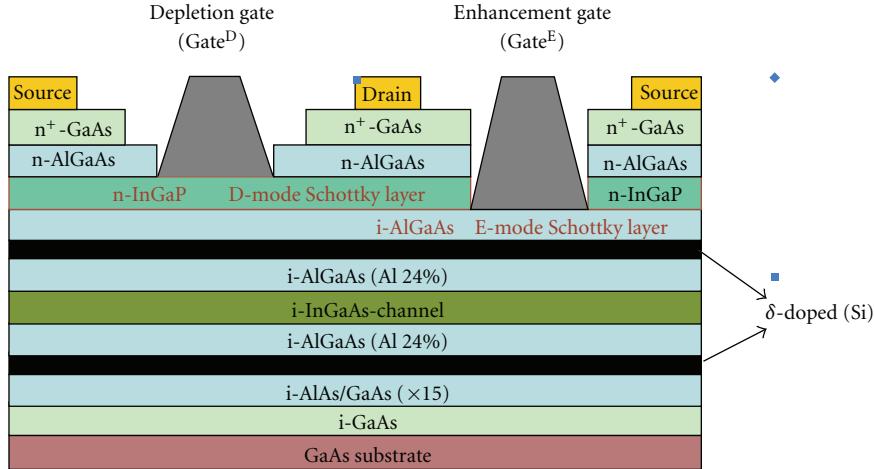
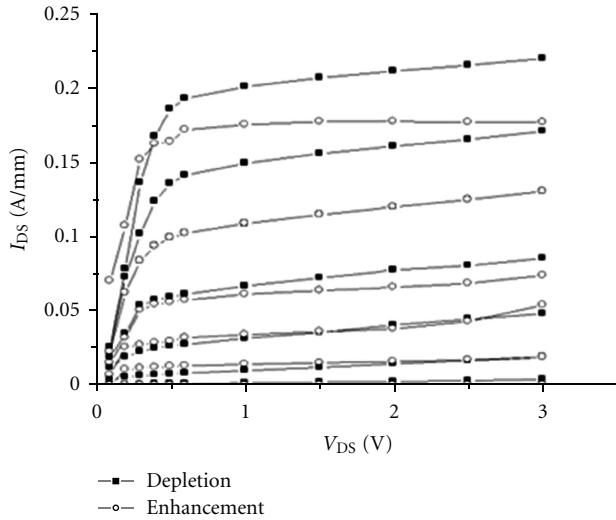


FIGURE 1: E/D substrate cross-sectional view.

FIGURE 2: Normalized output characteristics for Depletion (black symbols) and Enhancement (white symbols) devices for different gate voltages—Mag(V_{GS}) = 0, 0.1, ..., 0.6 V.

design fully integrated T/R module, due to the easy and quite immediate integration of both digital and analog circuits [7–10]. Nevertheless, GaAs-based Core Chips exhibit superior RF performance with respect to SiGe realizations, and Gallium Arsenide is a well-established and qualified process, being therefore still preferred to its SiGe counterpart for high-performance systems.

For GaAs mixed signal chip realization it is mandatory to have both Enhancement-mode and Depletion-mode devices available on the same substrate. For these reason, SELEX-SI foundry has developed a $0.4\text{ }\mu\text{m}$ GaAs E/D process based on double stop-etch epitaxial structure. On the basis of preliminary assessment of the technology and devices characterization, the more suitable logical family was selected and several basic digital functions (level shifters, NOR logic ports and D Flip-Flops) were designed, realized,

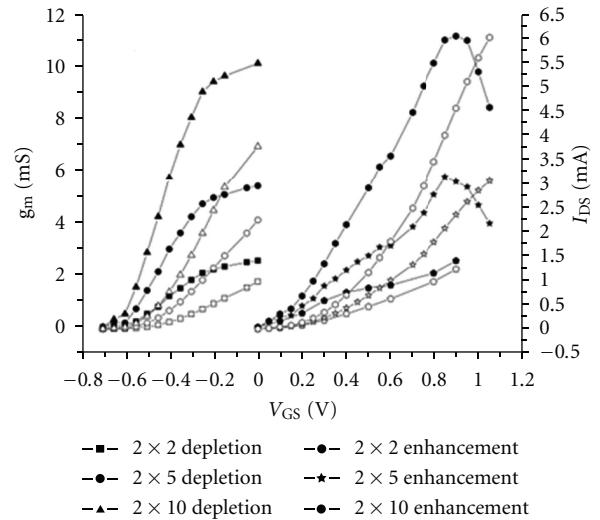


FIGURE 3: Transfer characteristics and transconductance for E/D devices with different gate widths.

and measured, demonstrating the implementation feasibility of digital control circuits on this GaAs process. All this circuits are aimed to form a more complex serial-to-parallel converter implementing the digital control section typically equipped on T/R modules.

The contribution is structured as follows: after the present introduction, in Section 2 a technological description of the E/D process will be given, while in Section 3 the results of the device characterization performed on the realized samples will be presented.

In Section 4 a description of the possible logic families to be adopted will be carried out, and in Section 5 the design of the single building blocks in the selected logic will be described. Section 6 is devoted to the measured results on the latter, while Section 7 is related to the further integration in a complete serial-to-parallel converter.

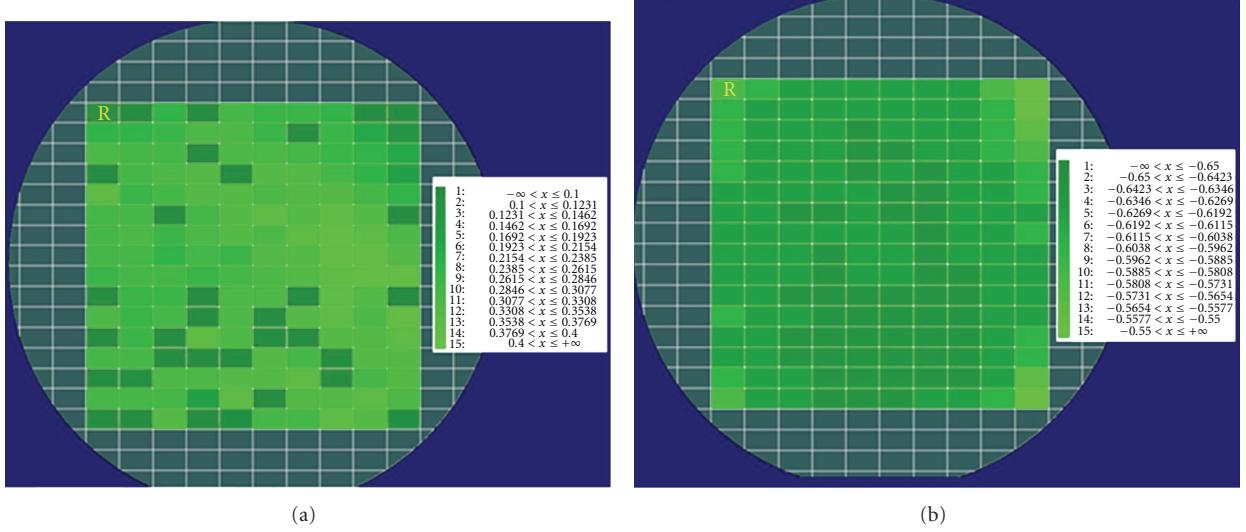


FIGURE 4: Pinch-off voltage water maps for E- and D-type devices.

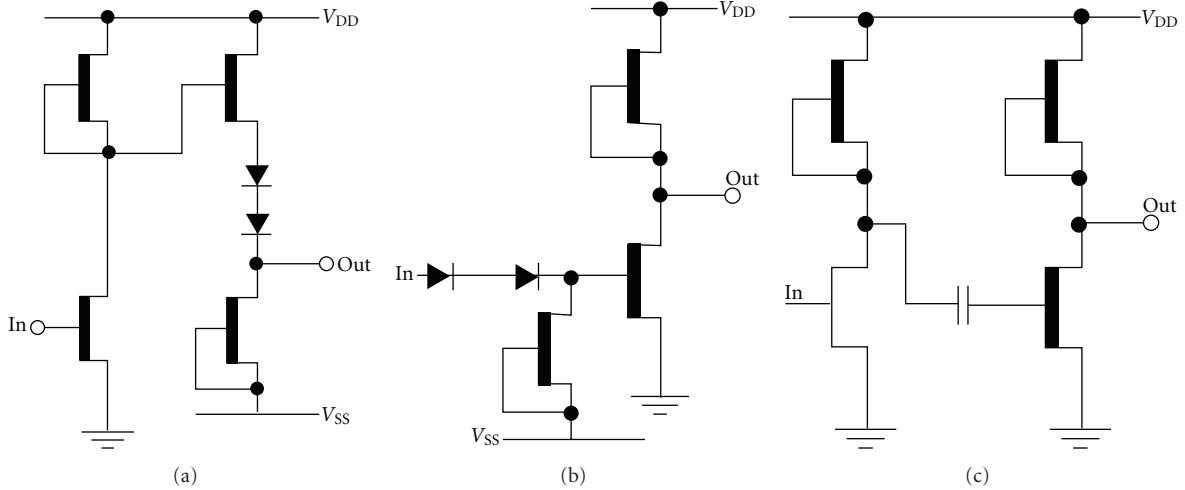


FIGURE 5: Depletion-based FET logic: (a) BFL; (b) SDFL; (c) CCFL.

2. Technology Description

Today's electronic systems requirements in terms of performances and large-scale industrial process yields, make Enhancement/Depletion technology very challenging. The uniformity of device's properties and performances is undoubtedly the most critical goal to be achieved since Enhancement- and Depletion-type devices operation is directly related to their own (specific) Gate Schottky junction. Under the substrate stack's point of view, a possibility to realize E/D device into the same wafer implies the introduction of two different semiconductor layers in order to realize two different Gate junctions. Bearing in mind those E/D technology peculiarities with the well-known performance sensitivity of pHEMT devices with respect to the epitaxial layer thickness, uniformity and defect density, it is mandatory that the etching processes have to be fully controlled. Moreover, it

is particularly important to minimize the complexity level of the technological process, with such requirement being strongly facilitated by a proper epitaxial structure selection.

In order to achieve the above-mentioned device properties, a double stop-etch epitaxial layer structure was engineered, schematically depicted in Figure 1.

The devices were fabricated on a heterostructure grown by molecular beam epitaxy (MBE) on a semi-insulating 4-inch GaAs substrate where a first n-InGaP etch stop layer is introduced to obtain Depletion-mode devices after well-controlled wet etching of n⁺-GaAs and n-AlGaAs layers. The Enhancement-Mode devices require a Gate contact closer to the channel, so that the 2-DEG is normally fully depleted. To realize onto the same substrate an Enhancement-mode pHEMT, an i-AlGaAs second etch stop layer has been set up, where the Gate contact is realized after selectively removing the n-InGaP layer. Subsequently, after the definition of the

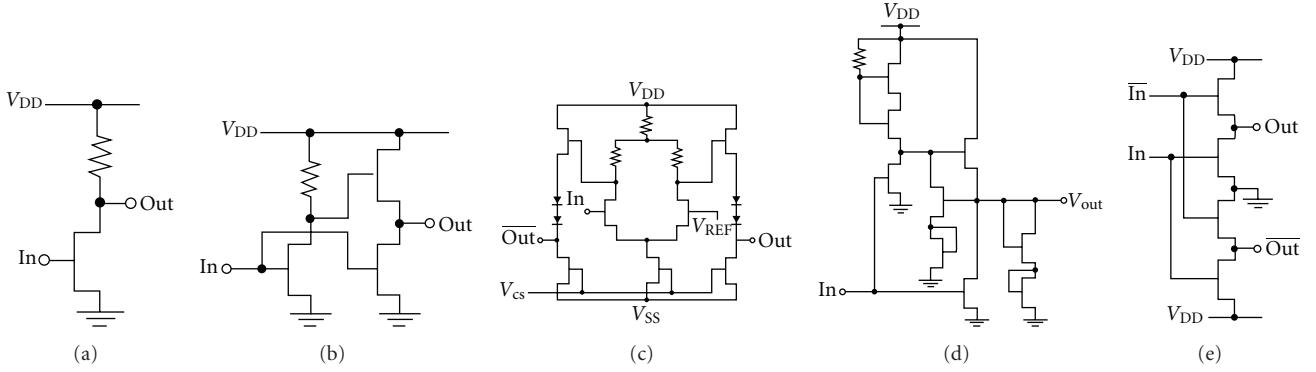


FIGURE 6: Enhancement-based FET logic: (a) DCFL; (b) BDCFL; (c) SCFL; (d) FFL; (e) PCFL.

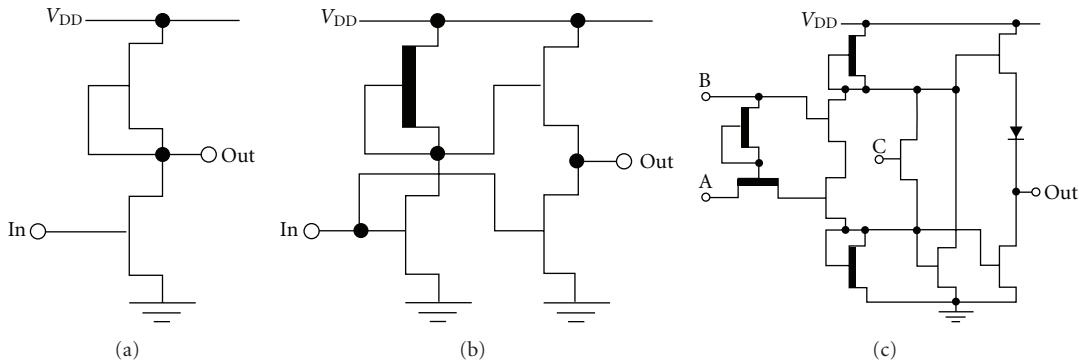


FIGURE 7: Enhancement-/Depletion-based FET logic: (a) DCFL; (b) SBFL; (c) F²L.

$0.4\mu\text{m}$ Gate contact by standard optical lithography, SiN has been removed by inductively-coupled plasma etch. Schottky junction contact metallizations are based on Ti/Al bilayer deposition. The heavily doped cap GaAs layer is utilized to form a low resistivity ohmic contact with the deposited Au/Ge/Ni trilayer, after a rapid thermal annealing step. Such contacts were processed simultaneously both for the E- and D-pHEMTs. The process further includes devices isolation that was achieved with proton implantation of the surface.

3. Devices Characterization

Enhancement- and Depletion-mode devices of different Gate peripheries and layouts were realized and characterized. Specifically, different devices in terms of access form were available, namely, coplanar and microstrip: the former was used to evaluate the transistor's analog performances, both DC and RF, while the latter have been measured with the primary focus on requirements of interest for digital applications.

The coplanar device type is composed by two Gate fingers with three Gate peripheries available, namely, $2 \times 2\mu\text{m}$, $2 \times 4\mu\text{m}$, and $2 \times 10\mu\text{m}$ while the other type is available with 1, 2, 4, 6, and 8 fingers with different width (from 2 up to $150\mu\text{m}$).

The device output characteristics normalized to the Gate periphery length of a typical $0.4\mu\text{m}$ gate length E- and D-pHEMT are shown in Figure 2.

Analyzing the output curves in Figure 2, a good and sharp pinch-off feature is evident for both D- and E-mode devices, evidencing a remarkable 2-DEG channel confinement. Drain current densities are comparable for the two device types, reaching 180 and 220 mA/mm for E- and D-mode devices, respectively. In the D-mode output characteristics a slightly nonsaturated behavior is noticeable, that can be ascribed to the i-AlGaAs leakage path.

Considering the D-mode characteristic for $V_{\text{gs}} = 0\text{V}$ (I_{dss0}), it must be a good compromise between the requirement to properly operate in digital circuits, requiring as low as possible currents, and proper RF operation where sufficiently high current levels are requested. Simultaneously, its value should be as close as possible to the E-mode maximum current (I_{max}): it is in this way possible to simplify the logic circuits topology by reducing the total gate periphery of E-mode devices. Moreover, to limit the logic gates current consumption and to prevent the accumulation of an offset voltage for devices adopting many gates in cascade, the E-mode I_{dss0} should be kept as close as possible to zero. The Drain-Source voltage at which saturated current occurs is nearly the same for both device types, reaching 0.6 V for normal devices, slightly increasing in the case of

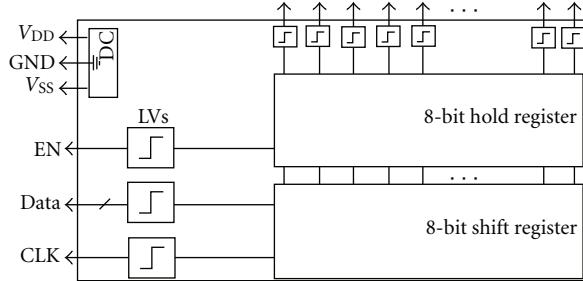


FIGURE 8: Functional block diagram of the digital control section.

smaller ($2\text{ }\mu\text{m}$) width devices. The measured specific ON-resistance was equal to 1.6 and $1.8\text{ }\Omega/\text{mm}$ for D- and E-mode pHEMTs, respectively. In the case of small (i.e., $2\text{ }\mu\text{m}$) width devices, where the parasitic resistance plays a major role in determining devices' active regions, the knee voltage increases to 0.8 V .

About Gate leakage current, a junction forward conduction for $V_{GS} \geq 0.8\text{ V}$ for E-mode devices can be observed, thus limiting device's performance and usability above that limit. As it can be noted from the above plot, no significant kink effect is observed in the fabricated devices. As presented in Figure 3, the measured device peak transconductance was 415 and 450 mS/mm for E- and D-mode, respectively. Slightly lower peak transconductance in E-mode pHEMT is probably due to lower channel thickness with a i-AlGaAs etching process inducing a reduced carrier mobility, even if the Gate capacitance is smaller than the D-mode counterpart. Different transconductance slope versus V_{GS} instead have to be linked to the presence of crystal defect at the i-AlGaAs surface as a consequence of chemical etching of InGaP stop layer for E-mode device realization, whose effect is a reduced Gate controlling capability for the E-mode device as compared to D-mode ones. Deeper analysis on this aspect will be carried out. Further analysis of Figure 3 evidences a well-marked difference between Enhancement and Depletion devices in terms of threshold voltages.

Microstrip devices were characterized and studied in terms of pinch-off voltages and output transfer characteristics. For proper operation of digital circuits, the more restrictive device feature is related to the Enhancement device pinch-off voltage which must be positive, E-mode device exhibiting zero current for $V_{GS} = 0$. Pinch-off voltage (defined as $I_{DS} = 1\text{ mA/mm}$ @ $V_{DS} = 1\text{ V}$) maps obtained for the E/D pHEMT process are presented in Figure 4. A mean value around $+0.1\text{ V}$ with an associated 75% on-water yield has been obtained for E-mode pHEMT, while for the D-mode pHEMT a mean value around -0.6 V and 90% on-water yield results.

Finally, on-water microwave S-parameter measurement on wider Gate periphery devices ($4 \times 50\text{ }\mu\text{m}$) has been performed by means of a vector network analyzer system. The cut-off frequency f_T has been extracted biasing at $V_{DS} = 2.5\text{ V}$ and V_{GS} selected for maximum transconductance, resulting in values higher than 30 and 35 GHz for the D-

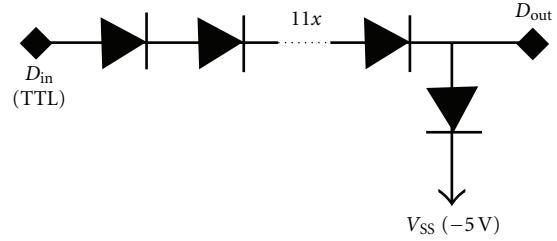


FIGURE 9: Input level shifters schematic circuit.

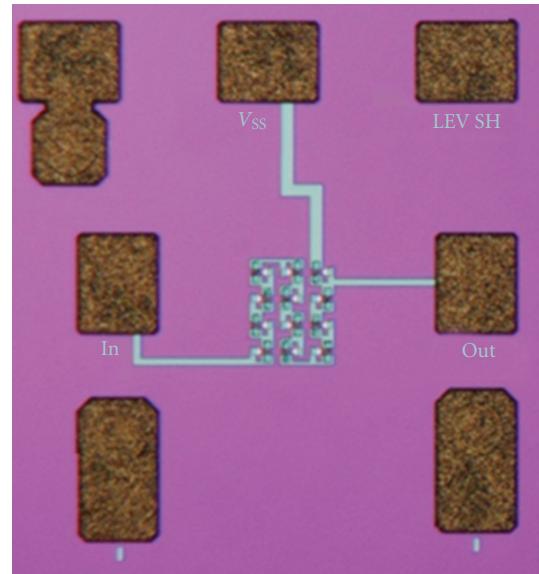


FIGURE 10: Microphotograph of the input level shifter test cell.

TABLE 1: Main E/D device properties.

	Depletion	Enhancement
$I_{D,\max}$ (mA/mm)	220	180
V_t (V)	-0.6	0.1
$g_{m,\max}$ (mS/mm)	450	415
f_T (GHz)	30	35
f_{\max} (GHz)	>40	>40
R_{ON} (Ω/mm)	1.6	1.8

and E-mode pHEMTs, respectively. The corresponding f_{\max} values are higher than 40 GHz in both cases.

The characterized E/D device/process's main properties are listed in Table 1.

4. Potential GaAs Logic Families

In order to allow the on-board implementation of the digital control interface in Core Chips, the digital control section chip area occupation should be minimized, and the digital control should require a low DC power consumption, being at the same time able to drive high capacitive loads (i.e., typically the devices' Gates of Attenuators, Phase Shifters

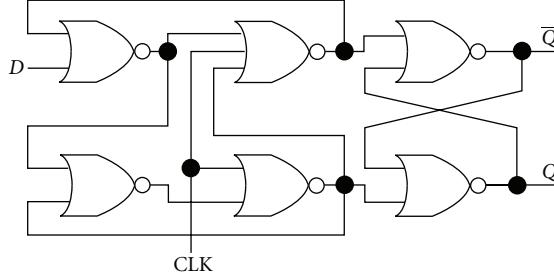
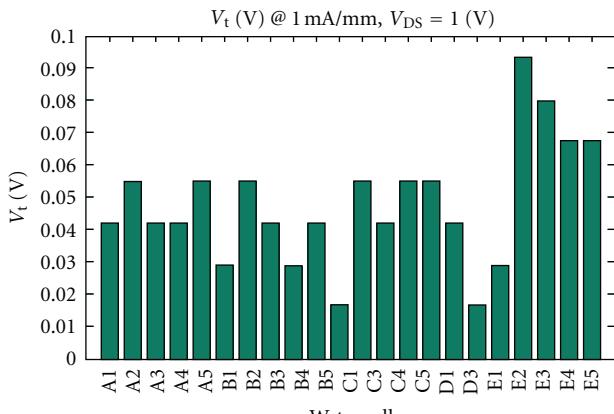
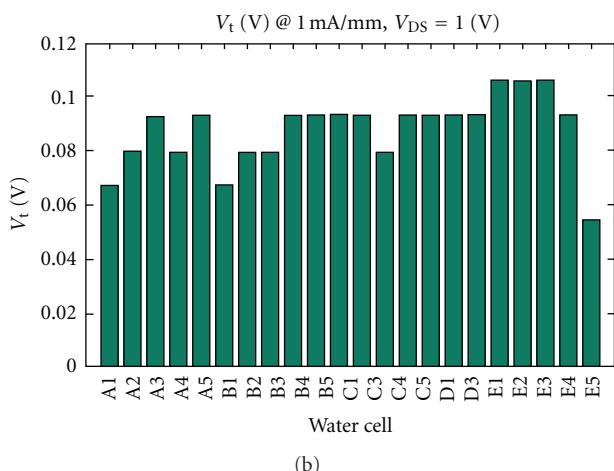


FIGURE 11: NOR-based D Flip-Flop architecture.



(a)



(b)

FIGURE 12: Threshold voltages variation along water surface for microstrip 1×2 and $1 \times 4\mu\text{m}$ D-type devices.

and Tx/Rx Switches). Finally, control circuitry response must be robust with respect to noise. Several logic families have been developed since the g70s and they have been considered and analyzed for the design of digital circuits on GaAs, as in the present contribution. Early logic families were based on a combination of diodes and normally ON devices (Depletion-mode FETs). Buffered FET Logic (BFL) [11], Schotkty Diodes FET Logic (SDFL) [12], and Capacitive-Coupled FET Logic (CCFL) [13] represent a few examples. These families however exhibit some drawbacks, such as

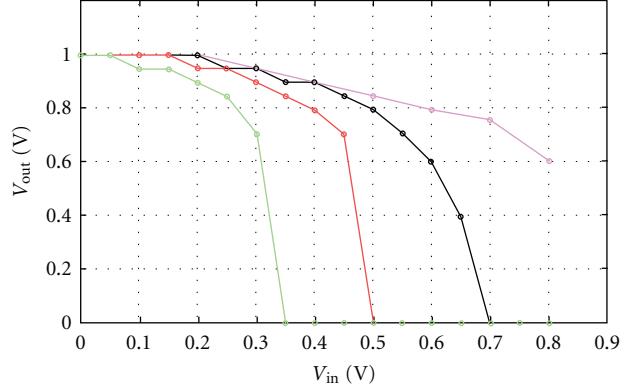


FIGURE 13: SBFL Inverter's voltage transfer function.

large area occupation and power consumption regarding the BFL, fan-out capability regarding the SDFL, and finally low operating frequency issues regarding the CCFL. Figure 5 shows the Inverter port implementation based on BFL (a), SDFL (b), and CCFL (c).

Along with the Enhancement-mode devices development, different logic families were proposed: Direct-Coupled and Buffered Direct-Coupled FET Logic (DCFL and BDCFL) [14], Source-Coupled FET Logic (SCFL) [15], Feedback FET Logic (FFL) [16], and Pseudo-Complementary FET Logic (PCFL) [17]. Enhancement-based DCFL and BDCFL exploit a load resistors to realize the inverter circuit, thus implying area occupation and power dissipation issues. The SCFL is based on a FET differential pair: even if it introduces some improvements with respect to high-speed operation, its complicated architecture and its large area occupation do not allow an easy integration in a mixed signal MMIC. Finally, the FFL needs a high number of devices to realize a simple inverter, while the PCFL is affected by signal degradation and noise margins issues. Inverters circuit schematic representation for each Enhancement-based logic family is reported in Figure 6.

The capability of providing normally ON and normally OFF devices on the same substrate leads to the E/D-based FET logic families. By replacing the load resistors with a normally ON load transistor, DCFL and BDCFL based on E/D devices can be implemented [14]. In [18, 19] the Super-Buffered FET Logic was introduced as a DCFL improvement exploiting an output buffer stage realized by Enhancement FETs. The SBFL exhibits better fan-out capability, better noise margins, and comparable rise and fall time with respect to its DCFL counterpart, against a slightly higher area occupation and DC power consumption. Another E/D-based logic family was successfully reported in [20], named FET-FET Logic (F²L), but it is characterized by a high number of transistors to implement a simple Inverter gate, and therefore it has not been taken into consideration for the digital control section design. In Figure 7 the Inverter circuit schematics for each E/D-based logic family are depicted.

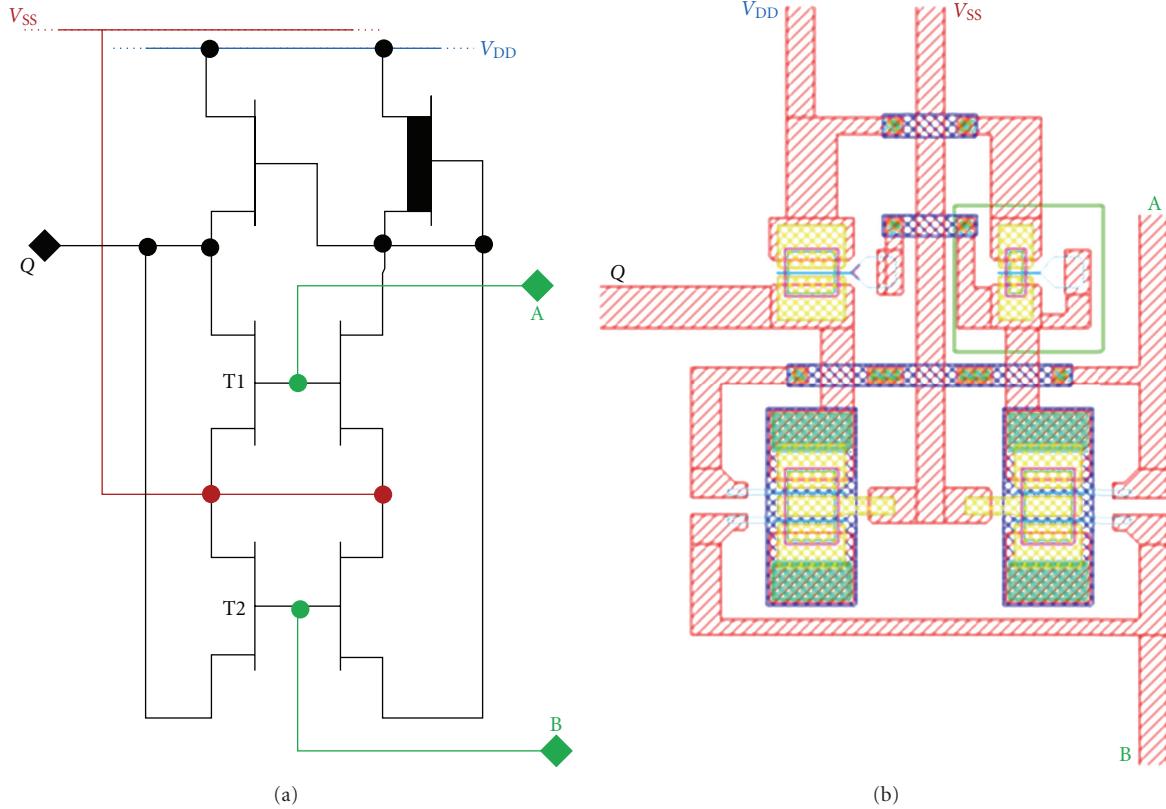


FIGURE 14: (a) 2-Input NOR port schematic; (b) optimized layout.

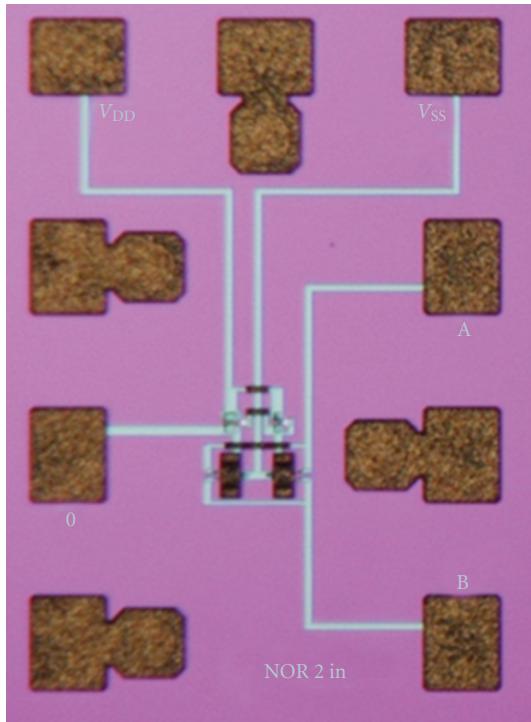


FIGURE 15: Microphotograph of the realized 2-Input NOR port test cell.

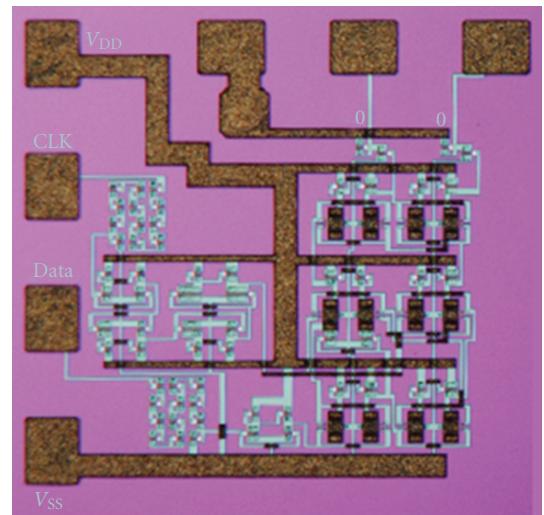


FIGURE 16: Microphotograph of the realized D-Flip Flop test cell.

On the basis of the analysis of the above GaAs logic families, a qualitative comparison among them, considering the Inverter gate design as a test vehicle, can be carried out as summarized in Table 2. In order to account for some relevant parameters such as the DC power consumption, area

TABLE 2: Comparison among GaAs logic families.

Logic family	Implemented devices	Minimum DC bias needed	Area per power (FoM)	Output buffer stage
BFL [11]	Depletion FETs diodes	2	48	NO
SDFL [12]	Depletion FETs diodes	2	33	NO
CCFL [13]	Depletion FETs diodes	1	21	YES
SCFL [15]	Enhancement FETs diodes	4	60	SI
FFL [16]	Enhancement FETs	1	38	YES
PCFL [17]	Enhancement FETs	1	12	NO
DCFL [18, 19]	E/D FETs	1	12	NO
SBFL [18, 19]	E/D FETs	1	20	YES
F ² L [20]	E/D FETs Diodes	1	50	YES

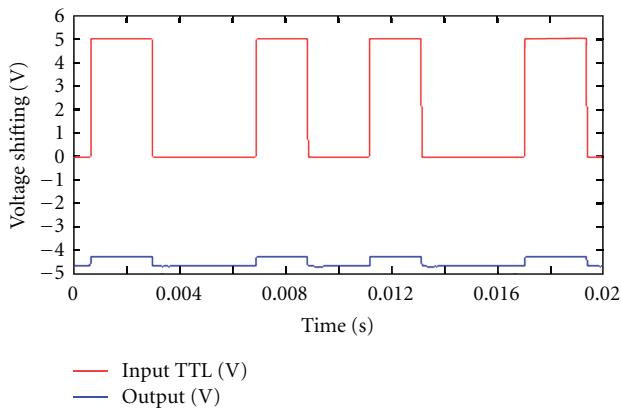


FIGURE 17: Measured results of the input level shifters' voltage transfer function (red line: input TTL; blue line: output).

occupation, and the load driving capability, in the Table are reported the following:

- (i) the minimum number of voltage supplies needed, related to the gate area occupation and DC lines routing criticalities;
- (ii) the output buffer stage implementation, concerning the gate fan-out capability, noise margins, and rise/fall times;
- (iii) the *area per power* product, that is, a qualitative figure of merit evaluating the gate size by the used devices number and the type, and the power consumption by the number of conductive paths between the voltage supply and the ground reference when two Inverters are cascaded and the input signal performs a low-high-low cycle.

As it can be noticed from the previous table, the DCFL represents the best trade-off selection in terms of power consumption and area occupation, together with PCFL. Both families, however, are affected by a low fan-out capability and low noise margins. As a consequence, the more suitable logic family for the SELEX-SI GaAs E/D process is the SBFL.

5. Test Vehicles Design and Realization

A functional block diagram of the digital control section is shown in Figure 8. Since the external TTL (0/5 V) logic level of the enable (EN), the serial data (DATA), and the clock (CLK) signals is not compatible with the internal logic levels (imposed by the normally OFF device's Gate-Source Schotkky junction), level shifters (LVs) at each input terminal are needed. Moreover, in order to correctly feed the Gates of the RF analog normally ON devices, the output terminals of the control section are equipped with LVs to translate the internal logic levels between 0 V and the Gate-Source pinch-off voltage. So, the control section's voltage bias must be accurately selected. In particular, the DC voltage rail is set to 1.2 V to minimize the DC power consumption and to guarantee the proper internal logic swing. V_{SS} is fixed to -5 V and consequently V_{DD} is set to -3.8 V.

5.1. Input Level Shifters Design. The input level shifters design is based on diodes in totem-pole configuration, as shown in Figure 9. Diodes are realized exploiting the $4\mu m$ E-FET's Gate-Source junction by short-circuiting Drain and Source contacts. The minimum number of diodes to be cascaded to guarantee suitable internal logic levels is $d = 12$. Each input level shifter operates between TTL voltage levels ($V_{TTL} = 0/5$ V) and V_{SS} .

The input level shifter's voltage transfers function is given by

$$V_{out,LV} = V_{SS} + \frac{V_{TTL} - V_{SS}}{d}. \quad (1)$$

So the computed internal "0" and "1" logic levels are $V_{out,LV0} = -4.58$ V and $V_{out,LV1} = -4.17$ V, respectively, with a 0.4 V voltage swing. Figure 10 shows a microphotograph of the realized input level shifter test cell. Circuit size without access pads is $126 \times 160 \mu m^2$.

5.2. 2-Input and 3-Input NOR Ports Design. The control section core consists in a 8-bit shift register, whose outputs are connected to the inputs of an 8-bit hold register. Each register consists in 8 D-Flip Flop memory cells designed with the NOR-based architecture. Figure 11 shows the circuit schematic of a D-Flip Flop, being D the data input and CLK the clock input (if the shift register is considered) or the enable input (if the hold register is considered).

On the basis of the previous analysis of GaAs logic families and from the technology assessment and devices characterization, the SBFL logic was chosen to design the 2-Inputs and 3-Inputs NOR ports. The SBFL logic is a "ratioed" logic: the logic swing depends on the ratio between the

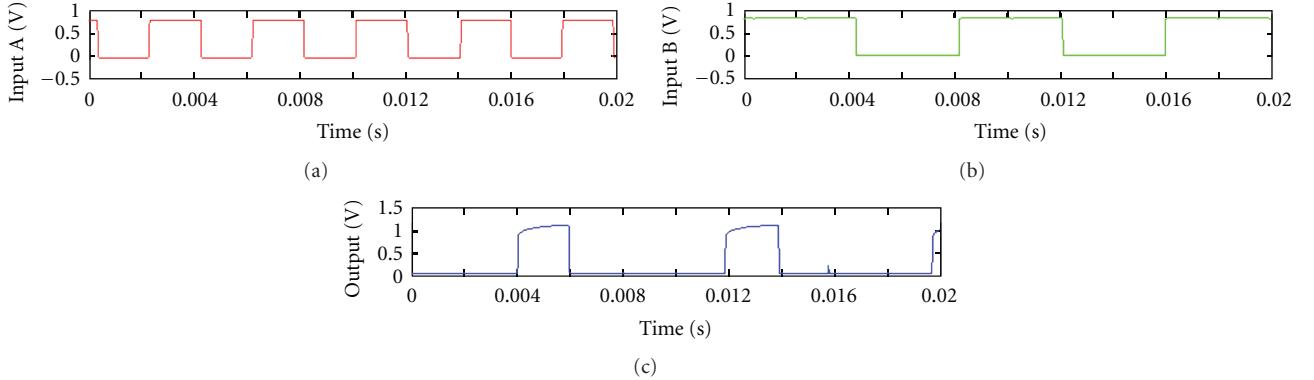


FIGURE 18: Measured results of the 2-input NOR port (red line: input A; green line: input B; blue line: Output).

pull down transistor's Gate periphery (W_E) and the load transistor's Gate periphery (W_D). The higher is the W_E/W_D ratio, the lower is the "0" logic level. However, it must be considered that power consumption and area occupation rise together with W_E/W_D ratio: it is therefore mandatory to find a suitable trade-off between logic swing, size, and consumption.

Analyzing experimental threshold voltages uniformity, it can be noticed that $1 \times 2 \mu\text{m}$ devices suffer poor stability making themselves unusable and leading to the choice of the smallest D-type device as the $1 \times 4 \mu\text{m}$ (Figure 12). The lack of uniformity showed in Figure 12 for the case of $1 \times 2 \mu\text{m}$ is probably due to leakage effect among device's Source and Drain regions.

Then, setting the load transistors to the minimum available Gate periphery ($W_D = 4 \mu\text{m}$), the voltage transfer function of an Inverter, with W_E as a parameter, is plotted in Figure 13. These curves were obtained by plotting the load transistor's I/V behavior measured at $V_{GS} = 0 \text{ V}$ on the switching transistor measured I/V characteristics. As it can be noted, the best value for the W_E/W_D ratio is 4, and then $W_E = 16 \mu\text{m}$.

In order to reduce the NOR area, single-gate-finger pHEMTs are replaced with multifinger devices configured so as the nearby gates are electrically disconnected by proper layout of the Gate metal [21]. Figure 14 reports the electrical circuit and the resulting layout of the 2-Input NOR architecture: the Gate metallization removal transforms a two-finger device into two single-finger devices sharing the same Drain and Source contacts, as required by the implementation (see devices T1 and T2 in Figure 14(a)). Similarly, the 3-Input NOR port has been designed. A 2-Input NOR port test cell has been realized and its microphotograph is reported in Figure 15. Port size without access pads is $170 \times 190 \mu\text{m}^2$.

5.3. Output Level Shifters Design. The output level shifters are DCFL-based Inverter operating between ground reference and V_{SS} . This solution is featured by small area occupation and the output level shifters can be easily integrated within the Hold Register's Flip-Flop cells.

5.4. Design of the D-Flip Flop with Interfaces. On the basis of the previous designs, a D-Flip Flop test cell equipped with the Input Level Shifters, the Output Level Shifters, and digital buffers has been realized as reported in Figure 16.

Digital buffers on the Clock and Data path are mandatory for the correct operation of the complete serial-to-parallel converter, so they have been implemented in the test cell in order to verify their operation. D-Flip Flop size without access pads and digital buffers is $460 \times 800 \mu\text{m}^2$, including the V_{DD} and V_{SS} DC lines.

6. Experimental Results

The measurement setup consists of an Agilent DSO6052A oscilloscope, an Agilent E3631A voltage source, a Cascade Microtech RF1 probe station, a National Instrument PXI-6259 mixed signal board to generate digital TTL and analog input signals, and controlled impedance cables terminated close to the loads. The mixed signal board is controlled via software in LabVIEW environment. The level shifter's measured results are reported in Figure 17. The level shifter's output voltage was obtained by applying an input random bit sequence in TTL logic (red line). The input signal period was set to 4 ms. The output voltage (blue line) is correctly translated to the internal logic levels. Measured levels are -4.7 V and -4.3 V for the logic "0" and the logic "1", respectively. These results are in good agreement with the computed translated levels, preserving a 0.4 V voltage swing.

The 2-Input NOR port was measured with a 1.2 V bias and the input signals logic levels were set to 0 V and 0.8 V: the measured results are depicted in Figure 18. To verify the NOR port's truth table, a square-wave sequence with 4 ms period was applied to input A (red line), while a square-wave sequence with 8 ms period was applied to input B (green line). As it can be noticed, the NOR port is properly operating.

The D-Flip Flop was measured setting the V_{DD} and V_{SS} biases to -3.8 V and -5 V , respectively, and applying TTL input signals to the Data and Clock terminals. In particular, Data signal is a random bit sequence with 8 ms period, and Clock signal is a square wave with 4 ms period. The measured results are presented in Figure 19. The input signal (red line)

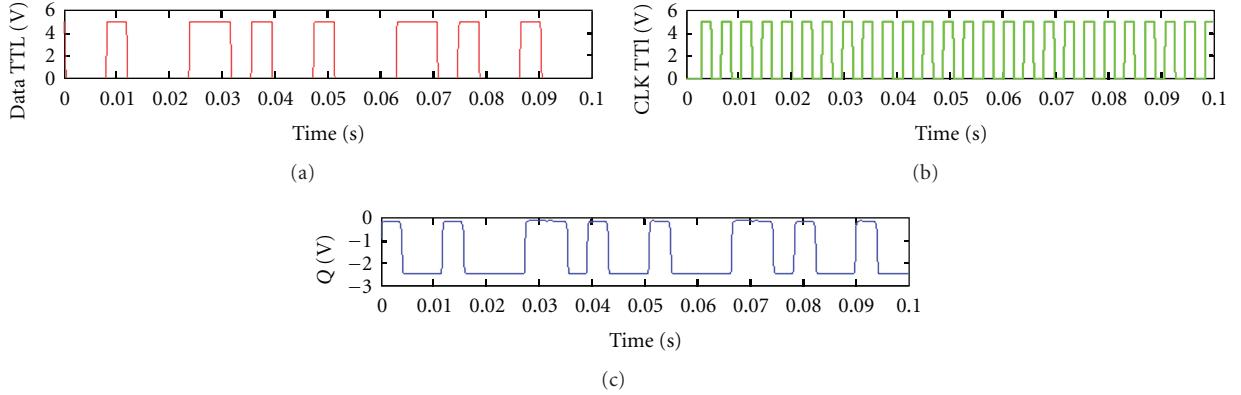


FIGURE 19: Measured results of the D-Flip Flop (red line: data input; green line: clock input; blue line: sampled output).

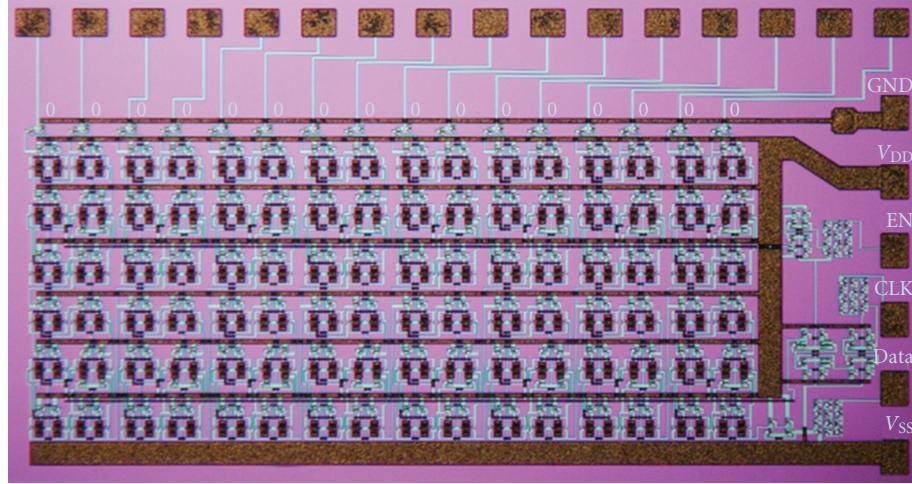


FIGURE 20: Microphotograph of the digital control section (serial-to-parallel converter).

is sampled by the clock (green line) and the test cell output (blue line) is a sampled copy of the input sequence, featuring different logic levels. In particular, the output voltage swing is between 0 V and -2.5 V, that correspond to the logic “1” and “0”, respectively. These voltage output guarantee the proper switching operation of the analog RF devices to be controlled.

7. Serial-to-Parallel Converter Realization

The microphotograph of the complete digital control section is reported in Figure 20. It consists in a 8-bit serial-to-parallel converter with TTL logic interface that provides complementary output voltages that are the RF analog devices' Gate voltages. Circuit size is 4.2×2.2 mm², including access pads. A modular architecture has been therefore adopted. This strategy allows for easy customization of the Core Chip digital part, according to the number of the required programmable functionalities, and thus of the length of the control data words.

8. Conclusions

An Enhancement/Depletion GaAs pHEMT devices integration was achieved by means of a simple and fully controlled double stop-etch epitaxial layer structure. Both E- and D-mode small periphery devices, down to $4\mu\text{m}$, exhibit uniform threshold voltage over a high water yield and comparable maximum Drain current and pinch-off capability.

According to the reported characterization, several GaAs logic families have been investigated in order to identify the suitable one for the reported E/D process, and therefore the SBFL logic family has been adopted. On the basis of this technological assessment, SBFL-based test vehicles have been designed and realized. Experimental results show promising performance of simple digital circuits such as NOR gates, level shifters, and D-Flip Flops. The designed test cells form a more complex serial-to-parallel converter devoted to drive RF Attenuator and Phase Shifter, analog in nature, that are digitally controlled, leading to a mixed signal circuit implementation in T/R module for AESA applications.

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