Research Article

A Zero-Voltage-Transition Interleaved Boost Converter and Its Application to PFC

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1. Introduction

Reduced power factor and polluted utility voltage have been rising due to the increase of nonlinear loads use by residential, commercial, and industrial customers. Nowadays international regulation governing the amount of harmonic current became mandatory.

Thus, the reduction of input current harmonics and high power factor operation is an important requirement for power supplies. The topology usually employed in power factor correction single-phase power supplies is composed by a front-end rectifier followed by a boost converter, as shown in Figure 1. In this topology, the boost converter in continuous conduction mode (CCM) with the average current control and pulse-width modulation (PWM) technique has been the most popular circuit [1–3].

High power density and fast transient response of this circuit can be achieved by increasing the switching frequency. However, the switching losses and electromagnetic interference noises will be occurred following increasing the switching frequency. In order to improve the efficiency of the power factor correction (PFC) circuit, many efforts have been done on the soft-switching converter [4–11]. Unfortunately, switching losses in the approaches proposed in [6, 7] can be reduced only at the expense of much increased current stresses of the main switch, which leads to a substantial increase in conduction loss.

To reduce the switching losses, initially raise the snubbers. Example of these snubbers can be found in the references [12, 13]. Later on appeared the quasi-resonant converters (QRCs) proposed in [14]. However, some of their characteristics such as load limitations and control difficulties due to variable frequency operation restrict the practical use of these converters. Quasi-resonant converters (PWM-QRC) [15] operate with fixed switching frequency; on the other hand they present all the other disadvantages of the QRC’s that limit their applications.

Nowadays there are many converters that do not present the limitations described above [16]. Although this converter presents several advantages, its main switch presents current and/or voltage stresses.

Most recent development in high-frequency converter configuration is a hybrid of resonant soft switching and pulse-width-modulation (PWM) control. This group of converters is called soft switching PWM converters, an example of these converters is presented in [17]. In the soft switching PWM converters, the switches operate in resonant mode only during switching transitions and then return to PWM operation for the rest of a switching period.
In [18] the soft-switching techniques allows operation with much reduced switching losses and stresses enabling high switching frequency operation with high efficiency.

The concept of interleaving several switching cells is not new and was originally used as a method for overcoming the limitations of ordinary power conversion techniques and device technologies [19]. Recognition of the general merits of interleaved conversion has prompted a diverse variety of subsequent investigations, as reflected in the literature.

In this paper, the interleaved power conversion refers to the strategic interconnection of two switching cells for which the conversion frequency is identical, but for which the internal switching instants are sequentially phased over equal fractions of a switching period. This arrangement applied to PFC combined with the soft switching technique to lower the switching losses in the approach proposed in [18] can reduce the net ripple amplitude and raises the effective ripple frequency of the overall converter without increasing switching losses or main switches stresses.

The main goal of this system can therefore realize savings in filtration and energy storage requirements, resulting in greatly improved power conversion densities without sacrificing efficiency.

The features of the proposed converter are discussed in this paper, and the principle of operation, simulation, and experimental results is presented to validate the proposed solution.

2. Proposed Structure

A configuration of the proposed structure is shown in Figure 2. This converter is based on the interleaved boost converter, integrated with the proposed soft switching auxiliary circuit.

2.1. Circuit Description. As the proposed structure is derived from the boost converter, there is one input inductor \((L_{F1} \text{ and } L_{F2})\) for each stage connected in parallel. The input current ripple is reduced by the parallel stages operating with different phases. The diodes \(D_{A1}\) and \(D_{A2}\) are the output diodes and operate like the output diodes of the interleaved boost converter. The output filter and load are represented by \(C_o\) and \(R_o\).

In order to simplify the description and the explanation of the principle of operation of the proposed converter, filter inductance’s \(L_{F1}\) and \(L_{F2}\) are assumed large enough to be considered as ideal current sources. The voltage across \(C_o\) presents no ripple, all components are treated as being ideal, and the input current flows through freewheeling diodes \(D_{A1}\) and \(D_{A2}\) until switch \(S_{A1}\) or \(S_{A2}\) is turned on at time \(t_o\). According to its working cycle, operations modes are described as follows.

2.2. Principle of Operation. The operation of the circuit will be described considering the branch 1 \((S_{A1} \text{ and } S_1)\), since the branch 2 \((S_{A2} \text{ and } S_2)\) operates in the same way. Under the assumption that the switching frequency \((100 \text{ kHz})\) is much higher than the rectifier output frequency \((120 \text{ Hz})\), the voltage \(V_i\) will not have a significant change. In this case the development of the analysis will consider a DC input voltage, since the soft-switching strategy is not compromised by the incoming AC line. Based on these assumptions, circuit operations in one switching cycle can be divided into seven stages. The seven dynamic equivalent circuits of the new boost converter during one switching period are shown in Figure 3 where the main switch \(S_1\) starts conducting at \(t = t_2\) and turns off at the time interval \(t_6\), and the auxiliary switch \(S_{A1}\) starts at \(t = t_6\) and turns off at time interval \(t_3\). The ideal relevant waveform of the new interleaved boost is shown in Figure 4.

In this section, the analytical expressions describing the operation of the proposed converter are presented. The following definitions are assumed:

\[
\alpha = \frac{I_{F1}}{V_i} \sqrt{\frac{L_R}{C_R}},
\]

\[
\omega_R(t) = \frac{1}{\sqrt{L_RC_R}},
\]

\[
Z_o = \frac{L_R}{C_R}.
\]

The resonant components are assumed to be with the same values: \(L_{R1} = L_{R2} = L_R\) and \(C_{R1} = C_{R2} = C_R\).

Stage 1 \((t_0, t_1)\), Figure 3(a). Before \(t = t_0\), the main switch \(S_1\) maintains turn-off state, the input current \(I_{F1}\) flows through \(D_{A1}, L_{F1}, C_F\), and \(R_o\). This stage begins when \(S_{A1}\)
Figure 3: Topology modes.
turns on with ZCS at \( t = t_0 \). The resonant inductor \( \text{IL}_R \) charges linearly due to output voltage \( V_o \) from zero to \( \text{IL}_F \). The stage ends when the resonant current reaches \( \text{IL}_F \) and diode \( D_{A1} \) turns off with ZVS at \( t = t_1 \). The resonant current \( i_{LR}(t) \) and voltage \( v_{CR}(t) \) can be, respectively, described as:

\[
i_{LR}(t) = \frac{V_o}{L_R} t, \quad i_{LR}(t) = 0, \quad \Delta t_1 = \frac{\alpha}{\omega R} t.
\]

Stage 2 ([\( t_1, t_2 \), Figure 3(b)]. In this stage, the current \( \text{IL}_F \) remains flowing through auxiliary switch \( S_{A1} \). The remaining semiconductors are in the off state. The resonant current \( i_{LR}(t) \) and voltage \( v_{CR}(t) \) can be, respectively, described as:

\[
i_{LR}(t) = \text{IL}_F, \quad v_{CR}(t) = 0, \quad \Delta t_2 = t_2 - t_1.
\]

In this time interval main switch \( S_1 \) is turned on in a ZCS and ZVS way.

Stage 3 ([\( t_2, t_3 \), Figure 3(c)]. In this stage, the resonance begins when \( S_{A1} \) turns off with ZVS at \( t = t_2 \). The resonant route proceeds by way of \( \text{IL}_R, C_R \), and \( D_{R1} \). The resonant current \( i_{LR}(t) \) decreases, and the resonant voltage \( v_{CR}(t) \) also decreases via the resonance of \( \text{IL}_R \) and \( C_R \). This state ends when the voltage \( v_{CR}(t) \) reaches output voltage \( V_o \) at \( t = t_3 \). The resonant current \( i_{LR}(t) \) and voltage \( v_{CR}(t) \) can be, respectively, described as:

\[
i_{LR}(t) = \text{IL}_F \cos(\omega R t), \quad v_{CR}(t) = Z_o \text{IL}_F \sin(\omega R t), \quad \Delta t_3 = \frac{1}{\omega R} \arcsin\left(\frac{1}{\alpha}\right).
\]
Stage 4 ([t_3, t_4], Figure 3(d)). In this mode \(i_{LR}(t)\) reduces to zero. This mode comes to an end at \(t_4\) when \(i_{LR}(t)\) becomes zero. The expressions for \(i_{LR}(t)\) and \(v_{CR}(t)\) are

\[
i_{LR}(t) = -\frac{V_o}{L_R} t + \frac{I_{LF1}}{\alpha} \sqrt{\alpha^2 - 1},
\]

\[
v_{CR}(t) = V_o,
\]

\[
\Delta t_4 = \frac{\sqrt{\alpha^2 - 1}}{\omega_R}.
\]

Stage 5 ([t_4, t_5], Figure 3(e)). The main switch is conducting, and the input current flows through the input inductor and power switch. All diodes are blocked, and the input inductor store energy. The equations that describe this mode are

\[
i_{LR}(t) = \alpha \sqrt{\alpha^2 - 1},
\]

\[
v_{CR}(t) = V_o - \frac{I_{LF1}}{C_F} t,
\]

\[
\Delta t_5 = t_5 - t_4.
\]

Stage 6 ([t_5, t_6], Figure 3(f)). At the instant \(t_5\), switch \(S_1\) is turned off in a ZVS way, and the energy stored in the input inductor \(L_{F1}\) is transferred to the output capacitor \(C_F\) through the diode \(D_{S1}\) and also to the resonant capacitor \(C_{R1}\). In this time interval, \(C_{R1}\) linearly discharges to zero voltage. The resonant \(i_{LR}(t)\) and \(v_{CR}(t)\) can be, respectively, described as

\[
i_{LR}(t) = 0,
\]

\[
v_{CR}(t) = V_o - \frac{I_{LF1}}{C_F} t,
\]

\[
\Delta t_6 = \frac{1}{\alpha \omega_R}.
\]

Stage 7 ([t_6, t_7], Figure 3(g)). In this stage, diode \(D_{A1}\) conduces the \(L_{F1}\) current. The duration of this stage is defined by switch modulation. At the end of this time interval, switch \(S_{A1}\) turns on, and the next operating cycle begins. The resonant \(i_{LR}(t)\) and \(v_{CR}(t)\) can be, respectively, described as

\[
i_{LR}(t) = 0,
\]

\[
v_{CR}(t) = 0,
\]

\[
\Delta t_7 = t_7 - t_6.
\]

The State-space phase of the converter can be represented by a diagram shown in Figure 5. It is only valid for \(\alpha > 1\), physically, for low values of load current, the energy stored in resonant inductor would not be sufficient to charge
resonant capacitor to output voltage, which makes converter to perform as a hard-switched system.

The static gain, which represents the ratio between the output and the input voltages as function of the duty cycle, can be obtained by analyzing the waveforms of the inductor \( L_{F1} \) and observing the time intervals

\[
t_{0, t_1} : v_{LF1} = -(V_o - V_i),
\]
\[
t_{1, t_5} : v_{LF1} = V_i,
\]
\[
t_{5, t_6} : v_{LF1} = V_i - \frac{I_{LF1}}{C_R} t,
\]
\[
t_{6, t_7} : v_{LF1} = -(V_o - V_i).
\]

After the mathematical analyses, the expression of the static gain can be obtained

\[
G = \frac{V_o}{V_i} = \frac{1}{1 - D - (1/T_s \omega_R)(-\alpha + (1/2\alpha))},
\]

where: \( T_s \) is switching period and \( D \) is duty cycle.

The expression of the static gain is illustrated in Figure 6.

3. Results and Discussion

The benefits of interleaving can be understood intuitively using a simple graphical analysis to show how the output power is shared between two boost switching cells connected in parallel.

For simultaneous synchronous operation (wherein the commutation instances of the two controlled switches are identical), the circuit performance is equivalent to a single boost converter with equal total energy storage and equal total semiconductor die area. The inductor and diode ripple current waveforms that result are shown in Figure 7 as solid ones.

If these same converter cells are interleaved, such that the commutation instances of the second switch are delayed relative to those of the first switch by half a switching period, the resultant ripple waveforms are those shown as dashed lines in Figure 7. Compared to the noninterleaved case with equal energy storage, the interleaved ripple waveforms have smaller amplitudes and increased frequencies, reducing the filtration requirements.

The rectifier is designed to operate in continuous-conduction mode (CCM). It was employed UC3854 as the
controller, which prescribes the shape and the frequency of the input current due to its inherently synchronous feedback loop. The synchronous signal is sensed from a rectified sinusoidal waveform. This signal is accessible at the output of the rectifier in the usual PFC boost converter [20]. Thus, a signal bridge rectifier is necessary to obtain the desired synchronous signal and the rms input voltage for the control IC. Hall effect sensor for detecting the input current is installed for the average current mode control. The reference current is then generated by a multiplier/divider combination of the synchronous feedback loop, output voltage feedback loop, and input voltage feed-forward loop. As the input voltage changes, which is the case in this PFC application, reference current monitors the input current in order to obtain almost unity power factor. Figure 8 shows the principle of the average current mode, used as a control reference in this project.

The simplified scheme of the controller and the power stage are shown in Figure 9.

The block diagram circuit to drive the four switches using the UC3854 PWM output (GTDrv Pin) is shown in Figure 10.

3.1. Simulation Results. The proposed converter was simulated using commercially available PSIM software. The main circuit components were \( L_{R1} = L_{R2} = 300 \mu \text{H} \), \( C_F = 680 \mu \text{F} \). The resonant components were \( L_{R1} = L_{R2} = 5 \mu \text{H} \) and \( C_{R1} = C_{R2} = 3.9 \text{nF} \). Figure 10 shows simulated waveforms obtained with the converter operating with input voltage \( V_i = 50 \text{V} \), duty cycle \( D = 0.25 \), output load \( R_o = 10 \Omega \), and switching frequency \( f_s = 100 \text{kHz} \).

It can be seen from Figures 11(a) and 11(b) that the converter switches can operate with soft switching. The auxiliary switch, during the turn-on period, operates with ZCS as the resonant components delay the rise in switch current and makes it fall to zero voltage during the turn-off period. It should be noted that the voltage across the main switch is zero during the turn-on and turn-off periods, which is characteristic of this soft-switched converter.

Figure 11(c) shows the resonant voltage and current waveforms. It should also be noted that switches voltage and current stresses are equivalent to conventional hard-switched interleaved converter.

3.2. Experimental Results. A prototype circuit was constructed to verify the waveforms predicted above. The values
of the components used experimentally are the same as those specified in the simulation. The used switches were the MOSFET IRF840, and the diodes were HFA15TB60.

The specifications considered for implementation and test of the proposed converter are

- input voltage: $V_i = 127$ V rms,
- output voltage: $V_o = 200$ V,
- output power: $P_o = 0.8$ kW,
- switching frequency: $f_s = 100$ kHz.

The experimental waveforms obtained in laboratory are shown from Figures 12(a)–12(c) and were acquired using a THS720 Tektronix oscilloscope and a Tm 502A Tektronix current gauge.

Figure 12(a) shows the main switch voltage and current waveforms. As it is observed, this switch operates under zero voltage and current during the turn-on period and zero voltage during the turn-off period.

Figure 12(b) shows the waveforms of voltage and current in the auxiliary switch. As seen in this photograph, it operates with ZCS during the turn-on period and ZVS during the turn-off period.

Figure 12(c) shows the input voltage and current waveforms. This result shows that the obtained power factor is suitable for international standards.

The discrepancy between theoretical and practical values is due to parasitic oscillations, which were not considered in the data acquisition.
The nominal power factor exceeds 0.98, and the efficiency of the power circuit reached at nominal load is equal to 96%, as shown in Figure 13.

These values were obtained using a Yokogawa WT230 Digital Power Meter. To provide a comparative analysis about the efficiency levels achieved with the laboratory prototype, a converter without the proposed soft-commutation cell was also built in the laboratory using the same layout and the same components. Thus, in this situation, one can conclude that significant efficiency improvements can be achieved with the application of the proposed soft commutation cell, as depicted in Figure 13.

4. Conclusion

In this paper an improved ZVT interleaved boost PFC converter is presented. An auxiliary circuit for interleaved boost PFC converter is analyzed. The proposed topology was simulated via PSIM software, and an experimental prototype was implemented. As seen from the results, the main switches are turned on and turned off under ZVS conditions. Also, the auxiliary switch and the other diodes used in the auxiliary circuit are turned on and/or off with ZVS and/or ZCS conditions.

The simulation and experimental results show that the total switching losses of the interleaved topology are reduced by applying the proposed auxiliary circuit. It can be also seen that the power factor correction is achieved.

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References


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