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Research Article

Performance Analysis of High Speed Hybrid CMOS Full Adder Circuits for Low Voltage VLSI Design

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This paper presents a comparative study of high-speed and low-voltage full adder circuits. Our approach is based on hybrid design full adder circuits combined in a single unit. A high performance adder cell using an XOR-XNOR (3T) design style is discussed. This paper also discusses a high-speed conventional full adder design combined with MOSCAP Majority function circuit in one unit to implement a hybrid full adder circuit. Moreover, it presents low-power Majority-function-based 1-bit full addersthat use MOS capacitors (MOSCAP) in its structure. This technique helps in reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. Simulation results illustrate the superiority of the designed adder circuits over the conventional CMOS, TG, and hybrid adder circuits in terms of power, delay, power delay product (PDP), and energy delay product (EDP). Postlayout simulation results illustrate the superiority of the newly designed majority adder circuits against the reported conventional adder circuits. The design is implemented on UMC 0.18 μm process models in Cadence Virtuoso Schematic Composer at 1.8 V single-ended supply voltage, and simulations are carried out on Spectre S.

1. Introduction

It is time we explore the well-engineered deep submicron CMOS technologies to address the challenging criteria of these emerging low-power and high-speed communication digital signal processing chips. The performance of many applications as digital signal processing depends upon the performance of the arithmetic circuits to execute complex algorithms such as convolution, correlation, and digital filtering. Fast arithmetic computation cells including adders and multipliers are the most frequently and widely used circuits in very-large-scale integration (VLSI) systems. The semiconductor industry has witnessed an explosive growth of integration of sophisticated multimedia-based applications into mobile electronics gadgetry since the last decade. However, the critical concern in this arena is to reduce the increase in power consumption beyond a certain range of operating frequency. Moreover, with the explosive growth, the demand, and the popularity of portable electronic products, the designers are driven to strive for smaller silicon area, higher speed, longer battery life, and enhanced reliability. The XOR-XNOR circuits are basic building blocks in various circuits especially arithmetic circuits (adders & multipliers), compressors, comparators, parity checkers, code converters, error-detecting or error-correcting codes and phase detector.

Adder is the core element of complex arithmetic circuits like addition, multiplication, division, exponentiation, and so forth. There are standard implementations with various logic styles that have been used in the past to design full-adder cells [1–4] and the same are used for comparison in this paper. Although they all have similar function, the way of producing the intermediate nodes and the transistor count is varied. Different logic styles tend to favor one performance aspect at the expense of the others. The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. The circuit *delay* is determined by the number of inversion levels, the number of transistors in series, transistor sizes (i.e., channel widths), and the intracell wiring capacitances. Circuit *size* depends upon the number of transistors, their

sizes and on the wiring complexity. Some of them use one logic style for the whole full adder while the other use more than one logic style for their implementation.

Power is one of the vital resources, hence the designers try to save it while designing a system. Power dissipation depends upon the switching activity, node capacitances (made up of gate, diffusion, and wire capacitances), and control circuit size. At the device level, reducing the supply voltage V_{DD} and reducing the threshold voltage accordingly would reduce the power consumption. Scaling the supply voltage appears to be the well-known means to reduce power consumption. However, lower-supply voltage increases circuit delay and degrades the drivability of the cells designed with a certain logic style. One of the most significant obstacle in decreasing the supply voltage is the large transistor count and V_{th} loss problem. By selecting proper (W/L) ratio we can minimize the power dissipation without decreasing the supply voltage.

To summarize, some of the performance criteria are considered in the design and evaluation of adder cells and some are utilized for the ease of design, robustness, silicon area, delay, and power consumption. The paper is organized section wise. Section 2 describes the review of full adder circuit topologies. Section 3 illustrates the concept of SUM function-based hybrid full adders topologies and highlights some 1-bit adder cells, which is based on XOR-XNOR (3T) circuits. A review of Majority function, MOS capacitor characteristics, and three-input and five-input Majority function (MOSCAPs) based full adder topologies has been discussed in Section 4. In Section 5, implementations of Hybrid XOR-XNOR (3T) and Majority-function-based full adder methodologies are discussed. The simulation results are analyzed and compared in Section 6. Finally, Section 7 concludes the paper.

2. Review of Full Adder Topologies

In recent years, several variants of different logic styles have been proposed to implement 1-bit adder cells [5–28]. There are two types of full adders in case of logic structure. One is static and the other is dynamic style. Static full adders are commonly more reliable, simpler and are lower power consuming than dynamic ones. Dynamic is an alternative logic style to design a logic function. It has some advantages over the static mode such as faster switching speeds, no static power consumption, nonratioed logic, full swing voltage levels, and lesser number of transistors. An N input logic function requires N+2 transistors versus 2N transistors in the standard CMOS logic. The area advantage comes from the fact that the pMOS network of a dynamic CMOS gate consists of only one transistor. This also results in a reduction in the capacitive load at the output node, which is the basis for the delay advantage. There are various issues related to the full adder like power consumption, performance, area, noise immunity, regularity and good driving ability. Many researchers have combined these two structures and have proposed hybrid dynamic-static full adders. They have investigated different approaches realizing adders using CMOS technology each having its own pros and cons.

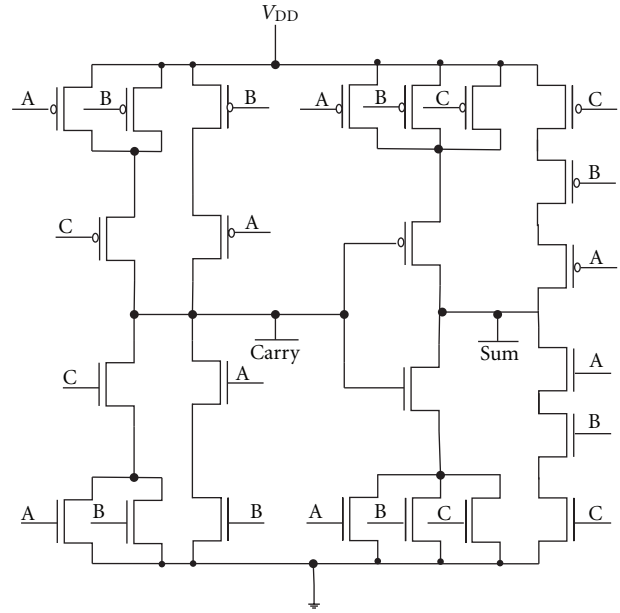


Figure 1: C-CMOS adder cell.

Full adder circuits can be divided into two groups on the basis of output. The first group of full adders have full swing output. C-CMOS, CPL, TGA, TFA, Hybrid, 14T, and 16T belong to the first group [5–20, 29–31]. The second group comprises of full adders (10T, 9T and 8T) without full swing outputs [21–28]. These full adders usually have low number of transistors- (3T-) based XOR-XNOR circuit, less power consumption, and less area occupation. The nonfull swing full adders are useful in building up larger circuits as multiple bit input adder and multipliers. One such application is the Manchester Carry-Look Ahead chain. The full adders of first group have good driving ability, high number of transistors, large area, and usually higher power consumption in comparison to the second group.

There are standard implementations for the full-adder cells which are used as the basis of comparison in this paper. Some of the standard implementations are as follows.

CMOS logic styles have been used to implement the low-power 1-bit adder cells. In general, they can be broadly divided into two major categories: the Complementary CMOS and the Pass-Transistor logic circuits. The complementary CMOS (C-CMOS) full adder (Figure 1) is based on the regular CMOS structure [3, 4, 29]. The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing, which are essential to provide reliable operation at low voltage with arbitrary transistor sizes.

The pass-transistor logic (PTL) is a better way to implement circuits designed for low power applications. The low power pass-transistor logic and its design analysis procedures were reported in [12, 13]. Its advantage is that one pass-transistor network (either pMOS or nMOS) is sufficient to implement the logic function, which results in lower number of transistors and smaller input load. Moreover, direct V_{DD}-to-ground paths, which may lead to short-circuit energy dissipation, are eliminated.

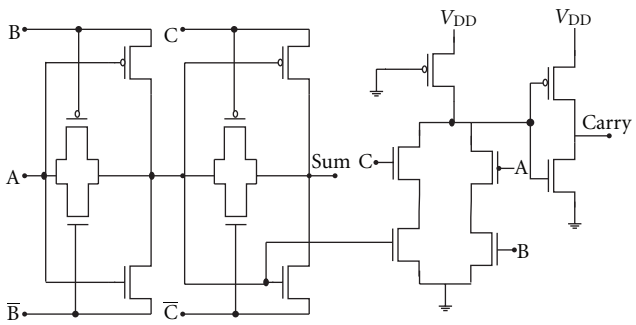


Figure 2: TG-Pseudo adder cell.

Pseudo nMOS full adder cell operates on pseudo logic, which is referred to as ratioed style. This full adder cell uses 14 transistors to realize the negative addition function. The advantage of pseudo nMOS adder cell is its higher speed (compared to conventional full adder) and less transistor count. The disadvantage of pseudo nMOS cell is the static power consumption of the pull-up transistor as well as the reduced output voltage swing, which makes this adder cell more susceptible to noise. To increase the output swing, CMOS inverter is added to this circuit.

Newly designed full adder [20] is a combination of low power transmission gates and pseudo nMOS gates as depicted in Figure 2. Transmission gate consists of a pMOS transistor and an nMOS transistor that are connected in parallel, which is a particular type of pass-transistor logic circuit. There is no voltage drop at output node, but it requires twice the number of transistors to design similar function.

Another full adder is the Complementary Pass Transistor Logic (CPL) with swing restoration, which uses 32 transistors [5, 6, 30, 31]. CPL adder produces many intermediate nodes and their complement to give the outputs. The most important features of CPL include the small stack height and low output voltage swing at the internal node which contribute to reduction in power consumption. The CPL suffers from static power consumption due to the low swing at the gates of the output inverters. *Double pass-transistor logic* (DPL) [8] and *swing restored pass-transistor logic* (SRPL) [9, 10] are related to CPL.

Some designs of the full adder circuit based on transmission gates are shown in Figure 3. Transmission gate logic circuit is a special kind of pass-transistor logic circuit [4, 5, 25]. The main disadvantage of transmission gate logic is that it requires twice the number of transistors than pass-transistor logic or more to implement the same circuit. TG gate full adder cell has 20 transistors. Similarly, transmission function full adder (TFA) cell has 16 transistors [4, 29]. It exhibits better speed and less power dissipation than the conventional CMOS adder due to the small transistor stack height.

3. Sum Function-Based Hybrid Full Adder Topologies

More than one logic style is used for implementation of the hybrid full adders. The hybrid adder cells may be classified into various categories depending upon their structure and logical expression of the Sum and Carry output signals. All hybrid designs use the best available modules implemented using different logic styles or enhance the available modules in an attempt to build a low power consuming full-adder cell [17–19]. Most full adder topologies are based on two XOR circuits: one to generate H (XOR) with $\overline{H}$ (XNOR), and the other to generate the Sum output. The carry signal is obtained by using one MUX (multiplexer):

$$\begin{aligned} \text{Sum} &= A \oplus B \oplus C, \qquad \text{Carry} = AB + C(A \oplus B), \\ H &= A \oplus B, \qquad \text{Sum} = H \oplus C, \\ \text{Carry} &= A \cdot \overline{H} + C \cdot H. \end{aligned} \tag{1}$$

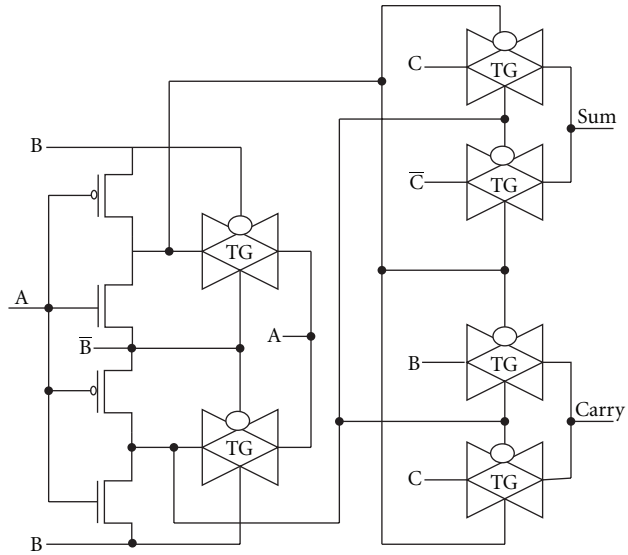
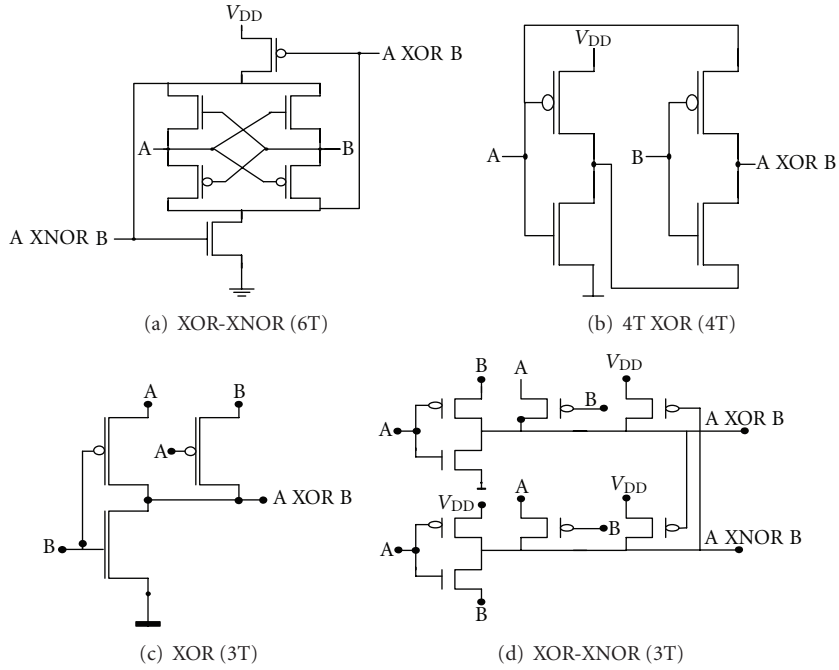


Figure 3: TG adder cell.

3.1. XOR-XNOR Topologies. In [28, 32–35], the XOR-XNOR circuit designed with static CMOS logic with complementary pull-up pMOS and pull-down nMOS networks is the conventional one, but it requires more number of CMOS transistors. This circuit may operate with full output voltage swing. Different XOR/XNOR topologies are illustrated in Figure 4. A PTL based 6-transitor XOR-XNOR circuit presented in [34] has full output voltage swing and better driving capability.

A new set of low power four transistor (4T) XOR and XNOR circuits called powerless P-XOR and Groundless G-XNOR, respectively, is proposed in [25–28, 32]. The P-XOR and G-XNOR circuits consume less power than other designs because they have no direct supply voltage (V_{DD}) or ground connection. The performance of the complex logic circuits is affected by the individual performance of the XOR-XNOR circuits that are included in them. An XOR and XNOR function with low circuit complexity can be achieved with only three transistors (3T) in PTL. Despite the saving in transistor count, the output voltage level is degraded at certain input signal combinations.



(a) XOR-XNOR (6T) (b) 4T XOR (4T)

(c) XOR (3T) (d) XOR-XNOR (3T)

Figure 4: Basic designs of XOR-XNOR gate found in literature.

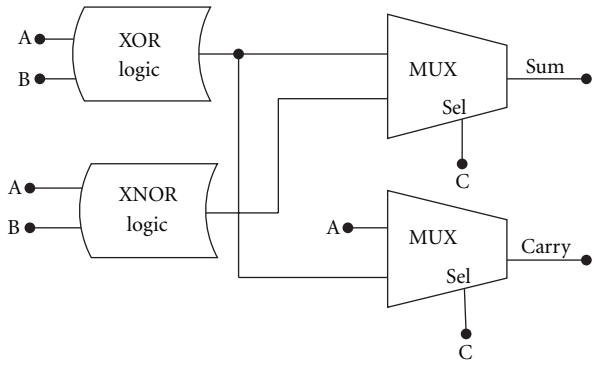


Figure 5: *Cascaded* XOR-XNOR based-*adder.*

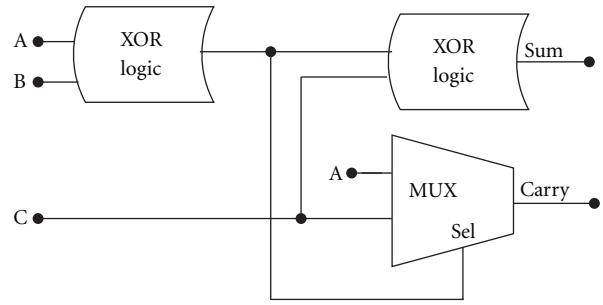


Figure 6: *Centralized* XOR-XNOR based-*adder*.

Generally, the main aim is to reduce the number of transistors in the adder cell and consequently to reduce the number of power dissipating nodes. This is achieved by utilizing intrinsically low power consuming logic styles like TFA, TGA or simply passing transistors. There are three main components to design a hybrid full adder circuit [19]. These are XOR or XNOR, Carry generator and Sum generator. Hybrid adders may be classified into two groups which are as follows.

3.2. Cascaded Output Based Adders (Group 1). In this category, signal Sum is generated using, either two cascaded XOR or two cascaded XNOR modules. Figure 5 shows the basic blocks of this category. Almost all the circuits in this category suffer from high delay in generating Sum and Carry signals. The Static Energy Recovery full adder (SERF) falls under this category [23].

3.3. Centralized Output Based Adders (Group 2). In this category, Sum and Carry are generated using intermediate signals XOR and XNOR. In this group, output Sum and Carry are generated faster than the outputs in cascaded output full adders. The key point here is to produce intermediate signals simultaneously. Otherwise, there may be glitches, unnecessary power consumption, and longer delay. Figure 6 shows the basic blocks of this category. TGA and TFA are in this category. Some of the hybrid full adders do not belong to any of these two groups, such as Complementary and Level Restoring Carry Logic (CLRCL) full adder [26] and Multiplexer based (MBF 12T) full adder [18].

3.4. 10T Full Adder. In [24] different components have been combined to make 41 new 10T full adder full adders. Some 10T full adders can be designed by interchanging the inputs of the module having lowest propagation delay amongst all the 10T full adder circuits. The design of the 10T adder cell is based on an optimized design for the XOR function

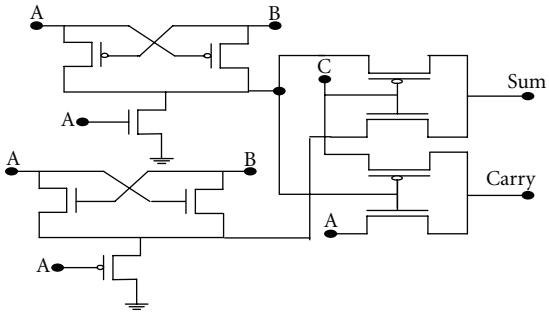


Figure 7: XOR-XNOR- (3T-) based 10T full adder.

and pass transistor logic to implement the addition logic function. Two XOR operations are required to calculate the Sum function. Each XOR operation requires four transistors (4T). 2X1 MUX is used for Carry function implemented using two transistors.

Another 10T full adder based on centralized structure is shown in Figure 7. Intermediate XOR and XNOR are generated using three transistor (3T) XOR and XNOR gate. Sum and Carry are generated using two double transistors multiplexers. 3T XOR and XNOR consume high energy due to short circuit current in ratio logic. They all have double threshold losses in full adder output terminals. This problem usually prevents the full adder design from operating at low supply voltage or cascading directly without extra buffering. The lowest possible power supply is limited to $2V_{tn} + V_{tp}$ where V_{tn} and V_{tp} are the threshold voltages of nMOS and pMOS respectively. The basic advantages of 10T transistor full adders are: less area compared to higher gate count full adders, lower power consumption and lower operating voltage. It becomes very difficult and even obsolete to keep full voltage swing operation as the designs with fewer transistor count and lower power consumption are pursued.

3.5. 9T Full Adder. In nine transistor (9T) full adder circuit, we have only one 3T XOR gate as is shown in the Figure 8 [36]. The design of 3T (M1–M3) XOR circuit is based on a modified version of a CMOS inverter and a pMOS pass transistor. When $A = 1$ and $B = 0$, voltage degradation due to threshold drop occurs across transistor M3 and consequently the output (M3) is degraded with respect to the input. The voltage degradation due to threshold drop can be minimized by increasing the W/L ratio of transistor M3. An equation relating threshold voltage of a MOS transistor to the channel length and width is given as

$$V_T = V_{T0} + \gamma\left(\sqrt{V_{SB} + \phi_0} - \sqrt{\phi_0}\right) - \alpha_l \frac{t_{ox}}{L}(V_{SB} + \phi_0) - \alpha_v \frac{t_{ox}}{L}(V_{DS}) + \alpha_W \frac{t_{ox}}{L}(V_{SB} + \phi_0), \quad (2)$$

where

V_{T0} is the zero bias threshold voltage,

γ is bulk threshold coefficient,

ϕ_0 is $2\phi_F$, where ϕ_F is the Fermi potential,

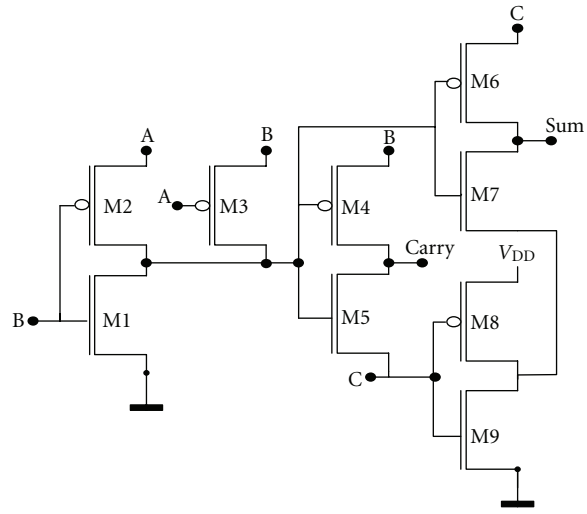


Figure 8: 9T full adder.

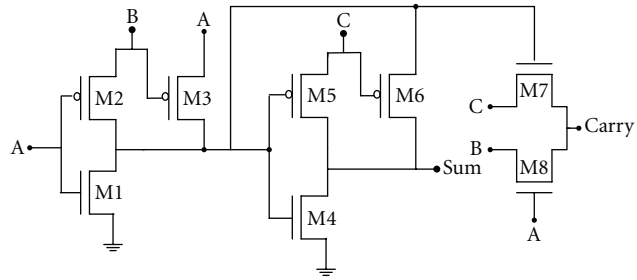


Figure 9: 8T full adder.

t_{ox} is the thickness of the oxide layer,

α_l, α_v, and α_w are the process dependent parameters.

The above equation shows that by increasing channel width (W) it is possible to decrease the threshold voltage (V_{th}). So it is possible to minimize the voltage degradation due to threshold voltage by increasing the width of M3 transistor & keeping the length constant. In 9T full adder circuit pass transistor M4, M5 and M6, M7 are used for Carry and Sum function respectively.

3.6. 8T Full Adder. The design of an eight transistor (8T) full adder using 3T XOR gates is shown in Figure 9 [37]. The Boolean equations for the design of the eight transistor full adder are as follows:

$$\begin{aligned} \text{Sum} &= A \oplus B \oplus C, \\ \text{Carry} &= BC + CA + AB = C(A \oplus B) + AB. \end{aligned} \quad (3)$$

The Sum output function is obtained by a cascade of 3T XOR gates. Carry can be realized using a wired OR logic in accordance with the above equation.

Another 8T full adder using centralizer output condition contains three modules—two 3T XOR gates and one multiplexer (2T). It can work at high speed with low power dissipation due to minimum number of transistors and small transistor delay.

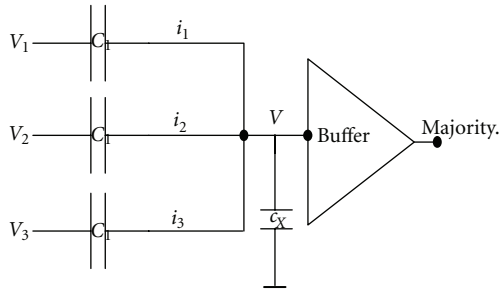


Figure 10: Implementation of Majority functions (MOSCAP).

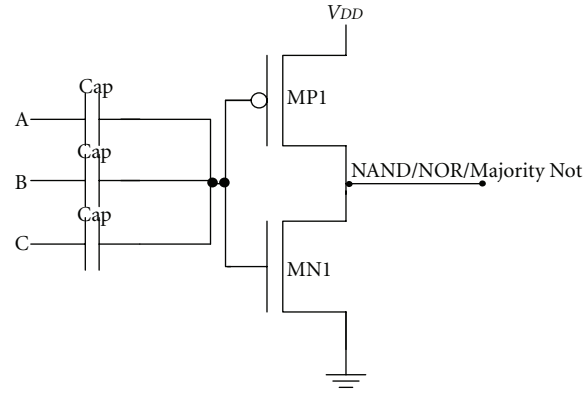


Figure 11: Majority function- (MOSCAP-) based logic gates.

4. Carry (Majority) Function-Based Hybrid Full Adder Topologies

The Majority function is a logic circuit that functions as a majority vote to determine the output of the circuits [38]. This function has only odd number of inputs. Its output is equal to "1" when the number of input logic "1" is more than logic "0". Comparing to the XOR implementations of full adder cells, Majority-based full adders are more reliable and robust [38]. Moreover, the bridge style full adder circuits [39] by sharing transistors can operate faster and are smaller than the conventional CMOS full adder circuits.

4.1. Literature Review of Majority Functions. Boolean algebra with three variables is used to facilitate the conversion of a sum-of-products expression to minimize majority logic as shown in Table 1 [38]. Three binary variables can only produce eight unique minterms. Any three-variable Boolean function can be represented by the combinations of up to eight of these minterms. The three-variable Boolean function of 5–7 minterms can be represented using the complement form of 3–1 minterms. Based on DeMorgan's theorem, a Boolean function, expressed as the sum of several minterms, can also be expressed as the complement of the sum of the remaining minterms. The simplified majority expressions for 13 standard functions are given in Table 1.

4.2. Circuit-Interpretation-of-MOS Capacitor- (MOSCAP-) Based Majority Not Function. The majority structure is implemented by three input capacitors. These three input capacitors prepare an input voltage that is applied for driving static CMOS buffer. The majority gates may be designed with more inputs by this method by increasing the number of input capacitors. The capacitor network is used to provide voltage division for implementing majority logic as explained below.

Total current I at node $V = I_1 + I_2 + I_3$,

$$\begin{aligned}(V)c_x s &= (V_1 - V)c_1 s + (V_2 - V)c_1 s + (V_3 - V)c_1 s \\ &= (c_X + 3c_1)V = (V_1 + V_2 + V_3)c_1, \\ V &= (V_1 + V_2 + V_3)\left(\frac{c_1}{3c_1 + c_X}\right).\end{aligned} \tag{4}$$

The input capacitors shown in Figure 10 are used to prepare an input voltage that is applied for driving static inverter. When the majority of inputs are "0", the output of capacitor network is considered as logic "0" by the CMOS buffer and consequently the output of buffer is 0 V. When the majority of inputs are logic "1", the output of capacitor network is considered logic "1" by the CMOS buffer and consequently the output of buffer is V_{DD}. The input capacitance of the CMOS buffer is negligible and has no effect on operation of the circuit. Three capacitors perform voltage summation to implement scaled-linear sum. Through superposition of input capacitors, increased input voltage is scaled at point V as shown in Figure 10 and given in Table 2 [40].

4.3. MOS Capacitor (MOSCAP) Structure. In this section hardware implementation and construction of MOSCAP are discussed. Tying the drain and source of a MOSFET together results in a MOSCAP. Many realizable alternatives such as Poly-Insulator-Poly capacitors (PIPCAP), Metal-Insulator-Metal capacitors (MIMCAP), or Metal-Oxide-Semiconductor capacitors (MOSCAP) can be utilized for realizing the capacitor network. However, MOSCAP has an advantage of more capacitance; less chip area. The nMOSCAP usually has lesser capacitance in comparison to pMOSCAP for the same area, so pMOSCAP is used for implementing the capacitor network. Table 3 shows that the variation of MOS capacitor with respect to channel width of MOS transistor.

4.4. Implementation of (NAND, NOR and Majority Not) Gates Using MOSCAP Majority Function. Figure 11 shows the circuit used to implement Majority Not function with inverter utilizing high-V_{th} for both nMOS and pMOS. This circuit can be used to implement NAND gate using high-V_{th} nMOS and low-V_{th} pMOS, and NOR gate using low-V_{th} nMOS and high-V_{th} pMOS. The Majority gates may be designed with more inputs by this method by increasing the number of input capacitors. The capacitor network is used to provide voltage division for implementing majority logic.

There are two methods to design the NAND and NOR logic circuits. First method is the transistor sizing that shifts the voltage transfer curve (VTC) to the left and right by changing the ratio of (W/L)n to (W/L)p. Raising this ratio moves VTC to the left; therefore, this circuit will operate as

Table 1: Majority expression of standard logic functions.

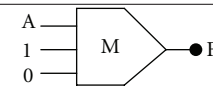
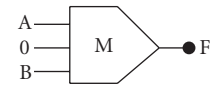
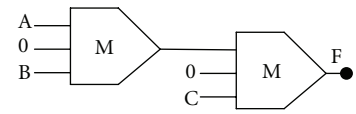
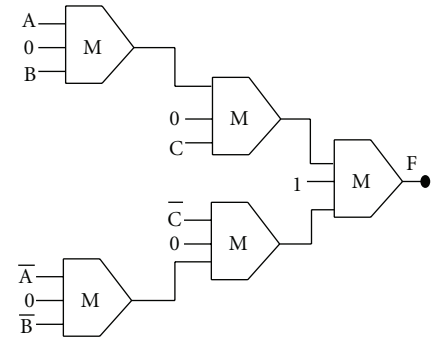
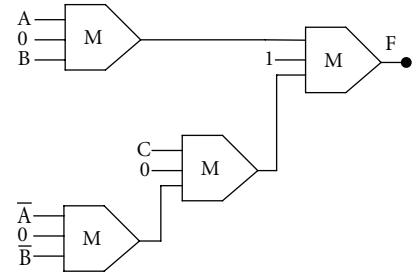
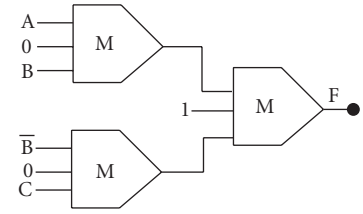
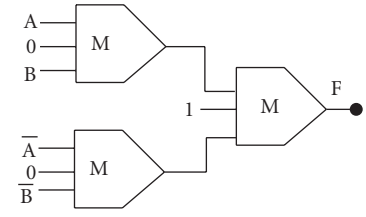
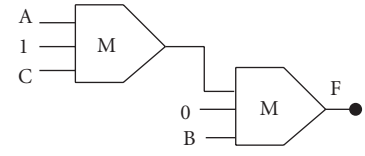
Standard Boolean function	Majority expression	Function implementation diagram
$F = A$	$M(A, 0, 1)$	
$F = A \cdot B$	$M(A, B, 0)$	
$F = A \cdot B \cdot C$	$M(M(A, B, 0), C, 0)$	
$F = A \cdot B \cdot C + \overline{A} \cdot \overline{B} \cdot \overline{C}$	$M\{M(M(A, 0, B), C, 0),\ M(M(\overline{A}, \overline{B}, 0), \overline{C}, 0), 1\}$	
$F = A \cdot B + \overline{A} \cdot \overline{B} \cdot C$	$M\{M(A, 0, B), M(M(\overline{A}, \overline{B}, 0), C, 0), 1\}$	
$F = A \cdot B + \overline{B} \cdot C$	$M\{M(A, 0, B), M(\overline{B}, 0, C), 1\}$	
$F = A \cdot B + \overline{A} \cdot \overline{B}$	$M\{M(A, 0, B), M(\overline{A}, 0, \overline{B}), 1\}$	
$F = A \cdot B + B \cdot C$	$M(B, M(A, 1, C), 0)$	

Table 1: Continued.

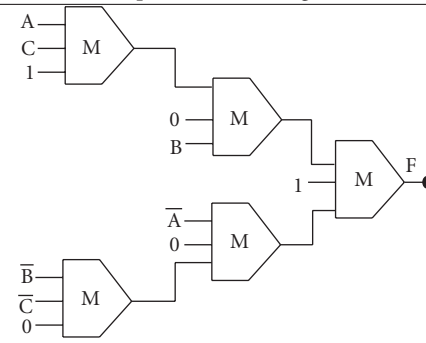
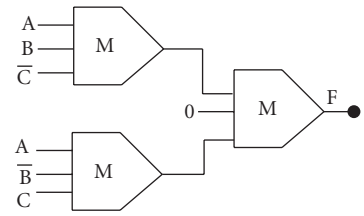
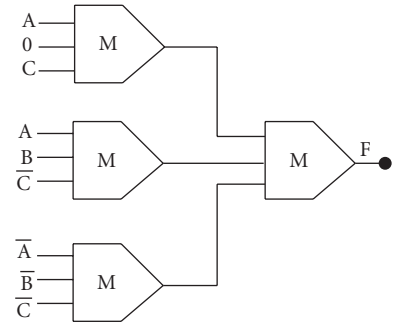
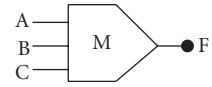
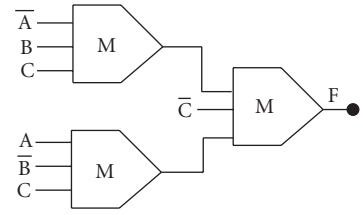
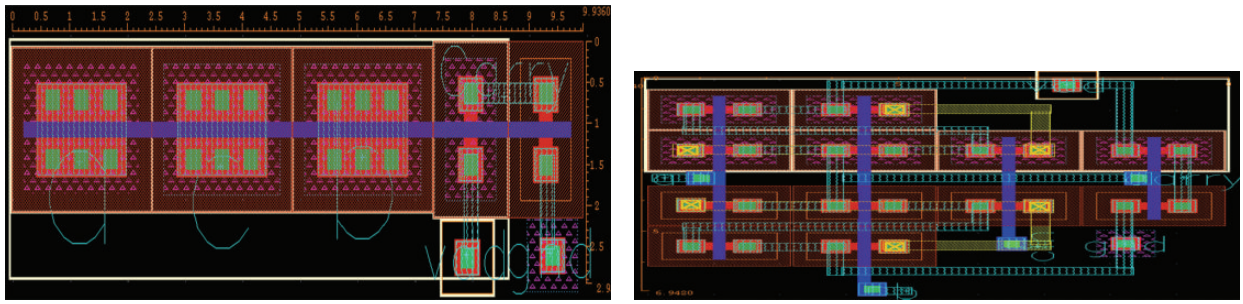
Standard Boolean function	Majority expression	Function implementation diagram
$F = A \cdot B + B \cdot C + \overline{A} \cdot \overline{B} \cdot \overline{C}$	$M\{M(B, M(A, C, 1), 0), M(\overline{A}, M(\overline{B}, \overline{C}, 0), 0), 1\}$	
$F = A \cdot B \cdot C + A \cdot \overline{B} \cdot \overline{C}$	$M\{M(A, B, \overline{C}), M(A, \overline{B}, C), 0\}$	
$F = A \cdot B \cdot C + \overline{A} \cdot B \cdot \overline{C} + A \cdot \overline{B} \cdot \overline{C}$	$M\{M(A, C, 0), M(A, B, \overline{C}), M(\overline{A}, \overline{B}, \overline{C})\}$	
$F = A \cdot B + B \cdot C + A \cdot C$	$M(A, B, C)$	
$F = A \cdot B \cdot C + \overline{A} \cdot \overline{B} \cdot C + A \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot B \cdot \overline{C}$	$M\{M(\overline{A}, B, C), M(A, \overline{B}, C), \overline{C}\}$	

Table 2: Switching voltage at output node V of the capacitance network.

Inputs			Voltage at V node	Majority Not
A	B	C	V_{DD}	$\overline{\text{Carry}}$
0	0	0	0V	1
0	0	1	$V_{DD}/3$	1
0	1	0	$V_{DD}/3$	1
0	1	1	$2V_{DD}/3$	0
1	0	0	$V_{DD}/3$	1
1	0	1	$2V_{DD}/3$	0
1	1	0	$2V_{DD}/3$	0
1	1	1	V_{DD}	0

Table 3: Channel width v/s MOS capacitor in 0.18 μm Tech.

Cap	2.89 fF	4.89 fF	6.89 fF	8.89 fF	10.91 fF
Width (W) μm	1.59	2.71	3.83	4.95	6.07



(a) (b)

Figure 12: (a) MOSCAP Majority Not function layout. (b) Static CMOS bridge (Majority function) layout.

NOR function. Contrary to this, decreasing the ratio makes the NAND function. The second method uses high-threshold voltage (V_{th}) transistors (MP1 & MN1) as shown in Figure 4.

Simulation results in Table 4 illustrate the comparison of static logic gates with MOSCAP-based majority function, static and dynamic logic style.

4.5. Layout and Area Analysis of Majority Circuits. The layout of Majority Not function (MOSCAP) and static CMOS bridge-type Majority function circuits are shown in Figures 12(a) and 12(b), respectively, and the area is given in Table 5. The area of the MOSCAP Majority function (MOSCAP) circuit is 50% less than that of the bridge type Majority function circuit. At low voltages (say 1 V) delay and power consumption is much more improved in comparison to the static one, and hence MOSCAP Majority function is more reliable, power efficient with less occupation of chip area in VLSI circuit designing. By a perfect layout design, even more reduction in the area is possible and thus a more compact design can be implemented.

4.6. A Review of Majority-Function-Based Full Adder Topologies. As Table 6 exhibits, Sum is different at merely two places with Majority Not function when inputs are 000 or 111. The values of these two functions are not equal at $A = B = C =$ "0" and $A = B = C =$ "1". Therefore, we correct these two states by using a pMOS and an nMOS transistor. These transistors must be arranged in a way that ensures the correctness of the circuit [39].

The basic logic design of a full adder includes two 3-input NAND and NOR gates with Majority Not function inputs as shown in Figure 13. The MajFA1 adder is designed using pass-transistor logic as shown in Figure 13 similar to the [39]. The logic (NAND and NOR) gates designed with pass transistor logic styles have less power dissipation and delay than in standard CMOS.

In six mid-states of Table 6, the Sum output is equal to $\overline{\text{Carry}}$ (Majority Not Function) and the MP1 and MN1 transistors are off. But, in all one input state and all zero

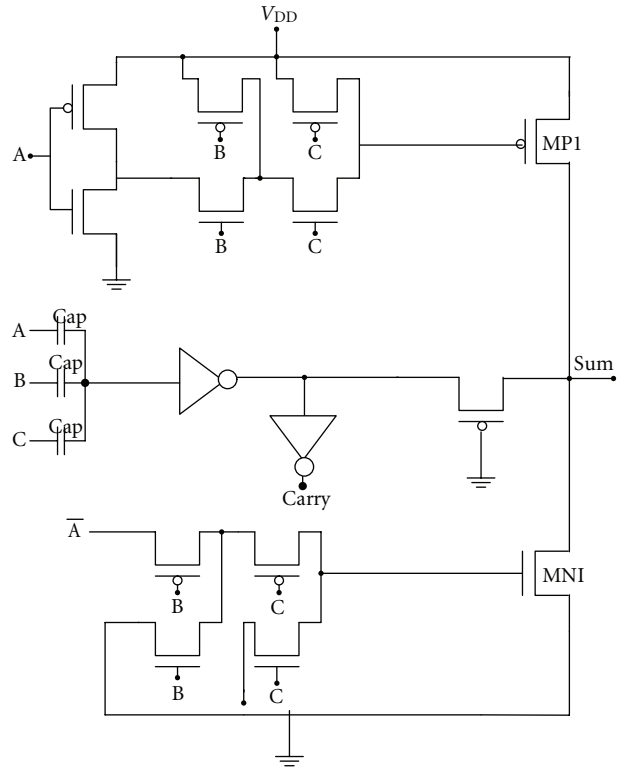


Figure 13: Design methodologies for Majority-function-based full adder (MajFA1).

input state the Sum is obtained by the NAND and NOR gates, respectively. In order to design circuit operations in the given state one nMOS and one pMOS pass transistor are added to the circuit. These transistors are used to disconnect the path between $\overline{\text{Carry}}$ and Sum in all "0" and "1" input state.

4.7. Majority Full Adder Using 3-Input Majority Not Function (MOSCAP). In this section full adder based on low power design of 3-input Majority Not function (MOSCAP) with

Table 4: Simulation results of NAND, NOR, and majority Not logic gates at 1 V.

Design	Static Majority function			MOSCAP Majority function		
	Delay (ps)	Power (μw)	PDP (10^{-18} j)	Delay (ps)	Power (μw)	PDP (10^{-18} j)
NAND	36	0.041	1.47	23	0.038	0.87
NOR	40	0.042	1.68	27	0.039	1.05
Maj. Not	43	0.048	2.06	18	0.038	0.68

Table 5: Simulation layout comparisons of Majority function logic.

μm	Bridge Majority function			MOSCAP Majority function		
Layout	Length (μm)	Width (μm)	Area (μm^2)	Length (μm)	Width (μm)	Area (μm^2)
Dimen.	8.8	6.9	60.7	9.9	2.95	29.2

standard logic gates is discussed. The Boolean expression may be expressed as

$$\text{Sum} = \overline{\text{Carry}} \cdot (A + B + C) + A \cdot B \cdot C. \quad (5)$$

$\overline{\text{Carry}}$ logic output will be generated by 3-inputs MOSCAP Majority Not function.

The MajFA2 full adder uses 12 transistors, and 3 capacitors are based on pseudo CMOS structure with MOSCAP Majority function. Full adder output $\overline{\text{Carry}}$ function is designed with 3 input Majority Not function logic. In this design, "a" and "b" inverters implement NOR and NAND functions, respectively.

The full adder (MajFA3) is based on MOSCAP Majority Not function with only static CMOS inverter as shown in Figure 14(b). Simulation results illustrate that the reported adder circuits having low PDP works efficiently at low voltages [41]. Outputs of the circuit will be connected to power supply or ground and therewith, the circuit has good driving capability. These inverter-based full adders are a suitable structure for the construction of low-power and high-performance VLSI systems.

4.8. Majority Full Adder Using 5-Input Majority Not Function (MOSCAP). Here if we exert a Majority function of five inputs out of which two are $\overline{\text{Carry}}$ and the other three are logic inputs (A, B, C), we will get Sum of the output as explained in the given equation. Consequently, according to this fact $\overline{\text{Sum}}$ is generated by means of two Majority Not functions. The first one is a three input Majority Not function which results in the $\overline{\text{Carry}}$ function and the second one is a five-input Majority Not function which creates $\overline{\text{Sum}}$:

$$\begin{aligned}
\text{Sum} &= ABC + \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\,\overline{C} \\
&= ABC + \left(\overline{AB} \cdot \overline{AC} \cdot \overline{BC}\right) \cdot (A + B + C) \\
&= ABC + \overline{\text{Carry}} \cdot \text{Carry} + \overline{\text{Carry}}\ (A + B + C) \\
&= ABC + \overline{\text{Carry}}\ (AB + AC + BC) + \overline{\text{Carry}}\ (A + B + C) \\
&= \text{Majority}\left(A, B, C, \overline{\text{Carry}}, \overline{\text{Carry}}\right).
\end{aligned} \quad (6)$$

Reference [42]. MajFA4 full adder design has two stages. $\overline{\text{Carry}}$ is implemented by means of a Majority Not function in the first stage and in the second stage a five-input Majority Not function is used for implementing Sum function.

In the full adder circuit shown in Figure 15, first Majority Not gate is made of 3-input MOSCAP with a CMOS inverter. Three Cap1 capacitors with input signal and CMOS inverter are used to generate $\overline{\text{Carry}}$ signal. These three input capacitors prepare an input voltage that is applied for driving CMOS inverter. If more than two inputs become high then the M1 transistor will turn-on and in this case the $\overline{\text{Carry}}$ will fall to "0" logic. Therefore, Carry will be "1" logic. Otherwise, M1 and M3 will turn-off and turn-on, respectively, and output Carry will fall to "0" logic. Second Majority Not function is based on five-input capacitors and CMOS inverter (M2 & M4 transistors). It has two capacitors Cap2 and three inputs Cap2. Based on function, $\text{Sum} = \text{Maj}(A, B, C, \overline{\text{Carry}}, \overline{\text{Carry}})$, the value of Cap2 is two times the value of Cap1, because we are providing two $\overline{\text{Carry}}$ as inputs with two parallel capacitors, and these two capacitors are added. One $2 \times$ Cap2 capacitance is attached between $\overline{\text{Carry}}$ output and input of transistor M2. The basic scheme of this full adder circuit utilizes only 7 capacitors and 8 transistors. The main advantage of this design is its simplicity, modularity, and lesser number of transistors being used.

As reported in MajFA5, hybrid full adder circuit in Figure 16 uses 16 transistors. Its output Sum function is based on 5-input Majority Not gates. In this design, the first Majority Not gate is implemented with a high-performance CMOS bridge circuit [43]. This design uses more transistors, called bridge transistors, sharing transistors of different paths to generate new paths from supply lines to circuit outputs. The bridge design offers more regularity and higher performance than the other CMOS design styles and is completely symmetric in structure. Using the bridge circuit leads to reduction in delay and power consumption of the full adder cell and it also increases the robustness of the circuit.

5. Proposed Hybrid Full Adder Topologies

5.1. XOR-XNOR- (3T-) Based Full Adders. The general structure of a XOR-based full adder consists of one exclusive

Table 6: Truth table for Majority-function-based full adder.

Inputs				Full adder logic outputs	
A	B	C	Carry	$\overline{\text{Carry}}$	Sum = Maj($A, B, C, \overline{\text{Carry}}, \overline{\text{Carry}}$)
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	0
1	1	1	1	0	1

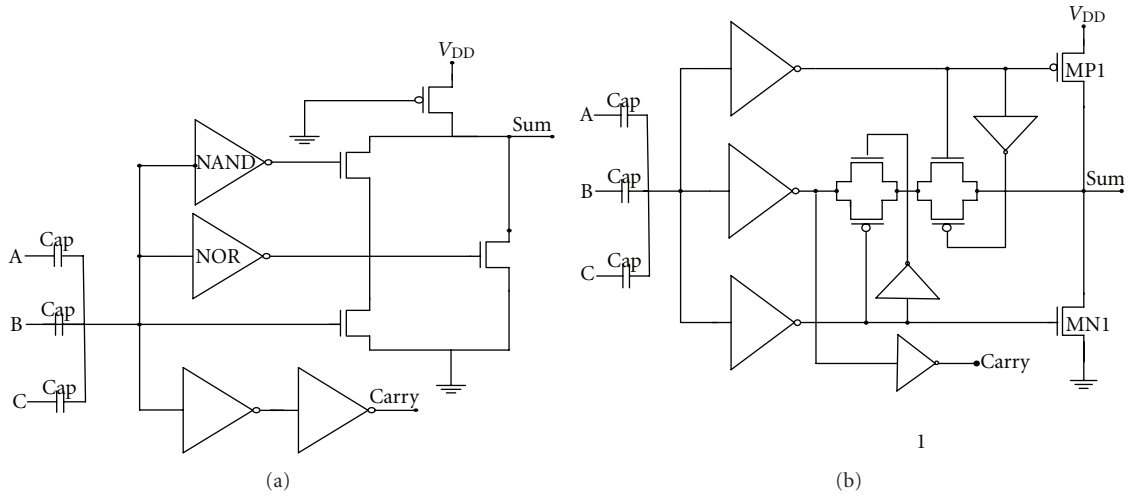


Figure 14: (a) Majority-function-based full adder (MajFA2). (b) Inverter-based Majority full adder (MajFA3).

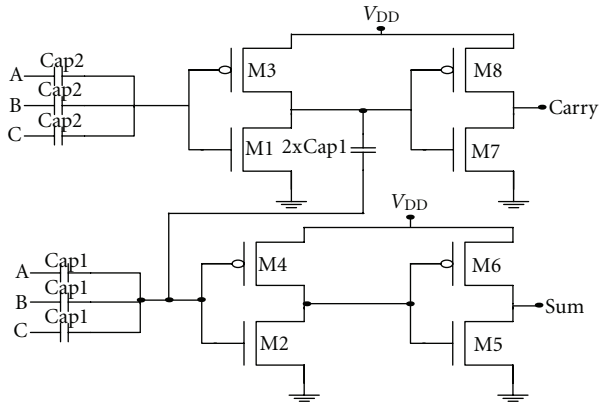


Figure 15: 3-input MOSCAP Majority full adder (MajFA4).

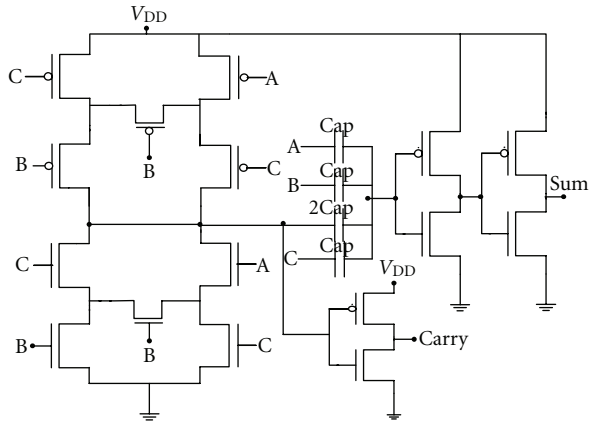


Figure 16: 5-input MOSCAP Majority full adder (MajFA5).

OR/NOR function (XOR/XNOR), two transmission gates in the middle, and one XOR gate to the right as shown in Figure 17. The complementary outputs of the XOR/XNOR gate are used to control the transmission gate which together realizes a multiplexer circuit producing the carry.

The circuit is a combination of two logic styles and offers high-speed, low-power consumption and energy efficiency. Lowering the supply voltage appears to be a well-known means of reducing power consumption. However, lowering the supply voltage also increases the circuit delay and degrades the drivability of cells designed with certain logic styles. By selecting proper (W/L) ratio, we can optimize the circuit performance parameters without decreasing the power supply. The 3T XOR/XNOR gates are used in a designed full adder circuits as shown in Figures 18 and 19.

In design1 full adder circuit, XOR circuit comprises M1, M2 and M3 transistors and the output of M4 and M5 transistor is XNOR circuit. TG (M6, M7) and TG (M8, M9) give the carry and restored output swing. TG (M10, M11) and pass transistor M12, M13 are used for Sum output

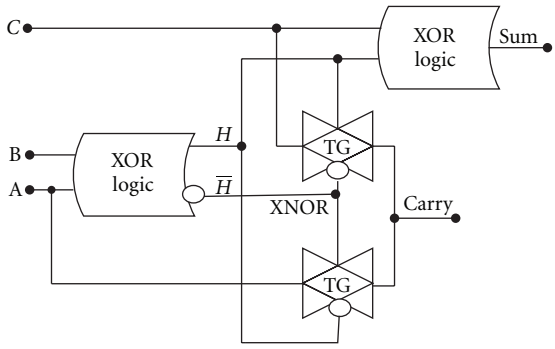


Figure 17: General structure of proposed XOR-XNOR-based adder.

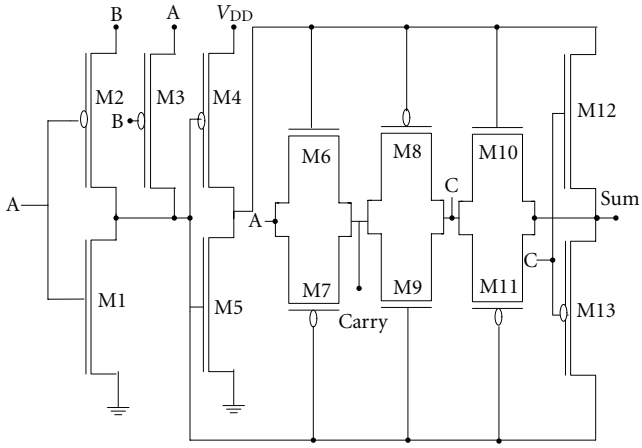


Figure 18: XOR- (3T-) based design 1 full adder.

and to restore the output swing as shown in Figure 18. It implements the complementary pass-transistor logic to drive the load.

A novel 16-transistor full adder circuit that generates XOR-XNOR outputs simultaneously is shown in Figure 19. Similarly in design 2 full adder circuits M1, M2 and M3 are used as XOR and the output of M4, M5, M6 is XNOR circuit. The cross-coupled PMOS transistors are connected between XOR and XNOR output to alleviate threshold problem for all possible input combination at low voltage ($0.8V_{DD}$) and reduce short-circuit power dissipation. The cross-coupled two pMOS transistors (M7, M8) are connected between XOR and XNOR outputs to eliminate the nonswing operation at low voltage.

5.2. Majority-Function-Based Full Adder. In the proposed methodology, we have designed two full adder topologies, one is based on static bridge logic style and other is based on dynamic bridge logic style. The proposed adder modules enjoy advantages of the bridge style including low-power consumption and the simplicity of the design. The proposed full adder structure design (PMajFA1) is based on capacitor network and Majority Not function as shown in Figure 20.

The proposed Majority-function-based adder design has some advantages which improves the metrics of the proposed design significantly. In the reported previous full adder design [43], the CMOS bridge circuit does not have high driving power to drive the capacitor (2Cap) and an inverter. This increases the delay at low voltages in nanotechnology. However, in the proposed design, an inverter with high driving power drives four transistor gates (bridge circuit) and an inverter. Besides, the more driving power of the inverter in comparison to the bridge circuit and the sum of the gate capacitances of four transistors being less than the capacitance of the capacitor (2Cap) of the reported design (MajFA5) illustrate the superiority of the proposed full adder design (PMajFA1).

Furthermore, as in the proposed design three capacitors perform voltage summation to implement scaled-linear sum instead of five capacitors. It has larger noise margins than the previous design. Moreover, the proposed design have no threshold loss problem at its nodes and has higher noise margin compared to MajFA3 (minimum no of transistor) because its inverters has normal VTC curve, which works on inverters with shifted VTC and its operation is highly dependent on the proper operation of these inverters.

The Majority-function-based proposed design 2 (PMajFA2) adder uses 15 transistors and is based on regular dynamic CMOS bridge transistors. Full adder output $\overline{\text{Carry}}$ function is designed with 3-input Majority Not function logic and output Sum function is generated using dynamic CMOS bridge logic style as shown in Figure 21. The advantage of these adder cells are higher speed, lower transistor count and it compromises noise margin. This type of circuit is preferred in smaller area requirement with lesser delay at low voltage. It has larger noise margins in comparison to the previous designs and reported full adder circuits.

6. Simulation Results

The simulation has been performed for different supply voltage ranging from 0.8 V to 1.8 V, which allows us to compare the speed degradation and average power dissipation of the reported and newly designed adder topologies. The results of the designed circuits in this paper are compared with a reported standard CMOS full adder circuit. To compare one-bit full adder's performance, we have evaluated delay and power dissipation by performing simulation runs on a Cadence environment using 0.18-μm CMOS technology at room temperature.

The simulation test bench used for load analysis is shown in Figure 22. Output loads have been added according to the test bench. The two inverters with same *W/L* have been used to make output buffers. Output load was added at the input of the output buffers to evaluate driving capability of the circuits without output buffers. We used buffers to check the output logic levels. Power and delay of inverters have been included in power and delay calculation of the whole circuit. The transistor size for buffers is two for pMOS and one for nMOS.

The transistors that are used in XOR-XNOR- (3T-) based full adder designed circuits (13T & 16T) are using 3T

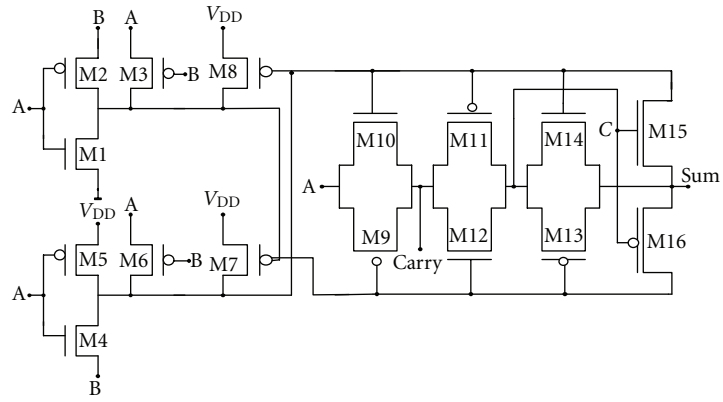


Figure 19: XOR-XNOR- (3T-) based design 2 full adder.

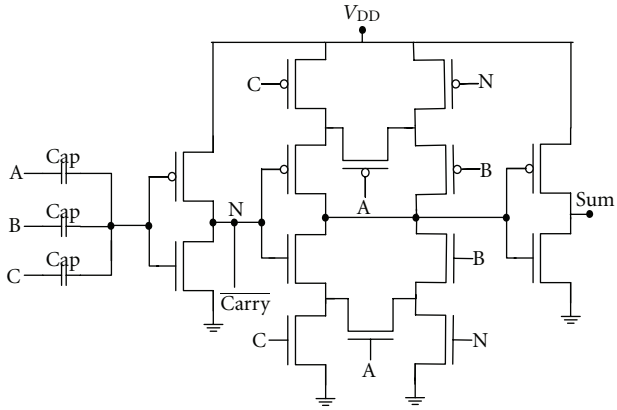


Figure 20: Majority-function-based adder design 1 (PMajFA1).

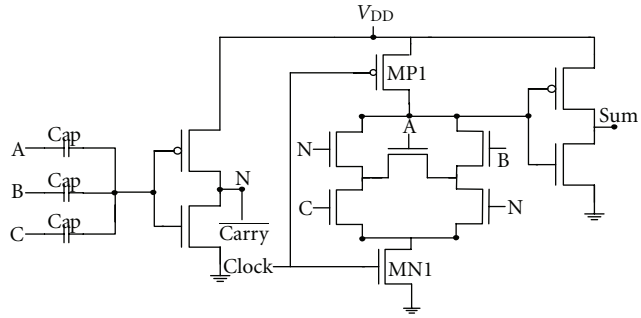


Figure 21: Majority function-based adder design 2 (PMajFA2).

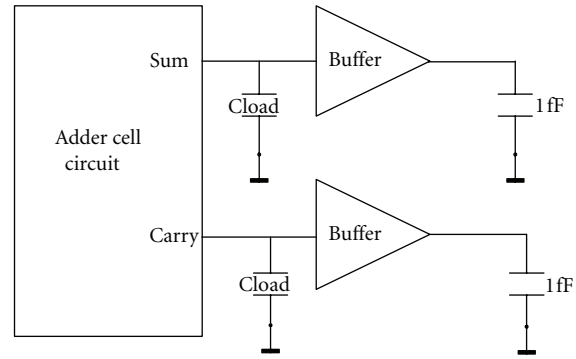


Figure 22: Simulation test bench for load Analysis.

transistors XOR logic. Thus the area overhead of the designed circuits is lower than that of the reported conventional adders and also some other adder circuits. By optimizing the transistor size of full adders considered, it is possible to reduce the delay of all the adders without significantly increasing the power consumption, and transistor sizes can be set to achieve minimum *power delay product* (PDP) and energy delay product (EDP). All adders were designed with minimum transistor sizes initially and then simulated. The PDP (10^{-18} j) and EDP (10^{-30} sj) are a quantitative measure of the efficiency and a compromise between power dissipation and speed. PDP and EDP are particularly important when low power and high speed operation are needed. At low voltages, design 1 is better than 9T and design 2. From the simulation results, it is perceptible that design 1 is superior in PDP to all the other designs at all simulation conditions.

Each one-bit full adder has been analyzed in terms of propagation delay, average power dissipation, and their products. By the value of delay, power, power-delay product and energy delay product of C-CMOS, hybrid and newly designed full adders are measured. The smallest voltage that could work on 10T is 1.4 V. The lowest supply voltage for simulation comparison for conventional CMOS, and newly designed full adder circuits, is 0.8 V (V_{DD}). For each transition, the delay is measured from 50% of the input voltage swing to 50% of the output voltage swing. The maximum delay is taken as the cell delay.

High speed of the designed full adders is due to the short path between input and output logic circuit. Simulation results (Figure 23(a)) show that design 2 is the best circuit in terms of speed at all voltages since XOR and XNOR logic is generated separately in a single circuit. It has high delay and high sensitivity against voltage scaling. Design 2 is miles ahead than design 1 and shows better performance even than 9T full adder. At low voltages, design 2 shows better delay than 9T. 9T has minimum number of transistors but high delay because XNOR logic is generated using XOR with

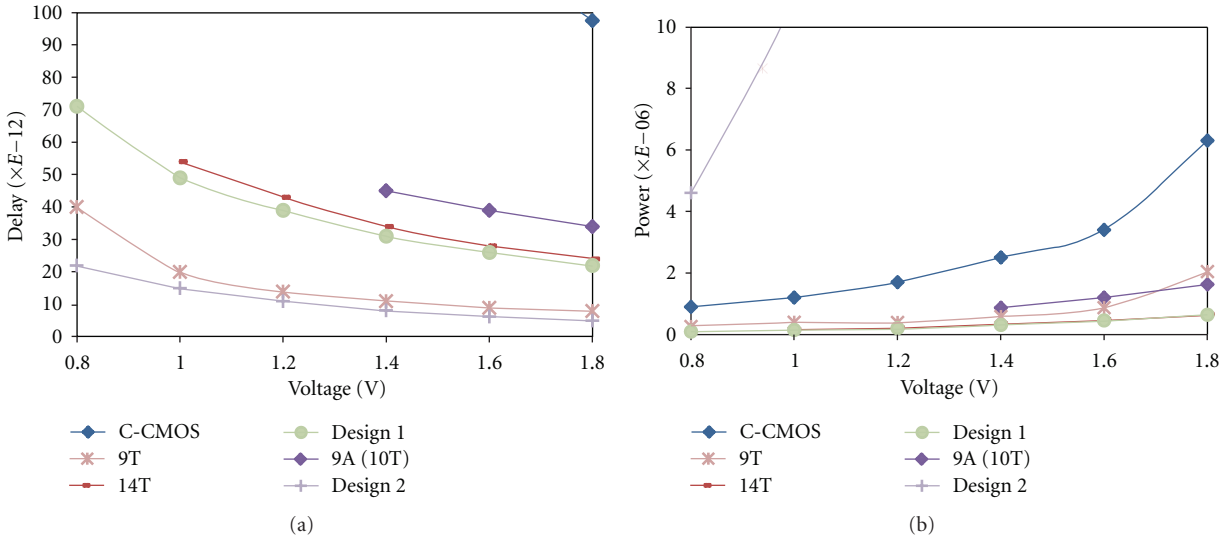


Figure 23: (a) Delay (ps) of XOR-XNOR-based adders. (b) Power (μW) XOR-XNOR-based adders.

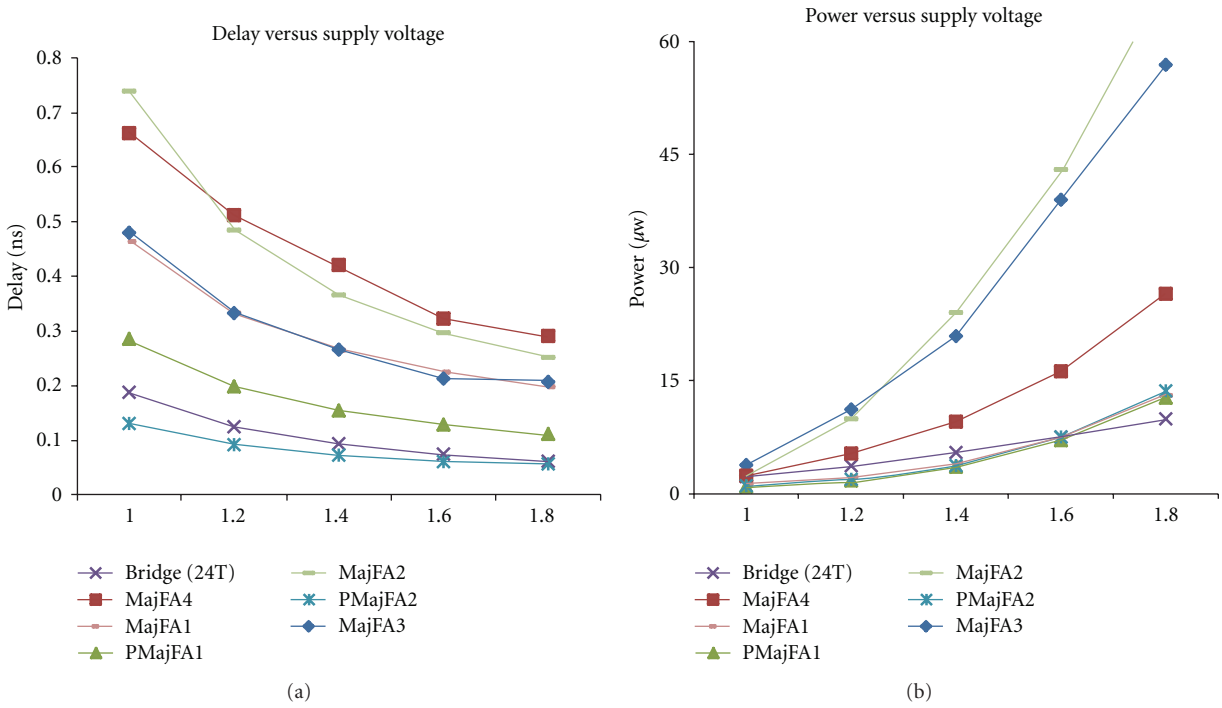


Figure 24: (a) Delay of Majority-function-based full adder circuits. (b) Power of Majority-function-based full adder circuits.

CMOS inverter. However, at all supply voltage variations Design 2 is faster than 9T full adder.

Figure 23(b) shows that proposed design 2 full adder is the most power consuming circuit at 1.8 V. The power consumption worsens as we increase the supply voltage. Design 1 has the least power consumption in comparison to the other simulated adder circuits. It worked successfully even at low voltage. Design 2 full adder consumes higher power due to the use of high power consuming 3T XOR and a 3T XNOR gate in a single unit.

Simulation results (Figure 24) show that Majority function based design 2 full adder (PMajFA2) is the best circuit in terms of speed at all voltages. It has low delay and high sensitivity against voltage scaling. Design 2 is miles ahead than the reported design and shows better performance.

6.1. Load Analysis. Output load is one of the important parameters that affects power and performance of the circuits. Here we changed the output loads from 2 fF to 500 fF. A fixed value 1 fF capacitance has been added at the output of the buffer circuit. Minimum output load for all the simulation is 2 fF, except for the case in which we study the effect of output load on full adder. The effect of output load is shown in Figures 25 and 26. All the circuits have been

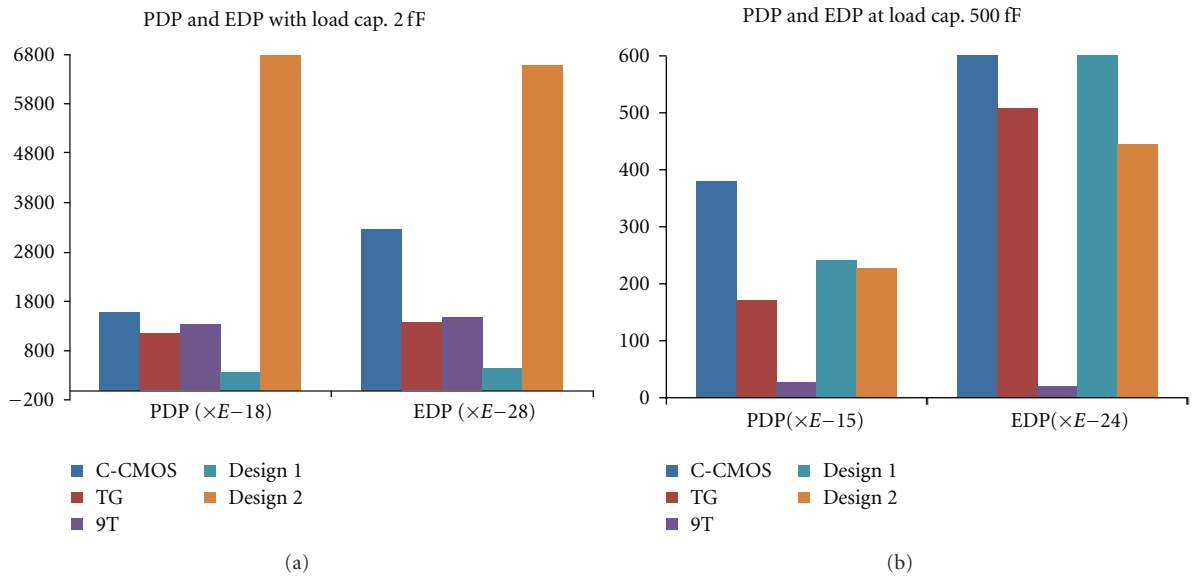


Figure 25: (a) PDP and EDP of XOR-XNOR based full adder cells with load capacitance (2 fF) at 1.8 V. (b) PDP and EDP of XOR-XNOR based full adder cells with load capacitance (500 fF) at 1.8 V.

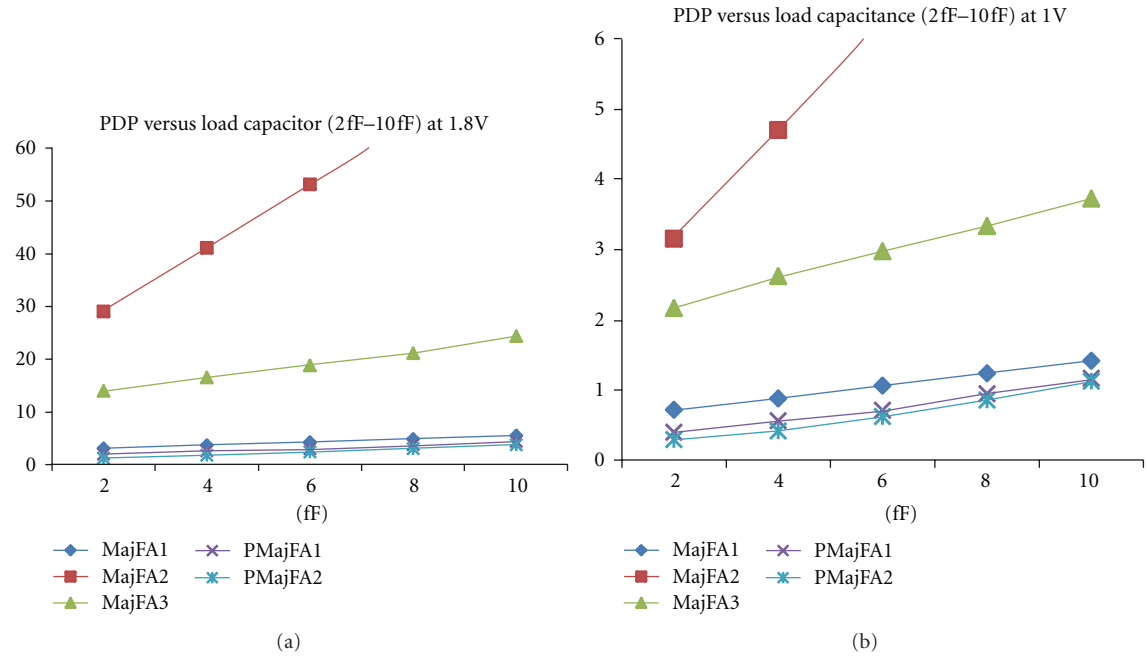


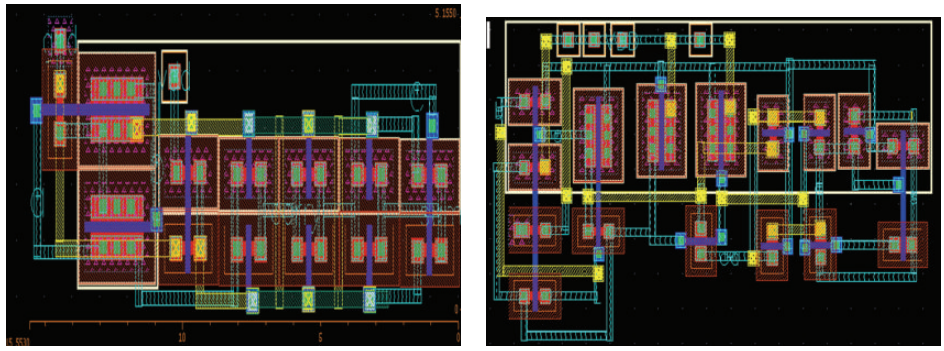
Figure 26: (a) PDP comparison of Majority-function-based full adder cells with capacitance load variation at 1.8 V. (b) PDP comparison of Majority-function-based full adder cells with capacitance load variation at 1 V.

optimized at 1.8 V supply voltage with 2 fF output load. For fair comparisons, the conditions were kept unchanged for all circuits.

9T is the best circuit in terms of power consumption since it has the least power consuming for all values of output load. The power of the designed circuits changes sharply by increasing the output load capacitance value as shown in Table 3 at 1.8 V. At 2 fF load, design 2 is the fastest circuit. Design 2 full adder is, however, placed second after 9T in terms of delay in high output load capacitance 500 fF. As shown in Figure 25, design 1 has the lowest PDP for all output loads below 500 fF. In the case of 500 fF output load, 9T shows huge improvement in terms of PDP in comparison to the other designed circuits. At 2 fF, 9T has better EDP than all other designed circuits. As shown in Figures 25 and 26, design 1 has lowest EDP in all output loads below 500 fF. In case of 500 fF output load, 9T has the lowest EDP. Design 2 shows improvement in terms of EDP in comparison to the other circuits at maximum load condition. At all output load values, 9T is better than design 1 in terms of EDP.

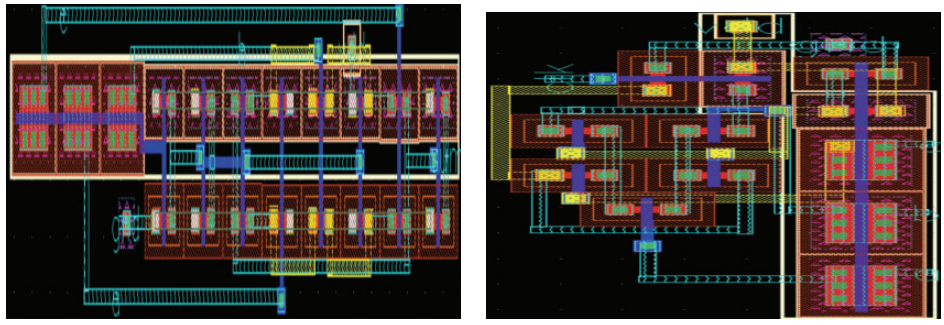
Table 7: Area comparisons of the XOR-XNOR-based adders.

Designs	CMOS	TGA	10T	9T	Design 1	Design 2
Length (μm)	17.5	14	11.2	10.1	15.5	15.2
Width (μm)	7.1	9.6	6.3	8.2	5.15	6.6
Area (μm^2)	124.2	135	71	82.8	80	100.3



(a) (b)

Figure 27: (a) Layout of design 1 (13T) full adder cell. (b) Layout of design 2 (16T) full adder cell.



(a) (b)

Figure 28: (a) Layout of design 1 (PMajFA1) full adder cell. (b) Layout of design 2 (PMajFA2) full adder cell.

Majority-function-based design 1 full adder (PMajFA1) is the best circuit in terms of power consumption for all values of output loads. The power of the designed circuits changes sharply by increasing the output load capacitance value at 1 V. At 2 fF load, Design 2 full adder (PMajFA2) is the fastest circuit. According to the simulation results, design 1 (PMajFA1) and design 2 (PMajFA2) has the lowest PDP among the other circuits for all output load capacitors as shown in Figure 26.

6.2. Layout and Area Analysis. With regard to the implementation area obtained from the layouts, it can be seen that the proposed full adders require the smallest area, which can also be considered as one of the factors for the lower delay and power consumption, as it implies smaller parasitic capacitances being driven inside the full adder. Table 7 illustrates that the layout of TGA full adders occupies the maximum silicon area. TGA adder is composed of transmission gates, which has more area due to the inefficient usage of the n-type wells. CPL adder needs the most number of metal lines to connect the complementary inputs. 10T adder has the lowest area because of the number of transistors, but the overall performance is inferior at low supply voltage (less than 1.4 V). The compact designed layout of the newly design full adders using 0.18 μm technology is all shown in Figures 27 and 28. The layout of the design 1 circuit occupies the least silicon chips area amongst all the simulated full adder cells that are performed well below 1 V. The schematic and layout editors are Cadence Virtuoso and Cadence Virtuoso XL, respectively, which are used for layout designing.

The values of layout circuit length, width, and overall area are listed in Table 7. Simulation layout results show that design 1 has the minimum power consumption due to the lowest area. 9T has minimum number of transistors but its area is much more due to the optimization of transistor parameter (W/L) which works at low voltage. Power consumption is lower than the 10T full adder and it can work up to 0.8 V satisfactorily. Design 2 has highest power dissipation when compared to the other designed full adder circuits. By

Table 8: Area comparisons of the Majority-function-based full adder cells.

Designs	MajFA1	MajFA3	MajFA4	PMajFA1	PMajFA2
Area (μm^2)	104.5	96	97	128	64

a perfect layouts design, more reduction in area is possible and more compact design will be implemented.

The compact designed layout of the newly design full adders using 0.18 μm technology are all shown in Figure 28. The layout of the design-2-Majority-function-based full adder circuit occupies less silicon area amongst all the simulated full adder cells that are performed well below 1 V. The value of layout circuit overall area of the conventional and newly designed full adder cells is listed in Table 8. Majority-function based Design 2 full adder (PMajFA2) has the lowest layout area.

7. Conclusion

An alternative internal logic structure for designing full adder cells is introduced. In order to demonstrate its advantages, four full adders were built in combination with pass-transistor powerless/groundless logic styles. Different adder logic styles have been implemented, simulated, analyzed, and compared. Using the adder categorization and hybrid-CMOS design style, many full adders can be conceived. As an example, new full adders designed using hybrid-CMOS design style with pass transistor are presented in this paper that targets low PDP. The hybrid-CMOS full adder shows better performance than most of the other standard full-adder cells owing to the new design modules proposed in this paper. The compared simulation result shows that the performance of the new designs is far superior to the other reference design of full adder circuits under different load conditions and for other simulation parameters.

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