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Research Article

9T Full Adder Design in Subthreshold Region

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This paper presents prelayout simulations of two existing 9T and new proposed 9T full adder circuit in subthreshold region to employ in ultralow-power applications. The proposed circuit consists of a new logic which is used to implement Sum module. The proposed design remarkably reduces power-delay product (PDP) and improves temperature sustainability when compared with existing 9T adders. Therefore, in a nut shell proposed adder cell outperforms the existing adders in subthreshold region and proves to be a viable option for ultralow-power and energy-efficient applications. All simulations are performed on 45 nm standard model on Tanner EDA tool version 13.0.

1. Introduction

Advances in CMOS technology have led to a renewed interest in the design of basic functional units for digital systems. The use of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been growing at a very fast pace. This trend is expected to continue, with very important implications for power-efficient VLSI and systems designs.

Digital integrated circuits commonly use CMOS circuits as building blocks. The continuing decrease in feature size of CMOS circuits and corresponding increase in chip density and operating frequency have made power consumption a major concern in VLSI design. Excessive power dissipation in integrated circuits not only discourages their use in portable environment but also causes overheating which reduces chip life and degrades performance.

Computations in these devices need to be performed using low-power, area efficient circuits operating at greater speed. The design of high-speed and low-power VLSI architectures needs efficient arithmetic processing units, which are optimized for the performance parameters, namely, speed and power consumption [1, 2].

Addition is one of the widely used fundamental arithmetic operations. In addition to its main task, which is adding two binary numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, and division. Full adder is an essential component for designing all types of processors, namely, digital signal processors (DSP), microprocessors, and so forth.

In most of the digital systems adder lies in the critical path that affects the overall speed of the system.

It is very important to choose the adder topology that would yield the desired performance. So enhancing the performance of the 1-bit full adder cell is the main design aspect.

One way to achieve ultralow is by running digital circuits in subthreshold mode [1, 2]. Subthreshold current of an MOSFET transistor occurs when the gate-to-source voltage (V_{GS}) of a transistor is lower than its threshold voltage (V_{TH}). When V_{GS} is larger than V_{TH}, majority carriers are repelled from the gate area of the transistor and a minority carrier channel is created. This is known as strong-inversion, as more minority carriers are present in the channel than majority carriers. When V_{GS} is lower than V_{TH}, there are less minority carriers in the channel, but their presence comprises a current and the state is known as weak-inversion. In standard CMOS design, this current is a subthreshold parasitic leakage, but if the supply voltage (V_{DD}) is lowered below V_{TH}, the circuit can be operated using the subthreshold current with ultralow-power consumption.

The proposed circuit operates efficiently in subthreshold region to achieve ultralow power. Results show improvement in temperature sustainability and PDP over the other adders

with comparable performance. The rest of the paper is organized as follows. Section 2 briefly describes the previous work reported in the literature. Proposed 9T Adder cell is described in Section 3. Section 4, presents the simulation results and conclusions are drawn in Section 5.

2. Prior Work

The full adder operation can be stated as follows. Given the three 1-bit inputs A, B, and Cin, it is desired to calculate the two 1-bit outputs Sum and Cout, where

$$\text{Sum} = A \oplus B \oplus \text{Cin}, \tag{1}$$

$$\text{Cout} = A \cdot B \ + \text{Cin}(A \oplus B). \tag{2}$$

The circuit shown in Figure 1 [3–5] is the schematic of modified 8T full adder cell [6–9] using an extra transistor M9 to improve the performance of the 8T full adder cell. The Sum output is basically obtained by a cascaded exclusive ORing of the three inputs in addition to an extra transistor M9. Cout is implemented using 2T multiplexer. 8T full adder is confronted with problems for certain input vectors. This problem is eliminated in the design of Figure 1 by adding an extra transistor M9. Although it has area overhead of one transistor, but still its power consumption is reduced than the 8T adder circuit. The outputs have good logic level only for certain input vectors. For the remaining input vectors, there is a major degradation in output voltage that may lead to functional failure as well as increased power consumption at higher voltages. An extra added transistor M9 remains ON for 010 and 100 input combinations also but does not contribute to produce Sum output and hence results into excess power consumption.

Figure 2 shows schematic of another 9T full adder design [10] reported in literature. In this circuit, a three-transistor XOR gate [6–9] and a multiplexer are used to implement Sum and one multiplexer to implement the Cout. The selector circuit of the output multiplexers is output of first-stage XOR. This circuit shows nominal improvements in power when compared with adder of Figure 1 in subthreshold region. The reason for less power consumption than the circuit of Figure 1 is shown in Table 2.

3. Proposed 9T Full Adder Design

The schematic of proposed 9T full adder cell is shown in Figure 3 and its truth table is stated in Table 1. The operating principle of proposed circuit is different from traditional circuits. For generating the Sum output in the proposed design, the truth table has been divided into two parts, one for input A = "0" and another for A = "1" rather than implementing the conventional Sum module of (1). From the truth table shown in Table 1 it is evident that when A = "0", Sum can be produced by XORing inputs B and Cin. Similarly, when A = "1", Sum is showing the XNORing between inputs B and Cin. Therefore, the operation of Sum module is based on implementing XOR operation and XNOR operation between inputs B and Cin which is indicated in (3) and (4). The logic for Cout output is stated in (5) and (6).

Table 1: Truth table of 1-bit full adder.

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

When $A = 0$,

$$\text{Sum} = B \oplus \text{Cin}. \tag{3}$$

When $A = 1$,

$$\text{Sum} = B \odot \text{Cin}. \tag{4}$$

For Cout, when $B \oplus \text{Cin} = 0$,

$$\text{Cout} = \text{Cin}. \tag{5}$$

When $B \odot \text{Cin} = 1$,

$$\text{Cout} = A. \tag{6}$$

An inverter is connected at the output of first-stage XOR gate to generate XNOR function. Finally the Sum is implemented by transferring these output levels through 2T multiplexer. Input to the PMOS (M6) of 2T multiplexer is XOR of B and Cin while to NMOS (M7) is XNOR of B and Cin. This 2T multiplexer is controlled by input A. Cout is implemented by using another 2T multiplexer which is controlled by output of first-stage XOR gate and passes either A or Cin accordingly. This circuit reduces the overall PDP at varying input voltages and operating frequencies and also improves the temperature sustainability while operating in subthreshold region. The most demanding design constraint for developing compact systems, that is, area, remains constant for all three designs.

Total power consumption in MOS logic circuits is expressed as sum of three components [2] as shown in (7):

$$P_{\text{Total}} = P_{\text{Switching}} + P_{\text{Sub}} + P_{\text{Short circuit}}, \tag{7}$$

where $P_{\text{switching}}$ denotes the average switching power consumption and is given by (8)

$$P_{\text{Switching}} = \alpha_T C_{\text{load}} V_{\text{DD}}^2 f. \tag{8}$$

Since no external load capacitance is connected in the circuit, hence total capacitance is only due to parasitic present in the design. Therefore at constant frequency and supply voltage, α_T (switching activity factor) will be the dominant factor which determines the total switching power of the circuit.

P_{Sub} denotes subthreshold power consumption and is given by (9)

$$P_{\text{Sub}} = V_{\text{DD}} \times I_{\text{Sub}}, \tag{9}$$

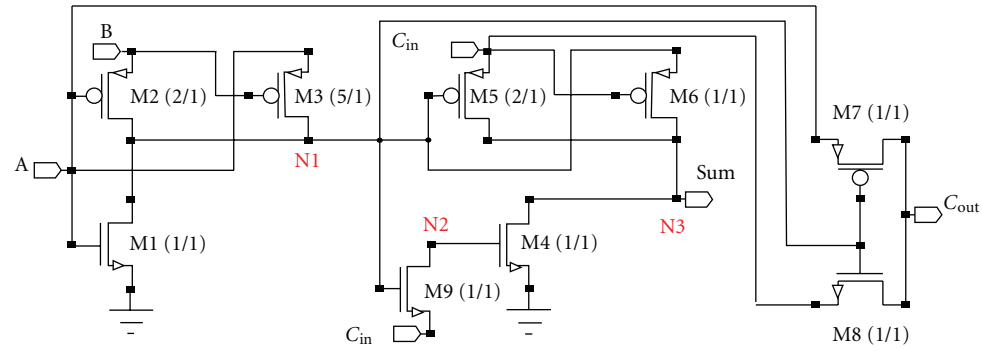

Figure 1: Existing 1-bit 9T full adder.

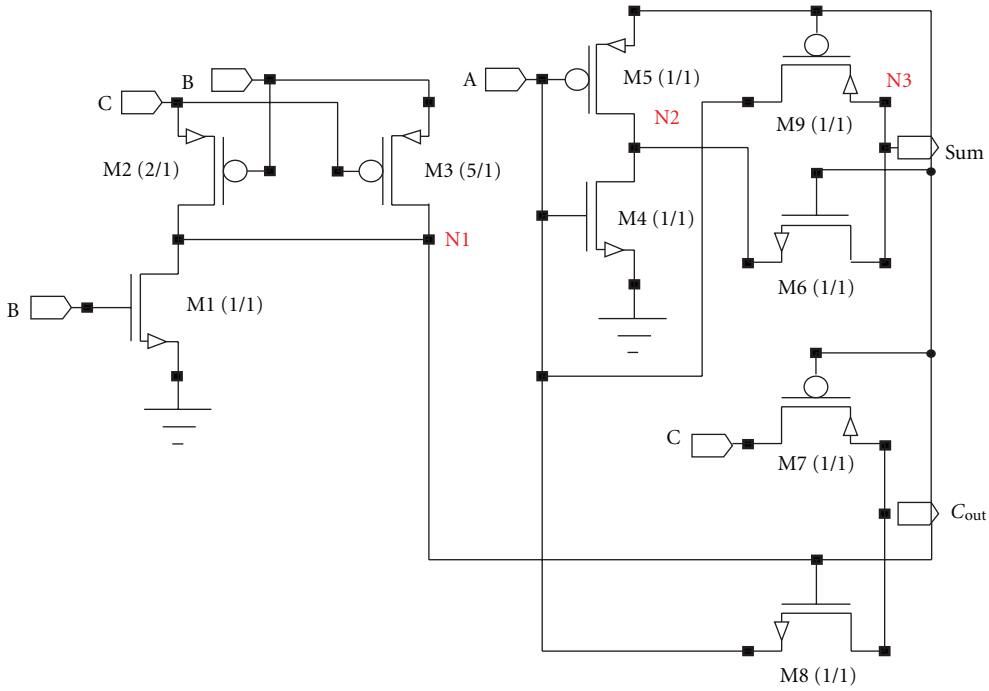

Figure 2: Existing 1-bit 9T full adder.

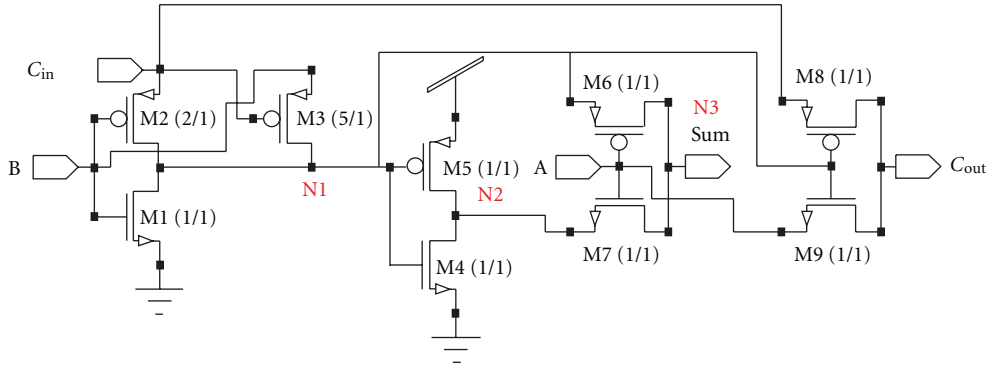

Figure 3: Proposed 9T full adder cell.

Table 2: No. of power consuming transitions at different internal nodes.

Figure 1			Figure 2			Proposed 9T (Figure 3)		
N1	N2	N3	N1	N2	N3	N1	N2	N3
1	4	3	1	3	3	2	2	3
Total = 8			Total = 7			Total = 7		

where

$$I_{\text{Sub}} = K \times \exp\left[\frac{(V_{\text{GS}} - V_t)q}{\eta KT}\right], \times \left[1 - \exp\left(V_{\text{DS}}\frac{q}{KT}\right)\right]. \quad (10)$$

As shown in (10), the reduced value of V_{GS} in subthreshold mode decreases current exponentially and thus reduces subthreshold power.

$P_{\text{Short circuit}}$ is due to the large rise and fall times of input voltage. But in all the designs included in this paper the default rise and fall time of 1 nsec has been taken for simulation which results into negligible short circuit power consumption.

The difference between existing and proposed designs is at Node N2 where the main logic has been implemented. In the proposed design, the power consuming transitions at node N2 are less than the existing ones. Table 2 shows the effective number of power consuming transitions at each internal node which lies in the path of Sum module.

As $P_{\text{Switching}}$ is proportional to α_T and the number of power consuming transitions at different nodes decides the value of α_T, therefore, reduction in number of power consuming transitions will result in reduced power consumption.

The previous description reveals the basic idea of the proposed technique. The data shown in Table 2 makes it evident that the number of power consuming transitions at node N2 where the proposed logic has been implemented results into low-power full adder cell.

In a nutshell, the proposed 9T full adder proves itself to be a better option for low-power compact systems. All the substrate terminals in Figures 1, 2 and 3 are connected to their respective source terminals in order to nullify the substrate-bias effect.

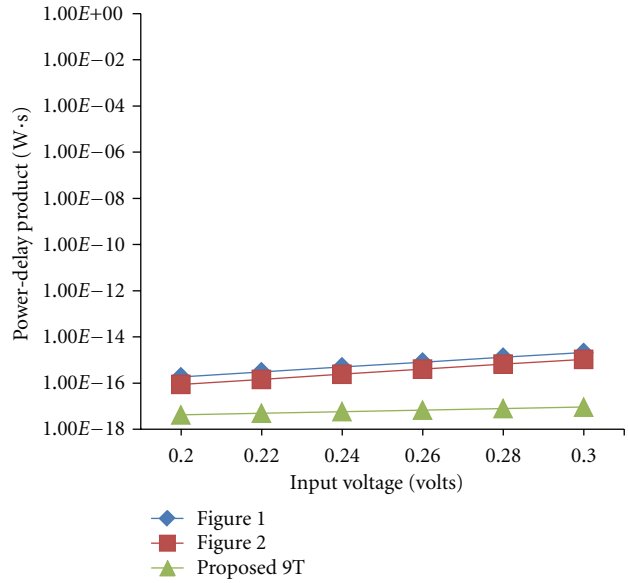

Figure 4: Power-delay product with increasing input voltage.

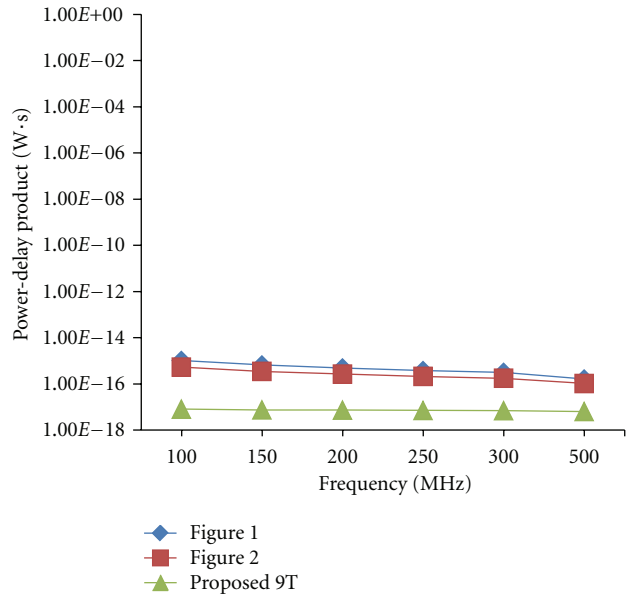

Figure 5: Power-delay product with increasing operating frequency at 0.3 V input voltage and supply voltage.

4. Simulations and Comparison

All schematic simulations are performed on Tanner EDA tool version 13.0 using 45 nm technology with input voltage ranges from 0.2 V to 0.3 V in steps of 0.02 V. In order to prove that proposed design is consuming low power and have high performance, simulations are carried out for power-delay product at increasing input voltage, operating frequency, and temperature. To establish an impartial testing environment all circuits have been tested on the same input patterns which covers each and every combinations of the input stream. From Figures 4, 5, and 6 it is evident that the performance of two existing adders is nearly same but the proposed adder is showing the difference at par. Also Figures 4, 5, and 6 reveals that the proposed 9T full adder cell proves its superiority in terms of power-delay product at different input voltages and frequencies and temperature sustainability over existing 9T adders. All these figures are plotted on logarithmic scale to show better view of comparison.

Equation (8) states that the increase in frequency will result into increased power consumption. But as power and delay are inversely proportional to each other, hence, the resulting PDP curve in Figure 5 is showing decreasing slope with increase in frequency.

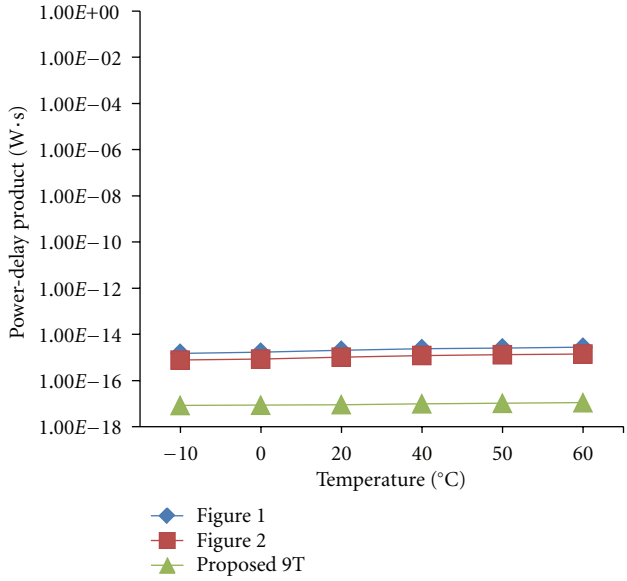

Figure 6: Power-delay product with varying temperature at 0.3 V input voltage and supply voltage.

The increase in temperature results into increase carrier mobility, and due to this random motion of electrons and holes will increase and hence more number of electron hole pairs will be formed in the interfacial region of the MOSFET thereby leading to delay in channel formation and increment in threshold voltage. This increment in threshold voltage will give rise to the power consumption of the device.

Also in a MOSFET, a pn junction is formed between the Drain/Source and Bulk of the transistor. The current equation of a pn-junction is expressed as

$$I = I_0\left(e^{qV/KT} - 1\right). \tag{11}$$

This states that with increase in temperature, current increases exponentially and results into more power consumption. This is the cause of slight rise in the curve of Figure 6 with increasing temperature.

5. Conclusion

Based on the subthreshold conduction region, the designing of a 1-bit full adder has been done. The proposed 9T 1-bit full adder is found to give better performance than both existing 9T full adders in subthreshold region. The proposed circuit has been tested to have better temperature sustainability and significantly less power delay product to achieve high performance. The proposed 9T adder has been designed and studied using 45 nm technology and can be a viable option for low-power complex circuit design.

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