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Research Article

High-Gain Power-Efficient Front- and Back-End Designs for a 90 nm Transmit-Reference Receiver

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A new microwave receiver configuration which transmits reference pulses embedded in data streams for synchronization is analyzed with a 90-nm IBM CMOS standard. A two-stage cascode low-noise amplifier (LNA) is proposed for the receiver front-end which is matched by a passive network to save on power-expensive matching techniques. The amplifier exploits a double-differential topology and achieves a below 4 dB noise figure near the center frequency. The overall 3-dB bandwidth is 3.3 GHz with S_{21} peaking up to 20.5 dB in the K-band. The back-end of the receiver is implemented through an adjustable analog window-detection circuit. It avoids the use of control voltage generators and sample-hold (S/H) blocks to save electronic overhead and is simulated with a 0.1~2.0 Gbps pulse stream. The achieved speed-to-power ratio for the back-end has a maximum limit of 266 GHz/W. When compared against simulated results of published literature, the proposed designs show improved performance in terms of small-signal gain, noise, speed, and power dissipation.

1. Introduction

The ultrawideband technology, with benefits like high data rate, low cost, and low complexity, has been considered as a promising initiative for short-distance wireless applications [1]. The main challenge of designing a wideband transceiver involves satisfying linearity, reverse isolation, gain, and noise requirements over a wide bandwidth. Different circuit techniques have been proposed in recent literature to achieve wideband operation for a radio-frequency (RF) front-end [2, 3]. Focus on the design of the back-end section of the receiver, on the other hand, has received relatively less attention. The wide variety of modulation and multiplexing techniques employed by the ultrawideband (UWB) system allow it to achieve high bit rates over a wide frequency range. For example, recent developments in UWB standards have proposed to exploit OFDM (orthogonal frequency division multiplexing), IR (impulse radio), and TR (transmit-reference) modulation techniques. Among them, IR-UWB is suitable for low rate applications (e.g., sensor network) and OFDM-UWB is more appropriate for high data rate transmission [4].

The idea of a transmit-reference (TR) system is that by injecting a reference pulse over the same channel as the information signal estimation of the channel model (to be directly used for convolution by a mixer) can be avoided. It is recognized that a TR system may face some limitations for a band-limited channel, but it allows data symbols to be decoded without direct calculation of multipath channel coefficients [5]. To realize this standard, efficient implementation is necessary for a millimeter-wave front-end low-noise amplifier (LNA) which immediately follows the receiving antenna and an RF multiplier (mixer) which correlates the received pulses with their delayed version [6]. As design requirements, this low-noise amplifier needs to provide reduced power consumption, low reflection (return) losses at peripheral ports, and reasonable forward gain. We aim to incorporate a double-differential topology for the LNA to provide less sensitivity to bias supply or common-mode noise, improved power supply rejection ratio, and a more linear behavior [7]. To complete the back-end section of the TR-receiver, a window comparator subcircuit with a current limiting mechanism is proposed which determines the final speed to power ratio at the receiver load-port.

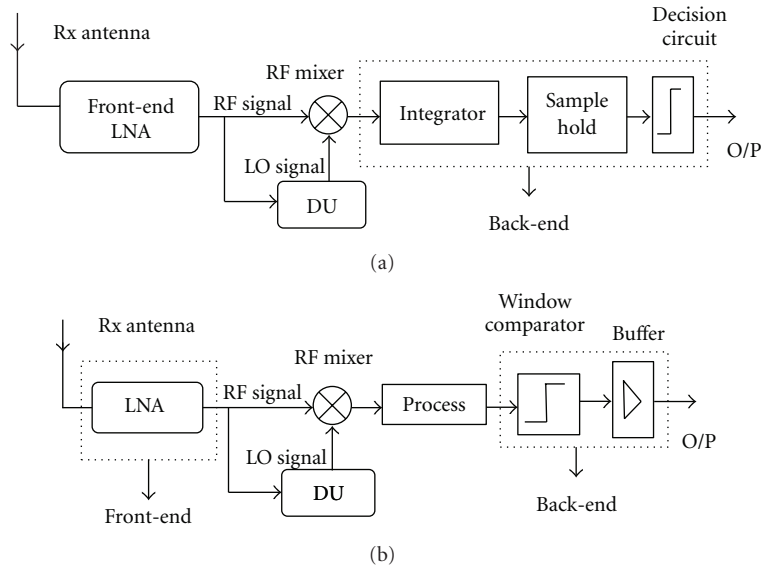


Figure 1: (a) Standard transmit-reference wideband receiver with an extended back-end (b) proposed TR-receiver architecture.

It avoids auxiliary electronic overheads in the form of control voltage generator and sample-hold blocks, therefore improving the overall performance of the transceiver.

To initiate the design of the receiver front-end, a high-gain two-stage cascode amplifier using a differential configuration is presented on an IBM .09-μm CMOS platform. The LNA operates in the K-frequency band with a 3.3 GHz bandwidth. Noise figure stays around 3.5 dB near the center point and the circuit is expected to be unconditionally stable according to Rollett criterion. Passive matching techniques are used at the interfacing ports to avoid area consuming transmission line matching. The amplifier is followed with a 90 nm threshold detection block using a separate control circuit to manipulate the ratio of integrated current mirrors. Its speed to power ratio ranges from 14 to 266 GHz/W as the input capacity is raised from 0.1 to 2.0 Gbps. The decision circuit dissipates only 7.5 mW of power (including bias circuits) and completes the implementation of the back-end part of a TR-receiver.

The paper is organized as follows. Section 2 introduces the proposed front- and back-end architectures of a TR-receiver. The operation of the microwave amplifier circuit and the design of the window comparator are discussed in detail in Sections 3 and 4, respectively. The results from the front-end amplifier and the decision circuit in the back-end occupy the focus in Section 5. Finally, Section 6 summarizes the performance of the designs and compares them with simulated examples from published literature.

2. Proposed TR Front- and Back-End Architectures

The microwave front-end including the feature of self-synchronization and the back-end with a decision block are presented in Figure 1(a) in the form of a traditional TR-receiver. For this architecture, a simplified transmitted TR frame typically consists of a "data pulse" modulated by signal message and a "reference pulse" necessary for synchronization. The two pulses are separated by a temporal displacement (delay) predefined during the design of the transceiver. This TR-receiver does not depend on direct estimation of the interchip channel and requires an architecture with a lower power demand. For Figure 1(a), demodulation is executed without obtaining channel state information and the scheme is resistant to distortion due to multipath propagation [6]. The transmitted signal passes through the channel for wireless interconnection and is received by the collecting antenna which relays it to a microwave front-end low-noise amplifier (LNA). The amplifier boosts the degraded signal while limiting the thermal noise accumulated in the front-end. The amplifier output (RF signal) and its delayed version (LO signal), produced by a specially designed delay unit (DU), are subjected as excitations to an RF mixer or correlator. This feature of self-synchronization reduces the receiver's architectural complexity but introduces the challenge of designing analog delay lines to align the LO signal with the amplifier output [8]. At the end of the front-end, the RF mixer facilitates the process of decoding the input data form the pulse stream. So, it is evident that the microwave LNA is a critical component for the receiver front-end of a TR scheme. It is also observed that a majority of RF LNAs reported in literature have been implemented with single-ended configurations [9–11].

The proof of the operation of the TR transceiver has been reported in detail in literature [12–16]. According to the model presented in [12], the signal of a TR scheme is grouped in individual message blocks. The length of each block is X where the number of "data pulses" and "reference pulses" are denoted by X_d and X_r, respectively. If T_f is the frame period of the standard, $n(t)$ is a gaussian white noise function,

$p(t)$ is the received pulse function, and d_i stands for the message stream, the received signal collected by the antenna in a TR scheme can be modeled with

$$r(t) = n(t) + \sum_{i=0}^{X_r-1} p\left(t - iT_f\right) + \sum_{i=0}^{X_d-1} d_i p\left\{t - (i + X_r)T_f\right\}. \quad (1)$$

Here the noise function has a spectral density of $N_o/2$ and $p(t)$ is calculated using the channel impulse response and the transmitted pulse function. If T_m is the delay suffered by a cluster m, $\tau_{m,n}$ is the delay of multipath n relative to the arrival of cluster m, and $\beta_{m,n}$ is the multipath gain factor, the channel impulse response in this case can be modeled with (in the absence of log-normal shadowing) [17]

$$h(t) = \sum_{m=0}^{M} \sum_{n=0}^{N} \beta_{m,n} \delta(t - T_m - \tau_{m,n}), \quad (2)$$

where M and N are the numbers of clusters and multipath for the distribution of clusters and signals. Here, the frame period has to be larger than the temporal spread introduced by the channel and the channel is assumed to be stationary according to the block fading assumption. At the end of the front-end, each data pulse is correlated with a template generated by the delay unit and the signal is passed to the back-end. A traditional approach to build the back-end section following the RF mixer would include the use of filters, a sample-and-hold block (S/H), and a separate decision circuit for threshold detection. This would necessitate the inclusion of control voltage generators for providing regulatory signals for integrator and sample-hold (S/H) sections. A separate circuit will also be needed to provide a calibrated reference voltage for driving the output decision circuit. If the output of the RF mixer does not have sufficient strength to drive the threshold detection section, further processing will be required before feeding the signal to the back-end. The aim of this paper is to propose an architecture which exploits a differential front-end and simplifies the circuit overhead of the receiver by implementing its back-end as an integrated comparator block.

Figure 1(b) shows the diagram of the proposed architecture for a transmit-reference receiver which employs a modified back-end section after the RF mixer. The front-end in this design is realized with a two-stage differential low-noise amplifier (LNA) with passive matching circuits. It makes the front-end compatible with differential topologies of the following RF mixer and improves the overall noise sensitivity of the receiver. The differential amplifier can also support direct connection to a double-balanced correlator and offers benefits like common-mode noise rejection with respect to substrate and power rail. Additionally, it has been reported that the differential architecture can influence the reduction of the second intermodulation product (IP_2) [18]. On the other hand, the proposed back-end uses a window comparator and reduces the receiver's electronic burden by substituting S/H blocks with logic and buffer sections. The comparator is built with a transconductance amplifier core with integrated bias circuits to deliver the comparator reference voltage and the gate voltage for a tail current source. It also includes a multiplication factor control block to regulate the width of the detection window and a logic section which delivers the output signal of the window comparator. The buffer block at the output of the back-end is implemented with a pair of cascaded inverters. The proposed TR-receiver front- and back-end circuits are discussed in detail in the next section.

3. Matched Front-End Low-Noise Amplifier

The proposed double-stage high-gain low-noise amplifier, which immediately follows the antenna in the receiver front-end (see Figure 1(b)), is presented in Figure 2. The circuit uses two back-to-back connected fully differential amplifier stages which allow it to exploit the advantages of the differential topology for a multistage amplifier. It employs a passive reactive Y-shaped matching circuit to provide it with input ($RF_{in_{1/2}}$), interstage, and load port matching. With the inclusion of these matching circuits, the amplifier achieves very low reflection losses (minimum return loss is better than -18 dB at the interfacing ports.) Matching also contributes to the improvement of the amplifier's noise figure following a mechanism described in [19]. The fully symmetric structure is expected to make the architecture more resilient against process variation for the 90 nm technology. Using an LC tuning circuit as the resonance bank provides the amplifier with the ability to fine tune its center frequency. The inclusion of multiple integrated bias circuits leads the LNA to be driven by a single supply voltage (1.2-V). It manages a high small signal forward gain with the double-stage core and careful selection of bias currents provides it with simultaneous power and noise matching. The architecture will be compatible with a fully differential TR front-end where the RF mixer can be built with a double-balanced topology. The amplifier includes features like improved linearity (because of cancelation of intermodulation products), is more resistant to power supply noise, and supports the use of image rejection schemes, dipole antenna, and Gilbert mixers.

To maintain design symmetry for the first block of the design, T_{11} with T_{21} ($60\,\mu/0.1\,\mu$) play the role of driving transistors and T_{12} with T_{22} ($50\,\mu/0.1\,\mu$) insulate the second stage from the driving input. The central operating point of the front-end built with this cascode configuration is determined by $L_{d.12}$ and $L_{d.22}$ in the first block, which form a pair of resonance tanks in conjunction with associated capacitances. The resistive elements in the tanks ($R_{d.12}$ and $R_{d.22}$) do not represent independently inserted components but model for parasitic contributions from adjoining tuning inductors. To include a provision of fine tuning, parallel capacitors are also included in the tanks in the form $C_{r.12}$ and $C_{r.22}$. A source degenerating port matching network (built with $L_{s.11}$ and $L_{g.11}$) adjusts the input impedance offered by T_{11} while $C_{\text{in}.11}$ works as a coupling capacitor. An LC matching branch is also placed at the input port of T_{21}. To ensure a smooth transition of signal and to save on power penalty and noise contribution, a secondary passive linking network

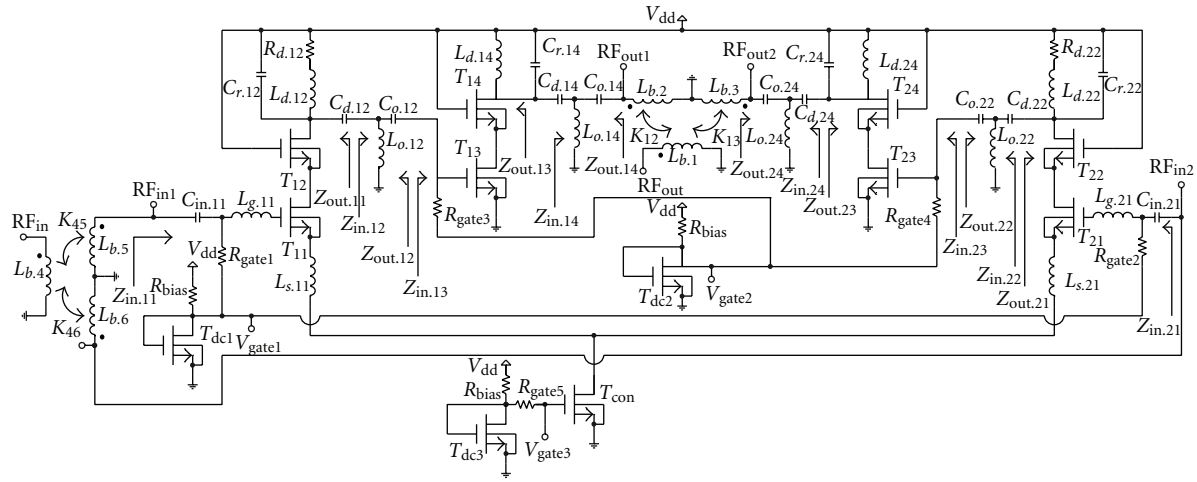


Figure 2: The double-differential matched wideband low-noise front-end with a tail source and two bias circuits.

joins the intermediate nodes between the two stages. It is made with $C_{d.12}$, $C_{o.12}$, and $L_{o.12}$ for the left-half segment of the amplifier. $C_{o.22}$, $C_{d.22}$, and $L_{o.22}$ provide a similar service for the second set of intermediate differential nodes located on the right-half of the design. The linking circuits ensure that additional input matching networks are not necessary for the second stage of the differential amplifier, leading to a boost in the overall amplifier gain. The two cascode trees in the second stage are made with $T_{1(3/4)}$ ($50\,\mu/0.1\,\mu$ and $40\,\mu/0.1\,\mu$) and $T_{2(3/4)}$ (similar dimensions). They closely follow the size of the devices in the first block except for process variation. The reactive elements in the secondary resonating banks ($L_{d.14}$, $L_{d.24}$, and $C_{r(1/2)4}$) are carefully matched with their counterparts in the first stage to maintain a stable operating point. Finally, T-shaped passive matching circuits (previously placed with intermediate nodes) are also utilized for the differential load ports ($RF_{out.1}$ and $RF_{out.2}$) to interface them with typical microwave loads that may follow. The components in the load matching circuits are designated as $C_{o.14}$, $C_{d.14}$, $L_{o.14}$, and like. A tail transistor (T_{con}) is added with the bottom rail of the first stage to exert control over the overall bias current which is split between the differential half circuits. The tail current controlling arrangement is not repeated for the second block for easier manipulation of the bias current. The gate bias supply for the control device (V_{gate3}) and the gate signals for the driving transistors (V_{gate1} and V_{gate2}) necessitate inclusion of three bias circuits to push the concerned transistors in a region of saturation. This three-way supply rail is also included in Figure 2, built with diode-connected devices T_{dc1} ($2\,\mu/1\,\mu$), T_{dc2} ($2\,\mu/1\,\mu$), T_{dc3} ($4.7\,\mu/1\,\mu$), and bootstrapping resistors (R_{bias}). For a 1.2-V 90-nm process, V_{gate1}, V_{gate2}, and V_{gate3} are set to 0.851, 0.851, and 0.699 V, respectively. An interfacing balun (balanced-unbalanced) circuit is placed at the $RF_{in.1/2}$ ports during simulation to interface the front-end with the antenna that feeds it. Three ideal coils ($L_{b.4-6}$) in a transformer formation facilitate this balanced to unbalanced conversion with coupling parameters $K_{45/46}$. If we define a quality factor for the input network [20] appended with T_{11} (excluding coupling capacitors), it will be a function of source impedance (Z_s) and operating frequency (ω_o) while relating to the gate-source capacitance ($C_{gs.11}$) of the transistor T_{11}:

$$Q_{inp.11} = \frac{\omega_o\left(L_{g.11} + L_{s.11}\right)}{2Z_s} \approx \frac{1}{2Z_s\omega_o C_{gs.11}}. \tag{3}$$

This quality factor has to be optimized to balance gain and bandwidth achieved by the first stage of the amplifier. In the resonance tank formed on top of T_{12}, the quality factor of the reactive element ($Q_{d.12}$) will ultimately determine the inductor's series resistance ($R_{d.12}$) which can be approximated by

$$R_{d.12} \approx \omega Q_{d.12} L_{d.12}. \tag{4}$$

Therefore, this undesirable resistive element can be minimized by selecting a reasonable value for the drain inductor. The designer also has to be careful about large quality factors achieved at microwave frequencies, which can push up the resistive value of $R_{d.12}$ [21]. For the 90-nm CMOS process (with the presence of parasitic junction capacitors) the output resistance offered by the cascode device (T_{12}) has low to moderate values like

$$R_{o.T_{12}} \approx 100 \sim 800\,\Omega. \tag{5}$$

The effective output resistance ($R_{out.12}$) seen from the load port of the first stage amplifier can be estimated using the adjoining resistive components with

$$R_{out.12} = R_{d.12} \,||\, R_{o.T_{12}}. \tag{6}$$

The quality factor seen by a load connected to the first stage can, therefore, be simplified as

$$Q_{op.12} = \frac{R_{out.12}}{\omega L_{d.12}}. \tag{7}$$

Tuning of the controlling parameters of this quality factor would influence the overall gain achieved by the first block of the double-differential amplifier. A very small $L_{d.12}$ would increase $Q_{\text{op.12}}$ and, as a consequence, message bandwidth and gain of the LNA may suffer [20]. To set the operating point in the K-band, the bank inductor ($L_{d.12}$) resonates with $C_{r.12}$ and an output capacitive element $C_{o.\text{total}}$ which can be calculated with

$$C_{o.\text{total}} = C_o + C_{\text{coup}} + C_l + C_{\text{par}}, \tag{8}$$

where C_o is the cascode capacitance seen from the drain of T_{12}, C_{par} represents extraneous parasitic elements existing between that node and ground, C_l is the capacitance offered by a following stage (load), and C_{coup} stands for the output coupling capacitance. So, all these considerations have to be taken into account during the design of the low-noise amplifier. After careful selection of the reactive elements for gain-bandwidth optimization, the input impedance of the amplifier [7] looking from the gate terminal of the transistor T_{11} can be derived as

$$Z_{\text{in.11}} = \frac{g_{m.11}L_{s.11}}{C_{\text{gs.11}}} + j\left[\omega\left(L_{s.11} + L_{g.11}\right)\right] - \frac{1}{\omega}\left(\frac{1}{C_{\text{in.11}}} + \frac{1}{C_{\text{gs.11}}}\right), \tag{9}$$

where $g_{m.11}$ is the transconductance of the transistor T_{11}. The dimensions of $L_{s.11}$, $L_{g.11}$, $C_{\text{in.11}}$, and the aspect ratio of T_{11} are manipulated to eliminate the imaginary part of the expression (as part of input matching) which reduces the equation and matches it with characteristic source or antenna resistance (R_{ant}),

$$Z'_{\text{in.11}} = \frac{g_{m.11}L_{s.11}}{C_{\text{gs.11}}} = R_{\text{ant}} = 50\,\Omega. \tag{10}$$

For the output matching circuit located on the left segment of the amplifier [22] (see Figure 2), the impedance $Z_{\text{in.14}}$ can be derived as

$$Z_{\text{in.14}} = -jX_{C_{d.14}} + \left(jX_{L_{o.14}}\right) \,||\, \left(R_{\text{Load}} - jX_{C_{o.14}}\right), \tag{11}$$

where $X_{C_{d.14}}$, $X_{C_{o.14}}$, and $X_{L_{o.14}}$ represent measures of reactance and R_{load} is offered by the circuit block which follows the low-noise amplifier in the receiver. Now the expression can be reduced to

$$Z_{\text{in.14}} = \frac{X_{L_{o.14}}^2}{R_{\text{Load}}} + j\left(X_{L_{o.14}} - X_{C_{d.14}}\right) \tag{12}$$

if the parameters are manipulated to equalize $X_{L_{o.14}}$, $X_{C_{d.14}}$, and $X_{C_{o.14}}$. The design equation which makes $Z_{\text{in.14}}$ equal to the first-stage output resistance (R_o) will be

$$X_{L_{o.14}} = \sqrt{R_o R_{\text{Load}}}, \tag{13}$$

where R_o is the real element of the port impedance $Z_{\text{out.13}}$. As an example, when $R_{\text{Load}} = 50\,\Omega$ and $R_o = \text{Re}\{Z_{\text{out.13}}\} = 186\,\Omega$ near the center frequency for the proposed design, if we set $X_{L_{o.14}} = X_{C_{d.14}} = X_{C_{o.14}} \approx 97\,\Omega$, then following (13) should result in $Z_{\text{in.14}}$ being equal to R_o and $Z_{\text{out.14}}$ being matched with R_{Load} (see Figure 2). A similar matching mechanism is also executed through a reactive network connected with the node RF_{out2} which is made with $L_{o.24}$, $C_{d.24}$, and $C_{o.24}$.

Noise figure contributed by the driving transistors (T_{11} and T_{21} for the first stage) of a differential amplifier has been modeled in literature [23] and is expressed in terms of quality factor of the input network ($Q_{\text{inp.11}}$), transit point (ω_T), and center frequency (ω_o):

$$\text{NF}_{\text{stage.1}} = 1 + \frac{\sigma}{\xi}\left[\frac{1}{Q_{\text{inp.11}}} - 2\left|c_{\text{gd}}\right|\sqrt{\frac{\xi^2\delta}{5\sigma}}\frac{1}{Q_{\text{inp.11}}} + \frac{\xi^2\delta}{5\sigma}\frac{\left(1 + Q_{\text{inp.11}}^2\right)}{Q_{\text{inp.11}}}\right]\frac{\omega_o}{\omega_T}, \tag{14}$$

where ξ is defined by zero-bias drain-conductance and device trans-conductance, c_{gd} correlates drain and gate noise functions, σ models channel noise, and δ models noise induced at gate terminal. If it is possible to partially cancel out the third and fourth components in (14), the expression for minimum noise figure (applicable for FET amplifiers) can be approximated by

$$\text{NF}_{\text{stage.1}_{\text{min}}} \approx 1 + 2.4\frac{\sigma}{\xi}\left(\frac{\omega_o}{\omega_T}\right). \tag{15}$$

If the effect of the cascode device in the first stage (T_{12}) is considered, the cascode noise-factor ($\text{NF}_{\text{stage.1}_{\text{cas}}}$) will be proportional to device transconductance ($g_{m.12}$) [24]

$$\text{NF}_{\text{stage.1}_{\text{cas}}} \propto \left(\frac{\omega_o^2 C_{\text{par.12}}}{\omega_T g_{m.12}}\right)^2, \tag{16}$$

where $C_{\text{par.12}}$ denotes the parasitic capacitance linking the two stages of the amplifier. Finally, an output balun block will be necessary to interface the amplifier if the following mixer or another front-end component is single-ended. The three reactive elements for the RF_{out} port balun are denoted by $L_{b.1-3}$, supported with carefully selected linking parameters ($K_{12/13}$). In this arrangement, the bias supply is set to 1.2 V for process requirements.

4. Back-End Architecture

The proposed decision section for a TR-receiver back-end is driven by a window detector with output logic and buffer gates, thus relaxing the overhead requirements for the receiver design. The symmetric nature of the decision circuit makes it resilient with respect to variation of process. The controlling voltage of the tail current source in the design and the reference voltage of the comparator are provided with integrated diode connected bias circuits. The inclusion of multiple bias arrangements allows the back-end to be driven by a single supply rail (1.2-V) which eliminates the need for external gate supply voltages. Optimization of the bias

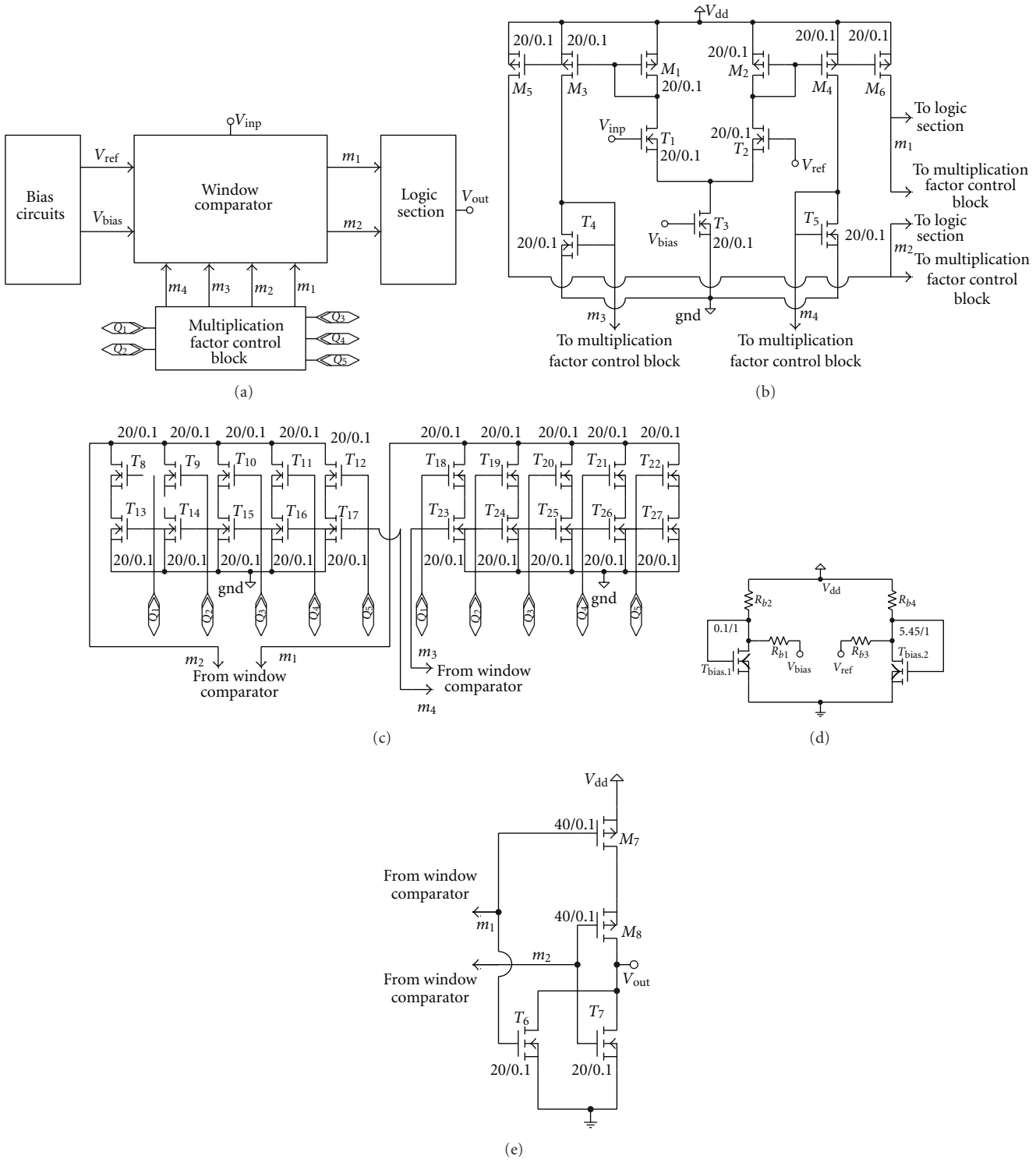


Figure 3: (a) Functional block diagram of the proposed back-end section (schematics of its different parts are shown in the subfigures) (b) window decision circuit (c) multiplication factor control block (d) bias circuits for gate and reference voltages (e) output logic section.

currents for the comparator reduces their power requirement with respect to comparable analog detection circuits. The architecture of the receiver back-end is simplified by avoiding sample-hold blocks and using logic sections and buffer gates. This reduces the electronic burden on the comparator's transconductance amplifier core and pushes down its power demand even further. The window of detection for the decision circuit can be controlled by multiple design parameters, one of which is influenced by a multiplication factor control block with external switching signals.

Analog window comparators have primary applications in testing of controlled systems and they typically capture multiple analog inputs to produce the output in a decoded format. They are called window detectors because they respond when the difference between the two excitations of the decision circuit is within the range of $[-e_{\text{thres}}, e_{\text{thres}}]$, with e_{thres} being the detection threshold for the comparator [25]. The proposed decision section, shown as a functional block diagram in Figure 3(a), is built on a differential input core, a number of current mirrors and a tail current source (the window decision circuit in Figure 3(b)), a mirror factor controlling block (Figure 3(c)), two bias supplies (Figure 3(d)), and an output logic section (Figure 3(e)). Transistors T_1 and T_2 $(20\,\mu/0.1\,\mu)$ constitute the input differential pair where V_{inp} represents the input signal (driving excitation) coming from an RF multiplier in the TR-receiver and V_{ref} denotes a calibrated reference voltage for the decision circuit. So, the input network of the window comparator resembles a differential transconductance amplifier core. If the input voltage (V_{inp}) falls in the vicinity of the threshold level (i.e., it is within the range $V_{\text{ref}} \pm e_{\text{thres}}$), the logic section implemented by transistors T_6, T_7 $(20\,\mu/0.1\,\mu)$, and M_7, M_8 $(40\,\mu/0.1\,\mu)$ produces a positive response in terms of output voltage. As a result, the comparator is able to detect whether the input signal falls within a particular window around the reference voltage or not [26]. If the tail bias current flowing through the design is I_{tail}, when both comparator excitations are sufficiently at the same level (V_{inp} equals V_{ref} or resides within the range $V_{\text{ref}} \pm e_{\text{thres}}$), transistors T_1, T_2, T_4, T_5, and $M_1 \sim M_6$ $(20\,\mu/0.1\,\mu)$ remain in a region of saturation. A split current ($I_{\text{tail}}/2$) flows through the transistors which depends on the dimensions of current mirrors. The tail current source is implemented by a device (T_3, $20\,\mu/0.1\,\mu$) attached to the bottom power rail and powered by a gate bias supply. The two bias circuits in the design (see Figure 3(c)) are developed by diode connected transistors ($T_{\text{bias.1}}$, $0.1\,\mu/1\,\mu$ and $T_{\text{bias.2}}$, $5.45\,\mu/1\,\mu$) which deliver calibrated dc voltages V_{bias} for T_3 and V_{ref} for T_2. $R_{b(1-4)}$ represent low to moderate values of impedance which ensure that V_{bias} remains at a value near the bias rail (V_{dd}) and the reference level (V_{ref}) can be fine tuned within the 0.6–1.2 V range using device dimensions (1–10 μm as width of T_{bias2}). Four p-type current mirrors are implemented by transistors M_3–M_6, all following a unity mirror factor. The n-type current mirrors introduce a regulating mirror factor (N_{mir}) as a way of controlling the width of the detection window. The first n-type mirror is formed by T_4 $(20\,\mu/0.1\,\mu)$ and T_{18}–T_{27} (variable dimensions) which split the bottom current path in five ways so that N_{mir} can be adjusted by the designer. Inclusion of switching signals (Q_1–Q_5) for the devices T_{18}–T_{22} turns it into a programmable current mirror which can be controlled by an external driving circuit. A similar extended mirror circuit is realized by the devices T_5 and T_8-T_{17}, also driven by a 5-bit input signal. The N_{mir} factor can be compounded (raised above 5) by adjusting the dimensions of the control transistors (T_8–T_{27}) as multipliers of the width of $T_{4/5}$. When the input voltage and the reference level are not in close proximity, currents flowing through devices T_1 and T_2 become $I_{\text{tail}}/2+i$ and $I_{\text{tail}}/2$-i or vice versa with i depending on the difference between the two inputs. The expression for the detection window width of the comparator ultimately takes the form of [25]:

$$e_{\text{thres}} = \sqrt{\frac{I_{\text{tail}}}{\mu_n \cdot C_{\text{ox}} \cdot (W/L)_{1/2}}} \sqrt{1 - \sqrt{1 - \left(\frac{N_{\text{mir}} - 1}{N_{\text{mir}} + 1}\right)^2}}, \tag{17}$$

where μ_n is the carrier mobility, I_{tail} is the tail current, C_{ox} denotes the gate capacitance per unit area, N_{mir} is the current mirror factor, and $(W/L)_{1/2}$ indicates the aspect ratio of T_1 or T_2. Because of the resemblance of the input pair of the comparator section with a differential transconductance ($g_{m_{1/2}}$) amplifier, its gain-bandwidth product ($g \cdot bw$) will depend on the input pair's effective load capacitance (C_{load})

$$\begin{aligned} g \cdot bw &= \frac{g_{m_{1/2}}}{2\pi C_{\text{load}}} \\ &\approx \frac{\mu_n C_{\text{ox}} (W/L)_{1/2} V_{\text{eff}}}{2\pi m_{\text{load}} \{WL\}_{1/2}} \\ &= \left(\frac{\mu_n C_{\text{ox}}}{2\pi m_{\text{load}} L_{1/2}^2}\right) V_{\text{eff}}, \end{aligned} \tag{18}$$

where m_{load} is a constant depending on load capacitance and V_{eff} is the overdrive voltage defined by

$$V_{\text{eff}} = V_{\text{gs}} - V_{\text{thres}}. \tag{19}$$

Here V_{gs} and V_{thres} are the input signal and the threshold voltage for the input differential pair, respectively. The $g \cdot bw$ factor for the decision circuit is optimized to fine tune the detection window. The bias rail (V_{dd}) may be connected with at least two of the switching combinations (Q_1–Q_5) to maintain a nominal value for N_{mir} (=2). Here, it is assumed that the relation between the output current and the input voltage of the two input transistors follows the standard equations of saturation region.

As indicated by the threshold expression, the detection window can be adjusted by changing the bias current I_{tail} which, in turn, is controlled by the voltage V_{bias} and the transistor T_3. As carrier mobility (μ_n) and gate capacitance (C_{ox}) are intrinsic device parameters, the other controlling factors of the error threshold are the multiplying factor of the tail current mirrors (N_{mir}) and the size of the input differential pair $(W/L)_{1/2}$. The gate biasing voltages in the comparator are provided by biasing arrangements already discussed in relation to Figure 3(d) where voltages are collected from the drain terminals of $T_{\text{bias}_{1/2}}$. To evaluate the performance of the back-end, characterization of the window detector [26] is performed in detail in the next section and the responses from the decision block for TR inputs are discussed.

5. Results and Discussion

5.1. Front-End LNA. The proposed design is analyzed on an RF simulator including layout parasites generated by the 90-nm circuit elements to enable accurate prediction of

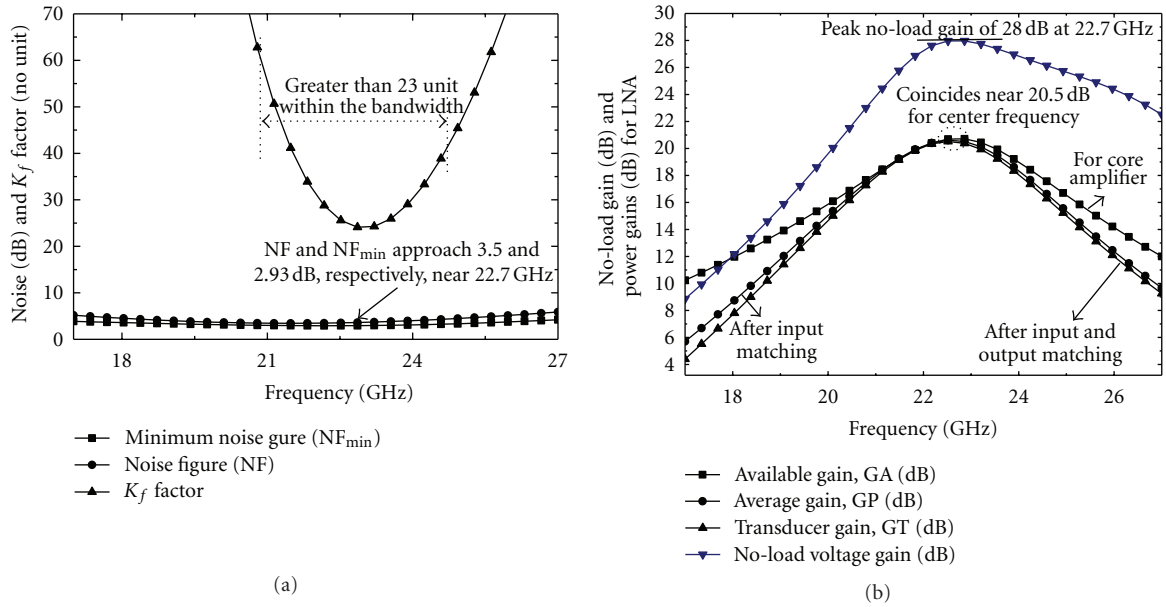


Figure 4: (a) Noise parameters (NF and NF_{min}) and K_f factor (b) power gains and no-load voltage gain achieved by the unmatched core and the matched amplifier.

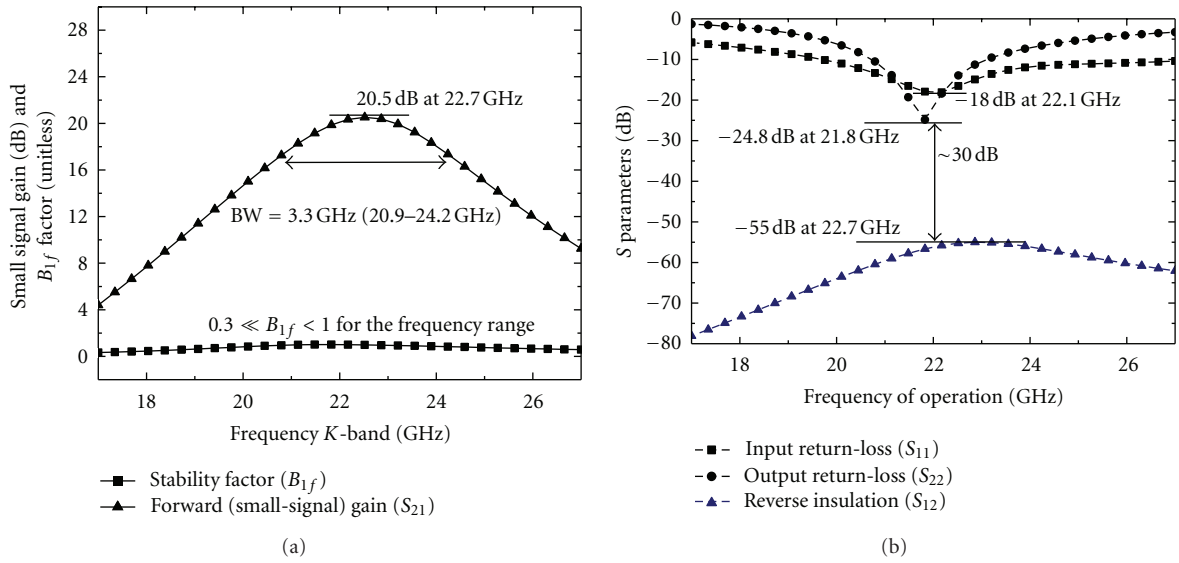


Figure 5: (a) Stability factor (B_{1f}) and forward gain (S_{21}) around the center frequency (b) reverse isolation (S_{12}) and return-loss (S_{11} & S_{22}) parameters.

microwave parameters during an RF analysis. In the first phase, the design parameters of the wideband low-noise amplifier are obtained on the 0.09-μm CMOS platform to evaluate power efficiency and gain performance of the proposed front-end.

5.1.1. Noise Performance. The projected noise figure (NF) and theoretical noise figure (NF_{min}) contributed by the front-end amplifier are documented to be around 3.5 and 2.93 dB, respectively, near the center frequency of the message bandwidth, as shown in Figure 4(a). In total, the driving transistors (T_{11}, T_{21} in the front stage, T_{13}, T_{23} in the second block) are responsible for about 23% of the total accumulated noise and the percentage contribution is slightly lower for the insulating devices.

5.1.2. Propensity of Oscillation. The low-noise amplifier is expected to be unconditionally stable within the bandwidth as the Rollette stability factor (K_f), plotted versus frequency in Figure 4(a), is always greater than 23 within the bandwidth, hence satisfying the criteria for nonoscillatory

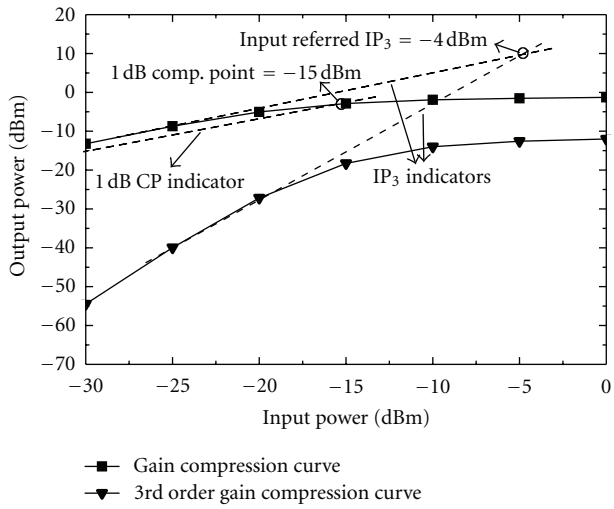


FIGURE 6: Linear behavior of the amplifier {1-dB compression point (1 dB-CP) and 3rd order intermodulation product (IP_3)}.

behavior [7]. This factor K_f is defined in terms of S-parameters:

$$K_f = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{21}||S_{12}|}. \quad (20)$$

Therefore, the LNA is not prone to oscillating in the presence of unwanted noise or interference.

5.1.3. Power and No-Load Gains. Available gain (GA), transducer gain (GT) and average power gain (GP) coincide around the center frequency at 20.5 dB in Figure 4(b). This coincidence can be attributed to the matching networks included in the design. Available gain is an estimation of the power gain provided by the core amplifier without any matching, which is then lowered down to transducer gain after the addition of passive linking networks at intermediate and interfacing ports of the front-end. The no-load voltage gain of the amplifier reaches a higher limit with its peak touching 28 dB, as shown in the same figure.

5.1.4. S_{21} and Stability Factor. Figure 5(a) shows the maximum small-signal forward gain (S_{21}) with a peak of 20.5 dB at the central operating point, managing a 3.3 GHz three-decibel bandwidth. To verify a second criterion for stability, the B_{1f} stability factor is also calculated for the amplifier and it resides within a range denoted by the inequality $0.3 < B_{1f} < 1$. The standard definition of the secondary factor (B_{1f}) is given with

$$B_{1f} = 1 + |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2. \quad (21)$$

5.1.5. Input/Output Return Loss. Figure 5(b) verifies that the parameter representing reverse isolation (S_{12}) is always better than −55 dB within the bandwidth. As a measure of return losses incurred at the front-end ports, the same frame plots the input and output reflecting parameters (S_{11} & S_{22}) showing dips at −18 dB and −25 dB, respectively, and maintaining a separation of 30 dB with the peak of the amplifier's reverse isolation.

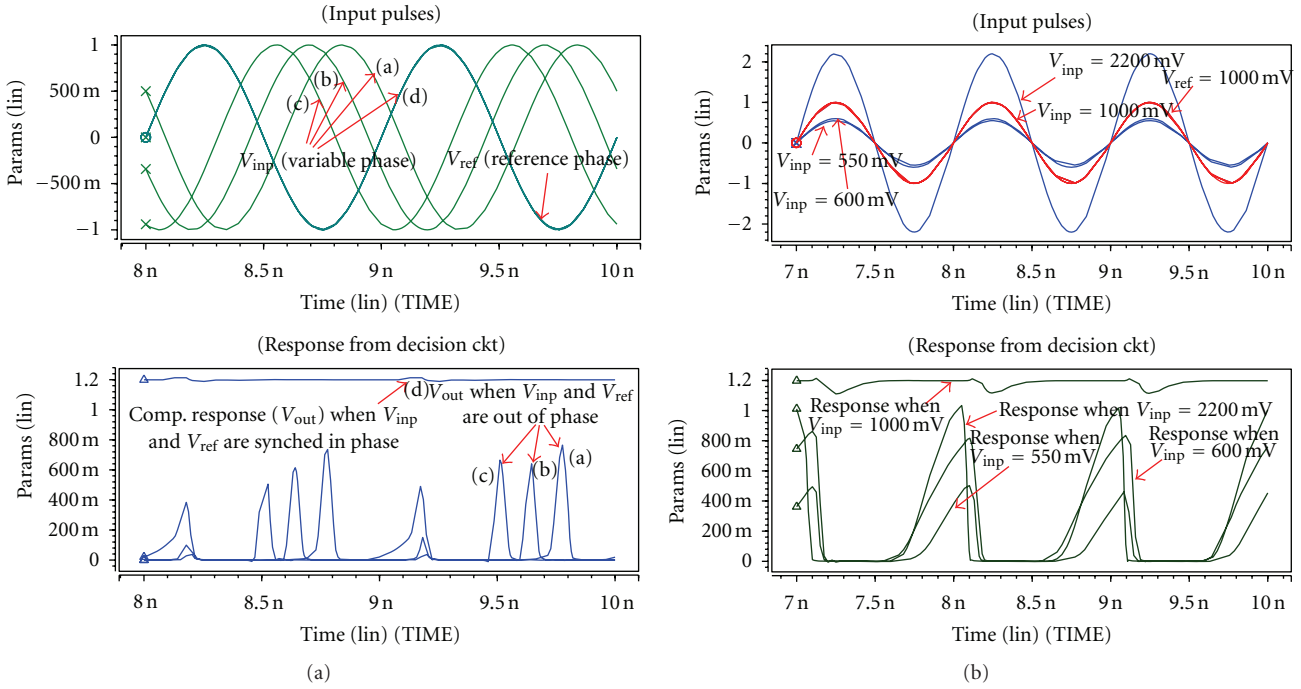
5.1.6. Region of Linear Behavior. The input referred 1-dB compression point (1 dB-CP) is crossed by the LNA at $-15\,\text{dB}_m$ of input power which pushes the amplifier into a region of nonlinearity (see Figure 6). The 3rd order intersecting point for intermodulation products (IP_3) settles near $-4\,\text{dB}_m$ with respect to input power (theoretically, it should have a difference of 10 dB with 1 dB-CP). At this cross point, the front-end would deliver $10\,\text{dB}_m$ power to a matched load connected with the output port.

5.2. Window Detector in the Back-End. The results from the decision section (window detector with buffer gates, as discussed in Section 4) implementing the back-end of the TR-receiver are also obtained with 90-nm process parameters on a CMOS platform.

5.2.1. Dynamic Response. In an effort to study the dynamic behavior of the proposed back-end, the input at the reference port of the comparator block is tied with a zero-phase sinusoid and the signal port (V_{inp}) is exited with a pulse of variable phase (0∼360 degrees). The corresponding response in Figure 7(a) detects a driving signal positively (high) only when the two phases follow each other. With an increase in phase difference, the circuit response starts to resemble nonuniform pulse peaks.

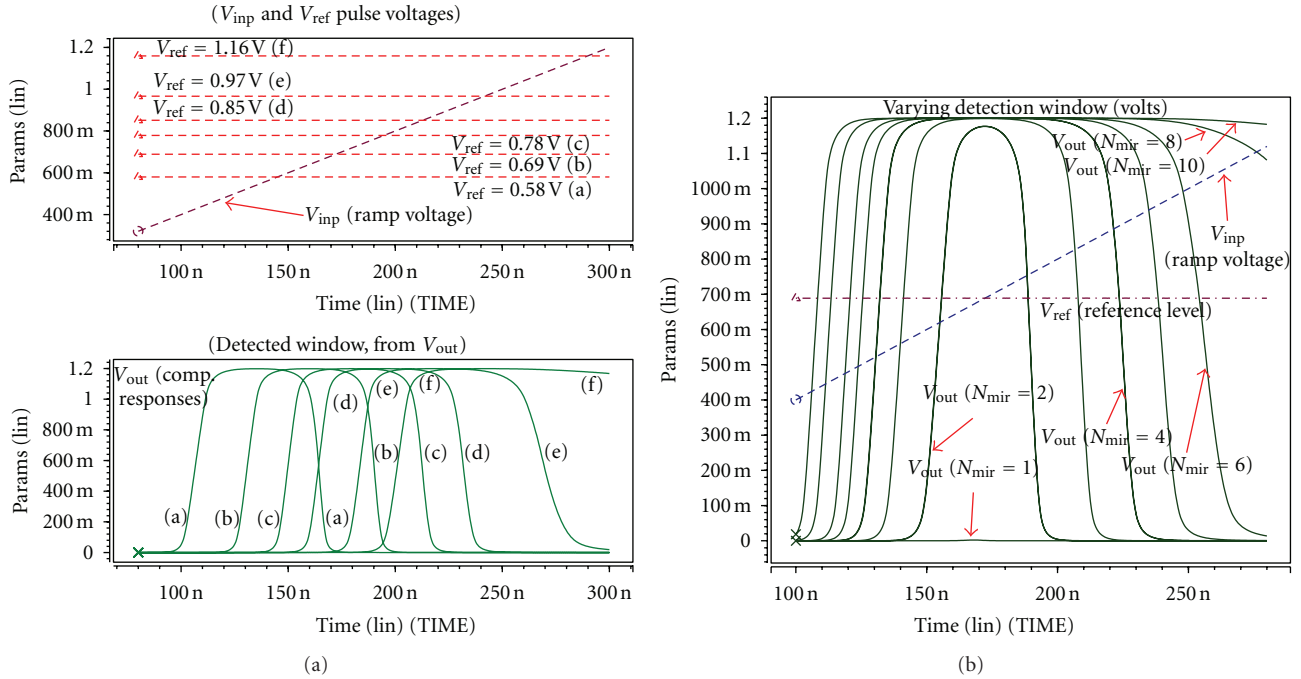
5.2.2. Behavior for Variable Amplitude. Both input ports of the detection subcircuit are tested with a number of combinations of frequency and magnitude for the input sinusoids. With a fixed reference level (settled at 1000 mV), the signal port is tied to a sinusoid whose amplitude is raised in steps from 500 to 2500 mV. Figure 7(b) demonstrates that, with an increase in the difference of magnitude between the two excitations or for signals existing outside the detection window, the magnitude of the amplitude response fails to reach the level which is achieved when the strengths of V_{inp} and V_{ref} are matched.

5.2.3. Setting the Reference Level. As the first step of performing static characterization for the detection unit, the operating point of the window detector (V_{ref}) is manipulated by setting the reference level with variable dc voltages (within 0.5∼1.2 V). The V_{inp} port is fed with a ramp (linearly increasing) source and corresponding output voltages are plotted for different combinations of the two inputs. The shape of the response in Figure 8(a) suggests a dependence of the detection window on the strength of reference level. For example, when V_{ref} is tied to 0.69 V the detectable range for the input is uniform and approximated by 0.55∼.78 V. In this case, the detection window is not perfectly symmetric around the reference level and the asymmetry may increase for wider ranges for the window. As for V_{ref} = 0.97 V, the window covers the domain of 0.76–1.12 V and for V_{ref} = 1.16 V, the window becomes open ended at one side.



(a) (b)

Figure 7: (a) Response of the back-end detector when the inputs are in and out of phase (b) variable amplitude response.



(a) (b)

Figure 8: (a) Variation of the reference level against a ramp input (b) influence of the mirror factor (1~10) on detection window.

This would indicate the necessity of a suitable choice for the detection width with regard to maintaining symmetry. The next section would test the influence of the controlling parameters obtained from the expression of the decision threshold.

5.2.4. Mirror Factor. Using the control circuit implemented by T_8–T_{27}, the N_{mir} factor can be set from 1 to 5 if these devices have the same sizes as T_4 and T_5. Out of the parameters obtained from (17), N_{mir} exerts a greater influence in manipulating the detection window. By doubling the size of

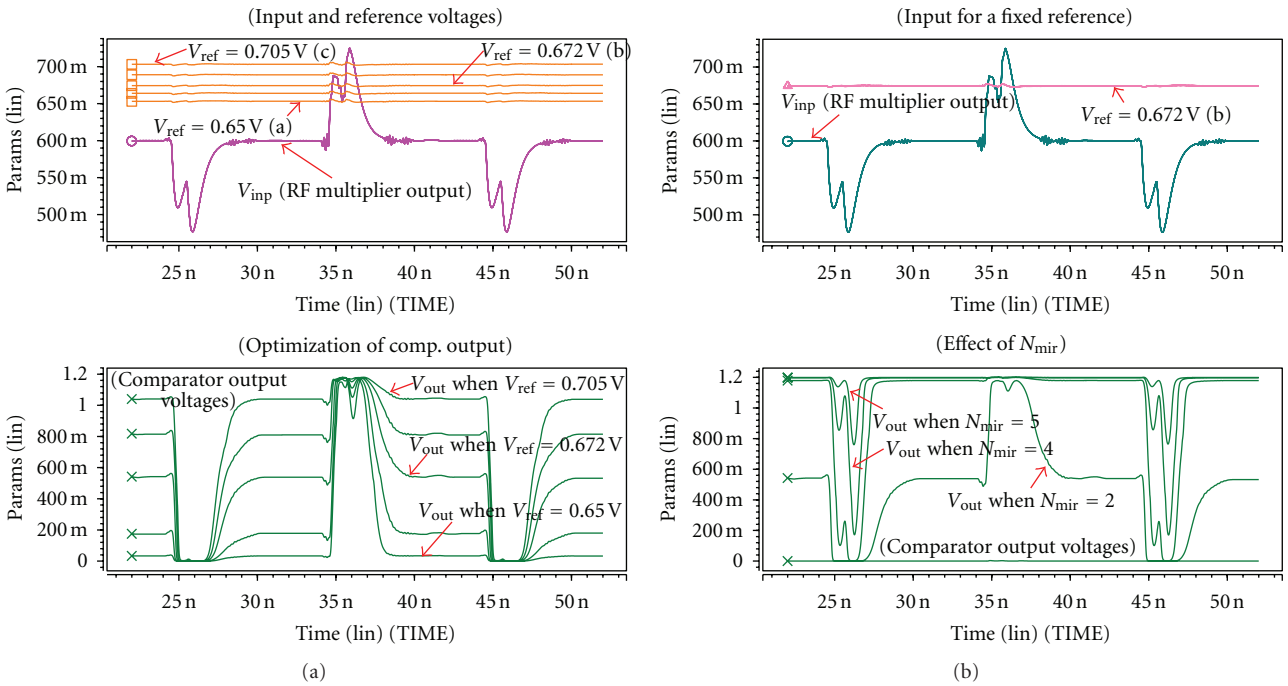


Figure 9: (a) Optimization of the reference level using the response from the decision circuit (b) effect of a variable mirror factor on the process of optimization.

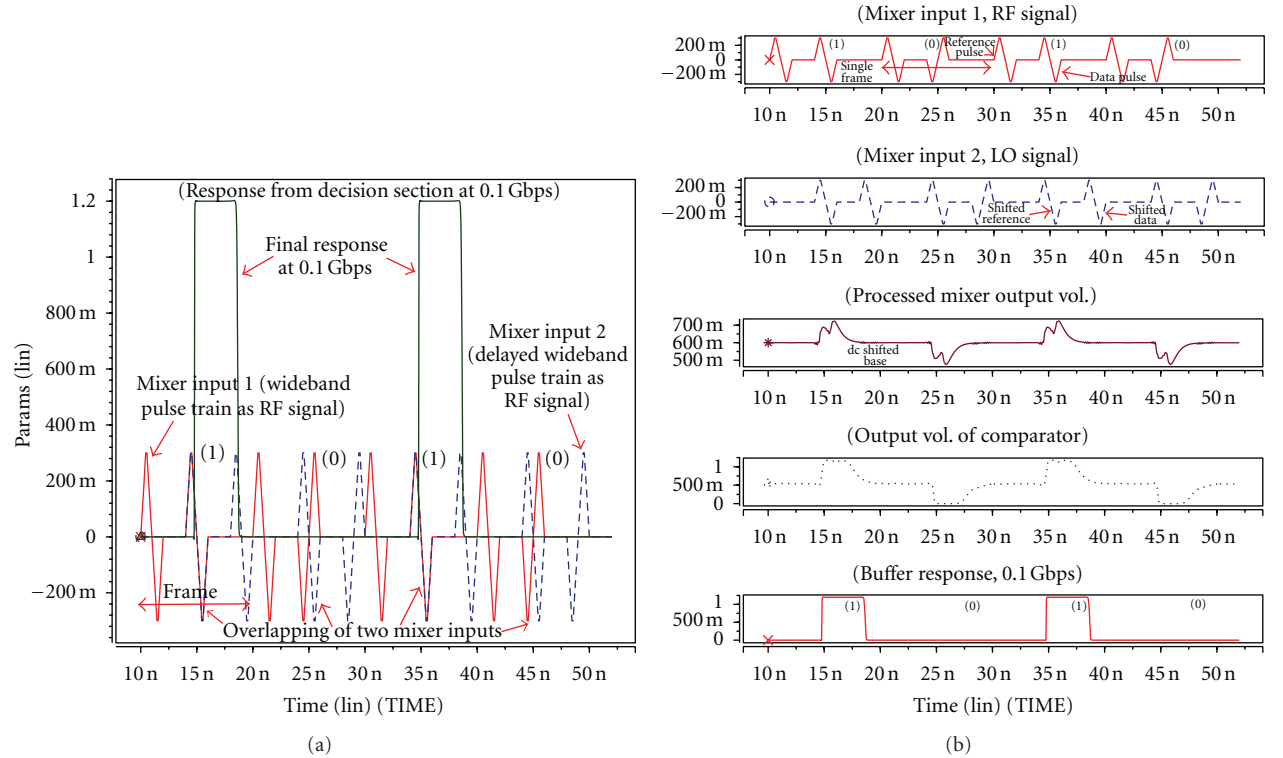


Figure 10: (a) RF and LO inputs and response for the decision block at 0.1 Gbps (b) corresponding signals at different stages in the proposed back-end of a TR-receiver.

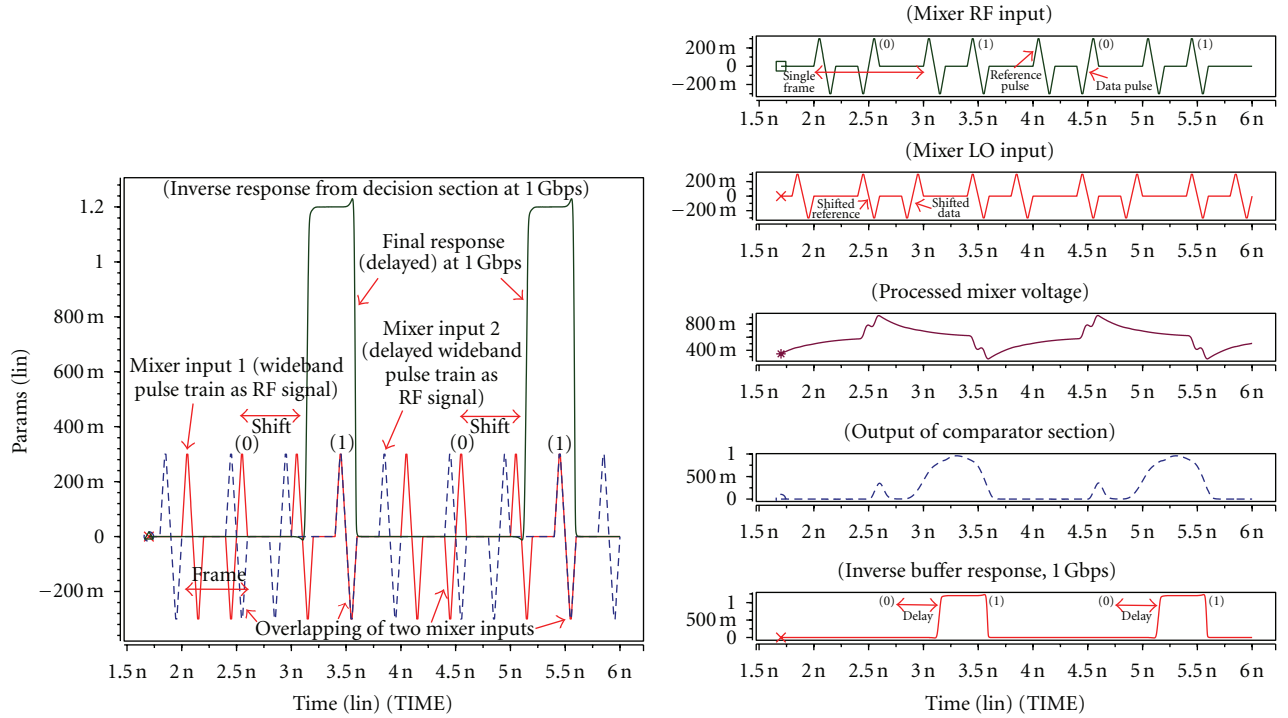


FIGURE 11: (a) Time-shifted inverse response at 1 Gbps (b) corresponding signals at different stages of the receiver.

T_8–T_{27} as compared to the dimensions of T_4 or T_5, N_{mir} can be extended to a value of 10. Within this coverage, the window width can be adjusted between ±80 to ±750 mV around the reference voltage, as shown in Figure 8(b). A high value of N_{mir} can lead to a very wide window, causing spurious detection in the receiver. So, a suitable value for the mirror factor is chosen as 2-3 to ensure a symmetric window. This can be achieved by tying two or three of the switching signals (Q_1–Q_5) in Figure 3(c) to the bias supply rail (V_{dd}).

5.2.5. Final Response from the Back-End. The back-end of a TR-receiver starts with an RF mixer (multiplier) which is followed by the threshold detection block (see Figure 1(b)). The RF mixer response, duely processed, is turned into a driving signal for the window detector. Rather than using separate integrator, sample-hold, and threshold detection blocks, we have proposed a buffered comparator core as the basis of the detector circuit. In the most simple form, each frame in a received UWB pulse train consists of a pair of pulses or a doublet. The first pulse in the frame is employed as a "synchronizing pulse" or "reference pulse" and it is followed by a "data pulse" modulated according to the message signal. We have seen in Figure 8(a) that the proposed decision circuit provides a quasi-symmetric detection window around a reference voltage of 0.58~0.78 V. Therefore, the mixer response is processed by a wideband amplifier and a shift in its dc base is introduced by a simple resistive adder. The shifted and modified RF mixer response is fed to the decision section as shown in Figure 9(a), and the reference level is carefully selected to vary between 0.65 to 0.705 V in minute steps of 0.01 V to optimize the reference signal. The corresponding response from the comparator becomes bipolar and quasi-symmetric with respect to its dc base when V_{ref} approaches 0.67 V. So the iteration of V_{ref} is repeated, this time in even smaller steps, and the final reference limit is set to the vicinity of 0.672 V. The N_{mir} factor is regulated in Figure 9(b) to assess the effect of a variable mirror factor after the reference signal is already optimized. The sharp degradation of the output signal suggests that the controlling parameters in (17) should be employed in a mutually exclusive fashion. And finally, a buffer gate should be placed at the output of the threshold detection circuit to recover a regular decoded data stream.

Figure 10(a) presents the response from a buffered window detector for an input bit rate of 0.1 Gbps. The two driving signals for the RF mixer (RF and LO excitations) are plotted in the same frame to visualize the overlapping of the two inputs at instances when the decision circuits produce a positive detection. The stream corresponds to an arbitrary four-bit sequence of 1 0 1 0, with the magnitude of the Gaussian pulses falling within the range of ±300 mV. The amount of delay between the two multiplier inputs is equal to the separation between the "reference pulse" and the "data pulse". The reference pulses of the second mixer input, after being delayed by a wideband element, become synchronized in time with the data pulses of the driving RF signal and there is no visible dispersion effect on the final responses. The signals at different stages of the proposed back-end for a TR-receiver are drawn separately in

Table 1: Relative merits of the 90 nm front-end amplifier.

References	Gain (S_{21}, dB)	Process (nm, CMOS)	Freq. (GHz)	Min. S_{11} (dB)	Min. S_{22} (dB)	Noise (NF, dB)	Supply (V)	IIP3 (dB_m)	Power (mW)	Core area (mm^2)	FOM_1
This work	20.5	90	22.7	−18	−24.8	3.5	1.2	−4	27.2	0.66	6.84
[20]	20	130	23.5	−12	−21.5	4.5	1.2	−5	24	0.36	5.59
[27]	23	180	16	−11	−18	6.5	1.5	—	28	1.32*	2.39
[28]	10	180	8	< −14	< −14	4.3	0.6	2	7	—	3.46
[29]	9.8	180	2.3	−20	−12	4	1.3	3	9	1.16	0.83
[30]	11	180	8.9	—	—	4.15	1	7	23.5	—	1.32
[31]	13	130	2.2	−28	—	4	1.3	7	2.62	0.58	3.64
[31]	15	130	2.2	−28	—	4.3	1.3	1	2.6	0.58	3.85
[32]	7	65	1	−17	—	2.6	1.2	1	14	0.009	0.31
[33]	17	180	1	−19	—	2.8	2.2	4	15.8	0.67	0.59
[34]	12	130	0.6	−12.5	−14	2.3	1.5	16	17.4	0.099	0.31
[35]	15	90	1.82	−20	—	3.85	1	14	4	0.294/	2.39
[36]	26	90	2	−23	−18	2.75	1	2	9	0.046	3.30
[37]	18	130	2	−23	—	3	1.2	−10	25	1.5*	0.72
[38]	12.5	65	1	−16	−23.5	2.3	1	−3	13.7	0.02	0.70
[38]	14.5	65	1	−12.5	−15.5	2.8	1	−5	7	0.03	1.15

/Including probe pads
*For entire front-end.

Table 2: Relative performance of the back-end decision circuit.

Reference	Technology (CMOS, nm)	Bias supply (V)	Power (mW)	Maximum speed/power (GHz/W)	Capacity/sampling freq.	Core area (mm^2)	FOM_2 (from (23))
This work	90	1.2	7.536	265.39	0.1∼2.0 Gbps	0.125	0.2212
[39]	130	1.8	180	8.9	1.6 GS/s	0.42	0.0049
[40]	65	1.2	110	9.1	1.0 GS/s	0.87	0.0076
[41]	65	1.2	60	16.7	1.0 GS/s	0.2	0.0139
[42]	65	1.0	40	55	2.2 GS/s	0.3	0.055
[43]	90	1.3	92	11.96	1.1 GS/s	0.37	0.0092
[44]	45	1.1	50	50	2.5 GS/s	1	0.0455
[45]	65	1.0	35	42.86	1.5 GS/s	0.5	0.0429
[46]	65	1.2	6.7	149.25	1.0 GS/s	0.11	0.1244
[47]	180	1.8	2.52	396.82	1.0 GS/s	—	0.2205
[48]	130	1.2	120	26.67	3.2 GS/s	0.18	0.0222
[49]	90	1.4	180	23.33	4.2 GS/s	0.66	0.0167

Figure 10(b), which include the input pulse streams (RF and LO) fed to a radio-frequency mixer, the base-shifted response from the mixer, the bipolar signal from the comparator (window detector), and the final response from an output buffer section. The buffer gate is implemented with a pair of cascaded inverters, producing a decoded stream from the response of the window comparator. The template data rate of the back-end circuits is tested up to 2 Gbps and at higher data rates (after 1 Gbps) the window detector performs with an inverse response, as shown in Figures 11(a) and 11(b). A certain amount of time-shift is also introduced by the logic gates existing in the design. The performance metrics of the TR front- and back-end components and their comparative standing with respect to published results are summarized in the next section.

6. Comparison of Performance

6.1. Front-End. Table 1 documents the performance of the proposed front-end double-stage 90 nm amplifier and compares it with simulated results from reported millimeter-wave front-end circuits [20, 27–38]. Simulated data have been collected from the references or concerned designs have been analyzed in the authors' environment to make a fair comparison. To evaluate designs built on different platforms, a composite figure-of-merit parameter (FOM_1) is defined with the following equation:

$$\mathrm{FOM}_1 = \frac{\text{Forward Gain(dB) Center Fr. (GHz)}}{\text{Power(mW)}\{\text{NF(dB)} - 1\}}. \quad (22)$$

As indicated by a high (FOM_1), the proposed design of the front-end delivers relatively high forward-gain, lower noise contribution, and a high peak gain frequency in the K-band, facilitating its interfacing with the following mixer in the TR-receiver.

6.2. Back-End. The performance of the buffered window comparator in the back-end is tabulated in Table 2, illustrating its relative merits with respect to data rate, power dissipation, speed/power ratio, and supply voltage. To quantify the relative simulated performance of the proposed decision block with respect to published detection circuits [39–49], a second figure-of-merit (FOM_2) is defined with

$$\mathrm{FOM}_2 = \frac{\mathrm{Max.\ Capacity}}{\mathrm{Power(mW)} \ * \ \mathrm{Bias\ Supply\,(V)}}. \tag{23}$$

The table shows the contrast in the figures-of-merit achieved by pipelined analog-to-digital converters and a window comparator. These findings verify the merits of the proposed TR-receiver back-end in terms of speed and power-efficiency.

7. Conclusions

The subject of this paper is the implementation of front- and back-end blocks for a transmit-reference (TR) receiver using noise and power efficient architectures. A 90-nm wideband amplifier is proposed for the front-end which achieves a forward gain 20.5 dB at the center-point with a 3.3 GHz bandwidth. The peak port matching parameters stand at −18 dB and −24.8 dB whereas the amplifier behaves linearly up to a power limit of $-4\,\mathrm{dB}_m$ at the driving port. To support the two-stage differential structure, the front-end consumes 27.2 mW while the noise performance (NF) approaches a minimum level of 3.5 dB near the center frequency (in K-band). The back-end of the TR-receiver is completed with a buffered detection circuit with a regulated decision window. Static and dynamic behavior for the detector block are tested with a variable transmit-reference pulse stream (0.1∼2 Gbps). For each unit of consumed power, the achieved speed of the window detector covers a range of 14 to 265.4 GHz. The proposed architectures fare better when compared with published designs of their counterparts and should help the on-chip realization of a TR-receiver.

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