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*Research Article*

# MOS Current Mode Logic with Capacitive Coupling

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A new MOS current mode logic (MCML) style exhibiting capacitive coupling to enhance the switching speed of the digital circuits is proposed. The mechanism of capacitive coupling and its effect on the delay are analytically modeled. SPICE simulations to validate the accuracy of the analytical model have been carried out with TSMC 0.18 $\mu$m CMOS technology parameters. Several logic gates such as five-stage ring oscillator, NAND, XOR2, XOR3, multiplexer, and demultiplexer based on the proposed logic style are implemented and their performance is compared with the conventional logic gates. It is found that the logic gates based on the proposed MCML style lower the delay by 23 percent. An asynchronous FIFO based on the proposed MCML style has also been implemented as an application.

## 1. Introduction

The rapid advances in the VLSI technology have led to the development of high-resolution mixed-signal applications. These applications demand high performance digital circuits to be integrated with analog circuitry on the same chip. MOS current mode logic (MCML) style has been widely used in digital circuits design for mixed-signal applications as they provide an analog friendly environment due to the low switching noise [1–4]. MCML circuits exhibit high switching speed, high noise immunity and better power efficiency at high operating frequencies along with a drawback of static power consumption [5–8].

In mixed-signal applications, the digital circuits are extensively used in the realization of digital signal processor functional units such as finite impulse response (FIR) filter and FFT module. The functional units are required to perform computations at high speed to efficiently use the bandwidth in communication systems which is also increasing. Therefore it is necessary to improve the speed of conventional MCML circuits. In this paper, a new MCML style with capacitive coupling that increases the switching speed of the circuits is proposed.

The paper first presents a brief introduction to conventional MCML style in Section 2. Thereafter, the architecture of the MCML style with capacitive coupling is proposed in Section 3. The mechanism of capacitive coupling is explained, and an expression for the delay is derived. The theoretical propositions are validated through SPICE simulations using TSMC 0.18 $\mu$m CMOS technology parameters in Section 4. The simulation results of several logic gates and an asynchronous FIFO are also presented in the same section. Finally, the conclusions are drawn in Section 5.

## 2. Conventional MCML Circuits

A conventional MCML circuit consists of three main components which includes a pull-down network (PDN), a constant current source, and a load circuit. The circuit of a conventional MCML inverter is shown in Figure 1. Its PDN consists of a source-coupled transistor pair MC2-MC3 with input A. The constant current source MC1 generates the bias current $I_{SS}$ while the load MC4 determines the output voltage swing [9]. The circuit works on the principle of current steering, where the bias current $I_{SS}$ is steered to one of the circuit branches depending on the input voltage. When the voltage at input A is high, the bias current $I_{SS}$ is steered to transistor MC2 and results in a low $V_{OL}$ ($V_{OL} = V_{DD} - V_P$) at the output node $Q$ and a high voltage ($V_{OH} = V_{DD}$) at the other node $\overline{Q}$ where $V_P$ is the voltage drop across the load [9]. Conversely, when the input $A$ is low, the bias current

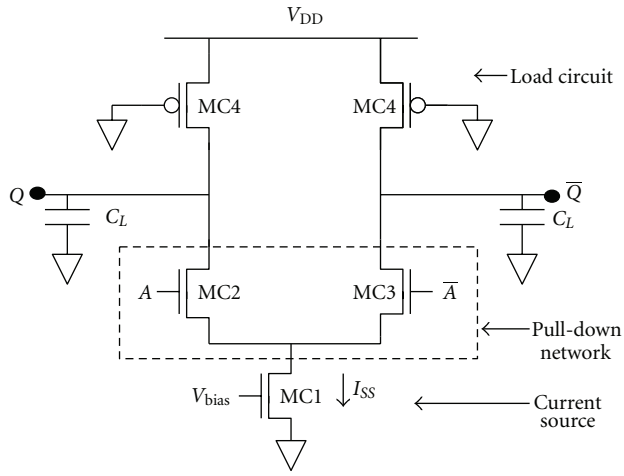


Figure 1: Conventional MCML inverter.

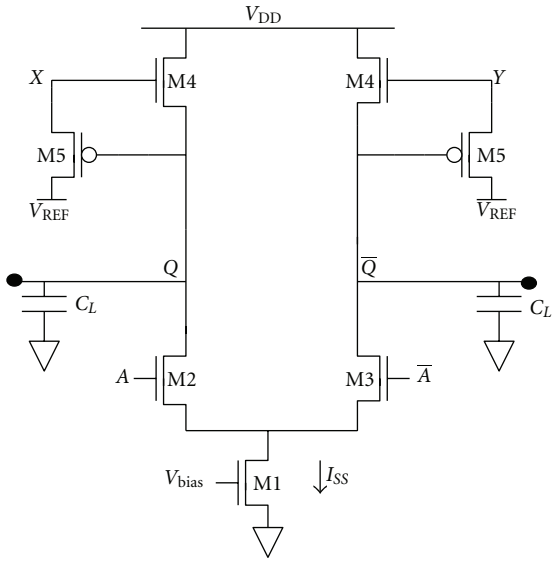


Figure 2: Proposed MCML inverter.

$I_{SS}$ is steered to MC3, and a high voltage is obtained at the node $Q$.

## 3. Proposed MCML Style

*3.1. Basic Architecture.* The basic architecture of the proposed MCML style includes a PDN, a constant current source, and a load that exhibits capacitive coupling to increase the switching speed of the circuits. An inverter based on the proposed logic style is shown in Figure 2. Its PDN consists of a source-coupled transistor pair M2-M3 to implement the logic function and a current source M1 to generate the bias current $I_{SS}$. The load includes one NMOS and one PMOS transistors M4-M5 as shown in Figure 2. The reference voltage $V_{REF}$ is chosen to be one threshold voltage above the supply voltage to allow the transistor M4 operation in linear region by making the potential at intermediate node

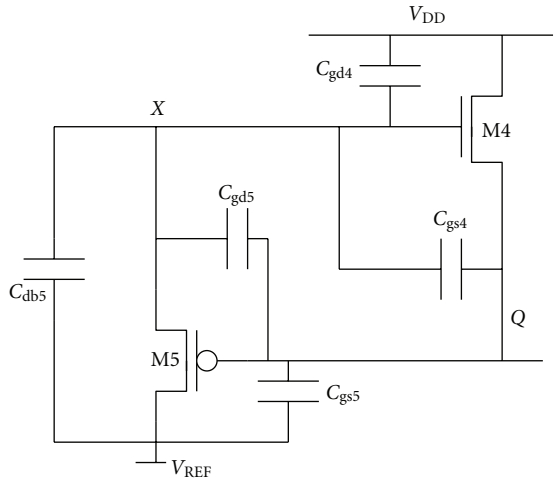


Figure 3: Parasitic capacitances of the transistors M4 and M5 in the load circuit.

$(X, Y)$ as $V_{REF}$. The circuit also works on the principle of current steering. The phenomenon of capacitive coupling in the proposed circuit is described in the following section.

*3.2. Capacitive Coupling.* In this section, the phenomenon of capacitive coupling in the proposed circuit is described, and an expression for the delay is derived. An expression for conventional MCML inverter delay, using the same method, is also given.

*3.2.1. Capacitive Coupling Analysis.* The phenomenon of capacitive coupling occurs in the load during the transition at output node voltage. This can be explained by considering the half circuit of the inverter (Figure 2) and identifying the capacitances at different nodes in the load (M4-M5). The capacitances are shown in Figure 3 where $C_{gdi}$, $C_{dbi}$ and $C_{gsi}$ represent the gate-drain capacitance, drain-bulk capacitance and gate-source capacitance of the $i$th transistor in the load. The capacitances $C_{gs4}$ and $C_{gd5}$ can be represented by the coupling capacitance between node $Q$ and the intermediate node $X$ as $C_C$ ($C_C = C_{gs4} + C_{gd5}$) whereas $C_{gd4}$ and $C_{db5}$ are the capacitance between node $X$ and ground as $C_X$($C_X = C_{gd4} + C_{db5}$). Initially, let the voltage at input A is assumed to be equal to high so that the voltage at Q is low ($V_Q = V_{OL}$). For a high-to-low transition at the input, the transistor M2 turns off and the voltage at $Q(V_Q)$ begins to rise from $V_{OL}$ to $V_{OH}$. This change in the output voltage gets coupled to node X through $C_C$.

Let $i_{C_C}$ and $i_{C_X}$ be the transient currents flowing through $C_C$ and $C_X$, respectively. By applying the KCL, the current equation at node X can be written as

$$i_{C_C} - i_{C_X} \approx 0, \tag{1}$$

where it is assumed that negligible current flows in transistor M5. Substituting the current values

$$C_X \frac{dV_X}{dt} \approx C_C \frac{d(V_Q - V_X)}{dt} \tag{2}$$

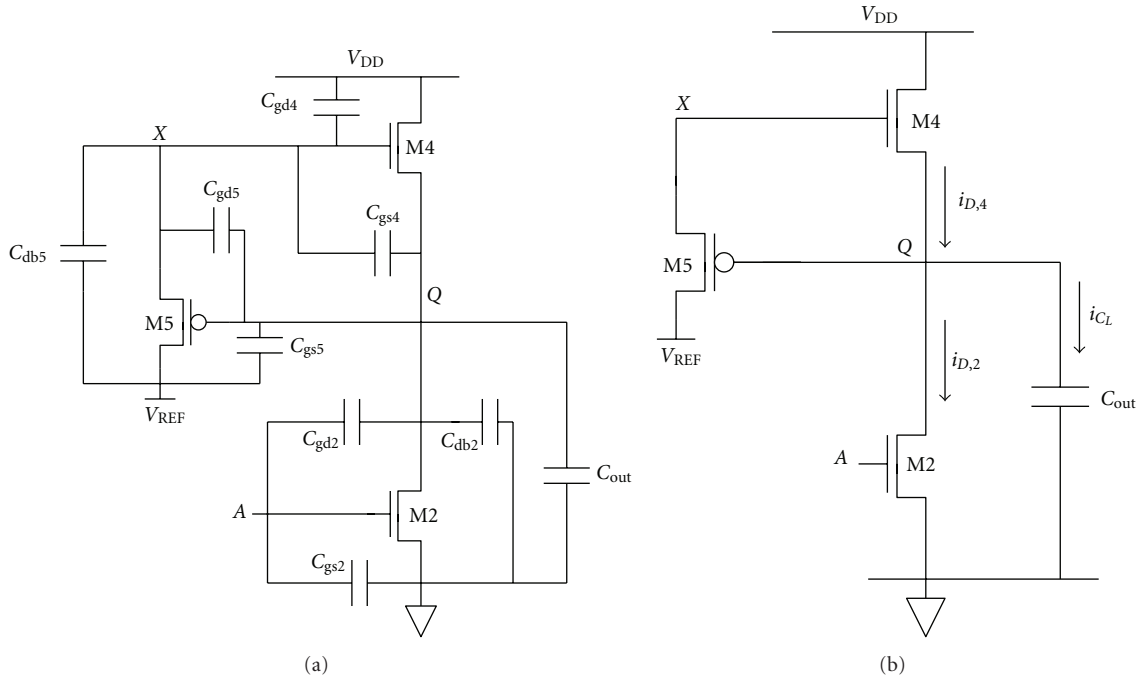


FIGURE 4: (a) Different capacitances in the half circuit of the proposed MCML inverter. (b) Half circuit of the proposed MCML inverter with load capacitance $C_L$.

which can be rearranged as

$$\frac{dV_X}{dt} = \frac{C_C}{C_C + C_X}\frac{dV_Q}{dt}. \tag{3}$$

It can be observe that an increase in the output voltage will result in an increase in the voltage of the node $X$. Multiplying (3) by dt and integrating both sides give

$$\int_{V_{REF}}^{V_X(t)} dV_X = \left(\frac{C_C}{C_C + C_X}\right)\int_0^t \frac{dV_Q}{dt}dt. \tag{4}$$

Completing the integral on the left side and rearranging it give

$$V_X(t) = V_{REF} + m\int_0^t \left(\frac{dV_Q}{dt}\right)dt, \tag{5}$$

$$= V_{REF} + m[V_Q(t) - V_Q(0)], \tag{6}$$

where $m = C_C/(C_C + C_X)$ represents the capacitance ratio and $V_{REF} = V_{DD} + V_T$. Further $V_X(t)$ may be expressed as

$$V_X(t) = \begin{cases} V_{DD} + V_T + m[V_Q(t) - V_{OL}] \\ \text{for } V_X(0) = V_{OL} \ldots \text{rising output} \\ V_{DD} + V_T - m\left[V_{OH} - V_Q(t)\right] \\ \text{for } V_X(0) = V_{OH} \ldots \text{falling output.} \end{cases} \tag{7}$$

*3.2.2. Delay.* The delay of the proposed MCML inverter can be modeled by solving the state equation of the output node in the time domain [10]. The half circuit of the proposed MCML inverter with the parasitic capacitances of the transistors is shown in Figure 4(a), where $C_{out}$ represents the output that includes the interconnect capacitance and the input capacitance of the subsequent stage, respectively. The total capacitance at the output node $C_L$ is shown in Figure 4(b) which may be computed as

$$C_L = C_{gd2} + C_{db2} + C_{gs5} + C_{gd5} + C_{gs4} + C_{out}. \tag{8}$$

The current through capacitor $C_L$ may be written as

$$C_L\frac{dV_Q}{dt} = i_{C_L} = i_{D,4} - i_{D,2}. \tag{9}$$

When the input switches from high to low, the current through transistor M2 becomes zero such that $C_L$ begins to charge through the load transistor M4. Thus, (9) reduces to

$$C_L\frac{dV_Q}{dt} = i_{D,4}. \tag{10}$$

The rising output voltage initiates the process of capacitive coupling in the load circuit. It is clear from (7) that the gate potential of M4 remains greater than or equal to $V_{REF}$ during the charging process, hence M4 operates in linear region throughout the switching process. Therefore, the delay $t_{PLH}$ may be calculated by solving (10) as

$$t_{PLH} = \int_{t_0}^{t_1} dt = C_L\int_{V_{OL}}^{V_{50\%}} \left(\frac{1}{i_{D,4}}\right)dV_Q. \tag{11}$$

Substituting $i_{D,4}$ in (11) results in

$$t_{\mathrm{PLH}} = \frac{2\,C_L}{k_{n,4}} \int_{\mathrm{V_{OL}}}^{\mathrm{V_{50\%}}} \left( \frac{1}{\left[2(\mathrm{V_X} - \mathrm{V_Q} - \mathrm{V_T})(\mathrm{V_{DD}} - \mathrm{V_Q}) - (\mathrm{V_{DD}} - \mathrm{V_Q})^2\right]} \right) \mathrm{dV_Q}, \tag{12}$$

where $k_{n,4}$ is the transconductance parameter of transistor M4

$$t_{\mathrm{PLH}} = \frac{2C_L}{k_{n,4}} \int_{V_{\mathrm{OL}}}^{V_{50\%}} \left( \frac{1}{(V_{\mathrm{DD}} - V_Q)\left[V_{\mathrm{DD}} + (2\,m - 1)V_Q - 2\,mV_{\mathrm{OL}}\right]} \right) dV_Q. \tag{13}$$

Evaluating the integral yields

$$t_{\mathrm{PLH}} = \frac{C_L}{k_{n,4}} \frac{1}{m(V_{\mathrm{DD}} - V_{\mathrm{OL}})} \times \ln \frac{V_{\mathrm{DD}} - V_Q}{V_{\mathrm{DD}} + (2\,m - 1)V_Q - 2\,mV_{\mathrm{OL}}} \Bigg|_{V_{\mathrm{OL}}}^{V_{50\%}}. \tag{14}$$

Equation (14) evaluates to

$$t_{\mathrm{PLH}} = \frac{C_L}{k_{n,4}} \frac{1}{m(V_{\mathrm{DD}} - V_{\mathrm{OL}})} \times \ln \frac{V_{\mathrm{DD}} + 2\,m(V_{50\%} - V_{\mathrm{OL}}) - V_{50\%}}{V_{\mathrm{DD}} - V_{50\%}}. \tag{15}$$

Similar analysis for a conventional MCML inverter (Figure 1) gives the delay as

$$t_{\mathrm{PLH}} = \frac{C_L}{k_{p,4}} \frac{1}{\left(V_{\mathrm{DD}} + V_{T,p}\right)} \left[ \ln \frac{V_{\mathrm{DD}} + 2V_{T,p} + V_{50\%}}{V_{\mathrm{DD}} - V_{50\%}} - \ln \frac{V_{\mathrm{DD}} + 2V_{T,p} + V_{\mathrm{OL}}}{V_{\mathrm{DD}} - V_{\mathrm{OL}}} \right], \tag{16}$$

where $k_{p,4}$, and $V_{T,p}$ are the transconductance and the threshold voltage of PMOS transistor MC4, respectively.

## 4. Simulation Results

This section first demonstrates the phenomenon of capacitive coupling in the proposed MCML inverter (Figure 2) to verify the theoretical propositions presented in Section 3. Thereafter, the performance of the proposed MCML logic style is compared with the conventional MCML logic style by simulating different logic gates. Lastly, the simulation results for an asynchronous FIFO based on the proposed style are presented. All the simulations are performed by using TSMC 0.18 $\mu$m CMOS technology parameters with $V_T = 0.5\ V$ and a supply voltage of 1.8 V. The bias current of all the circuits is taken as 100 $\mu$A uniformly.

*4.1. Proposed MCML Inverter.* The proposed MCML inverter (Figure 2) with $m = 0.6$ and $V_{\mathrm{OL}} = 1.4\,\mathrm{V}$ is designed and simulated to demonstrate the phenomenon of capacitive coupling. The aspect ratios of the transistors calculated are $(\mathrm{W/L})_{\mathrm{M1}} = 0.81/0.18$, $(\mathrm{W/L})_{\mathrm{M2,M3}} = 26.8/0.18$, $(\mathrm{W/L})_{\mathrm{M4}} = 0.68/0.18$, $(\mathrm{W/L})_{\mathrm{M5}} = 0.54/1.35$. The waveforms at the input, $X$, and output nodes are shown in Figure 5. It can be observed that the rising output voltage increases the voltage of node X which confirms the relation between voltages at node $Q$ and $X$ (3). Also, it can be observed that during a low-to-high transition at the output, for an output voltage $V_Q = 1.8\,\mathrm{V}$ the potential at node $X$ raises $V_X = 2.54$ V and is in accordance with (7) in Section 3.

The delay of the proposed MCML inverter expressed by (15) is validated for different values of m ranging from 0.1 to 1. The error in the predicted and the simulated delay is plotted for different values of m in Figure 6 and is always is less than 12%. Thus, the simulation results are in close agreement with the theoretical values.

*4.2. Performance Comparison.* Several logic gates such as inverter, five-stage ring oscillator (RO5), NAND, XOR2, XOR3, multiplexer, and demultiplexer based on the proposed MCML style and conventional MCML style are implemented for the purpose of comparison. The aspect ratios of the transistors in the PDN of the two styles are taken to be same. It may be noted that since all the circuits are implemented with the same supply voltage and bias current, therefore they will consume the same static power which is computed as the product of the supply voltage and bias current [4]. The delay of the gates based on both the logic styles is listed in Table 1. It can be observed that an improvement varying from 16% to 23% can be obtained in delay by using the proposed MCML logic style.

Table 1: Delay comparison of logic gates.

| Logic gate | Delay of conventional MCML-based circuit (ps) | Delay of proposed MCML-based circuit (ps) | Percentage reduction |
|---|---|---|---|
| Inverter ($C_L$ = 50 fF) | 209 | 165 | 21% |
| Inverter ($C_L$ = 100 fF) | 419 | 340 | 18% |
| Inverter ($C_L$ = 250 fF) | 985 | 827 | 16% |
| Ring Oscillator (RO5) | 290 | 250 | 14% |
| NAND | 1795 | 1503 | 16% |
| XOR2 | 1950 | 1506 | 22% |
| XOR3 | 2153 | 1800 | 16% |
| 2 : 1 Multiplexer | 1955 | 1511 | 23% |
| 1 : 2 Demultiplexer | 1988 | 1600 | 19.5% |

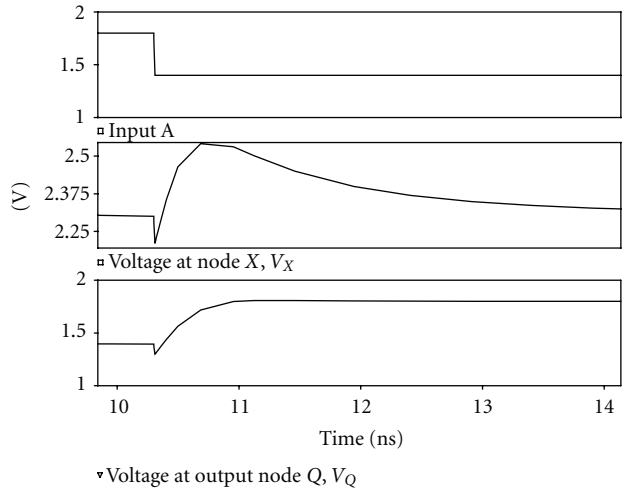


Figure 5: Voltages at different nodes of the proposed MCML inverter.

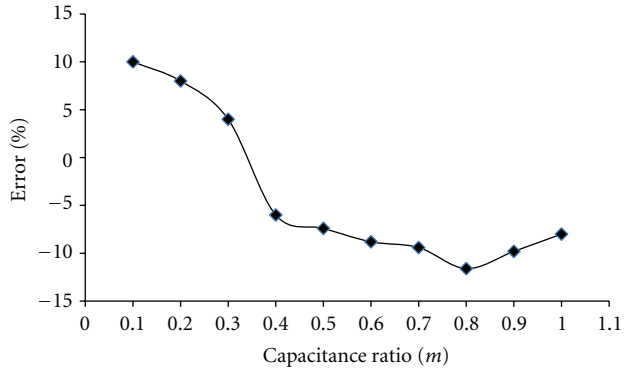


Figure 6: Error in the predicted and the simulated delay for the proposed MCML inverter with respect to $m$.

*4.3. Application Example.* An asynchronous FIFO is implemented as an application of the proposed MCML logic style. An asynchronous FIFO connects the sender and the receiver through a data bus consisting of separate request and acknowledge signals, and data signals [11–13]. The block diagram of a 4 stage FIFO is shown in Figure 7. It comprises of four stages wherein each stage consists of a functional unit and a control unit. The functional unit has a combinational stage for computing the result of each stage and a matched delay element inserted in the request line. The control unit employs a double-edge triggered flip-flop (DETFF) and a C element to control the communication between the successive stages. The signals shown as Req(in) and Ack(out) communicate the data, Data(in) between sender and the first stage. At the receiver side, the signals Req(out) and Ack(in) are used to synchronize the output data, Data(out) with the receiver and the last stage. Initially, the input data, Data(in) is loaded in the first stage of the FIFO and the Req(in) is asserted to low to start the data transfer. This results in a transition at the output of a C-element such that the data is stored in the DETFF of the first stage. At the same time an acknowledge signal Ack(out) is given to the sender. The stored data then flows through the different stages in the FIFO. Then, a request signal Req(out) is generated by the last stage to the receiver to enable the receiver to accept the data. This is followed by an acknowledge signal, Ack(in) from the destination to the last stage.

The circuits of the control unit elements based on the proposed logic style are shown in Figure 8. The waveforms obtained through the simulation of a four-stage asynchronous FIFO are shown below in Figure 9. The first three waveforms correspond to the input data Data(in), request signal (Req_in), and acknowledge signal (Ack_out) at the sender section. The last three graphs are the acknowledge signal Ack(in), data Data(out) and request signal Req(out). It can be found that the asynchronous FIFO based on the proposed logic style outputs the sampled data correctly.

## 5. Conclusion

In this paper, a new MCML style with capacitive coupling to increase the speed of the digital circuits is proposed. The phenomenon of capacitive coupling occurs in the load of the proposed style. The coupling phenomenon has been explained and analyzed. An expression for the delay has also been derived and validated through SPICE simulations using TSMC 0.18 $\mu$m CMOS technology parameters. Several logic gates based on the proposed logic style are implemented and their performance is compared with the conventional logic

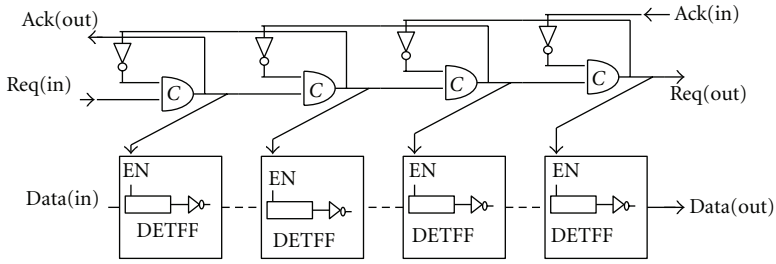


Figure 7: Block diagram of 4-stage asynchronous FIFO.

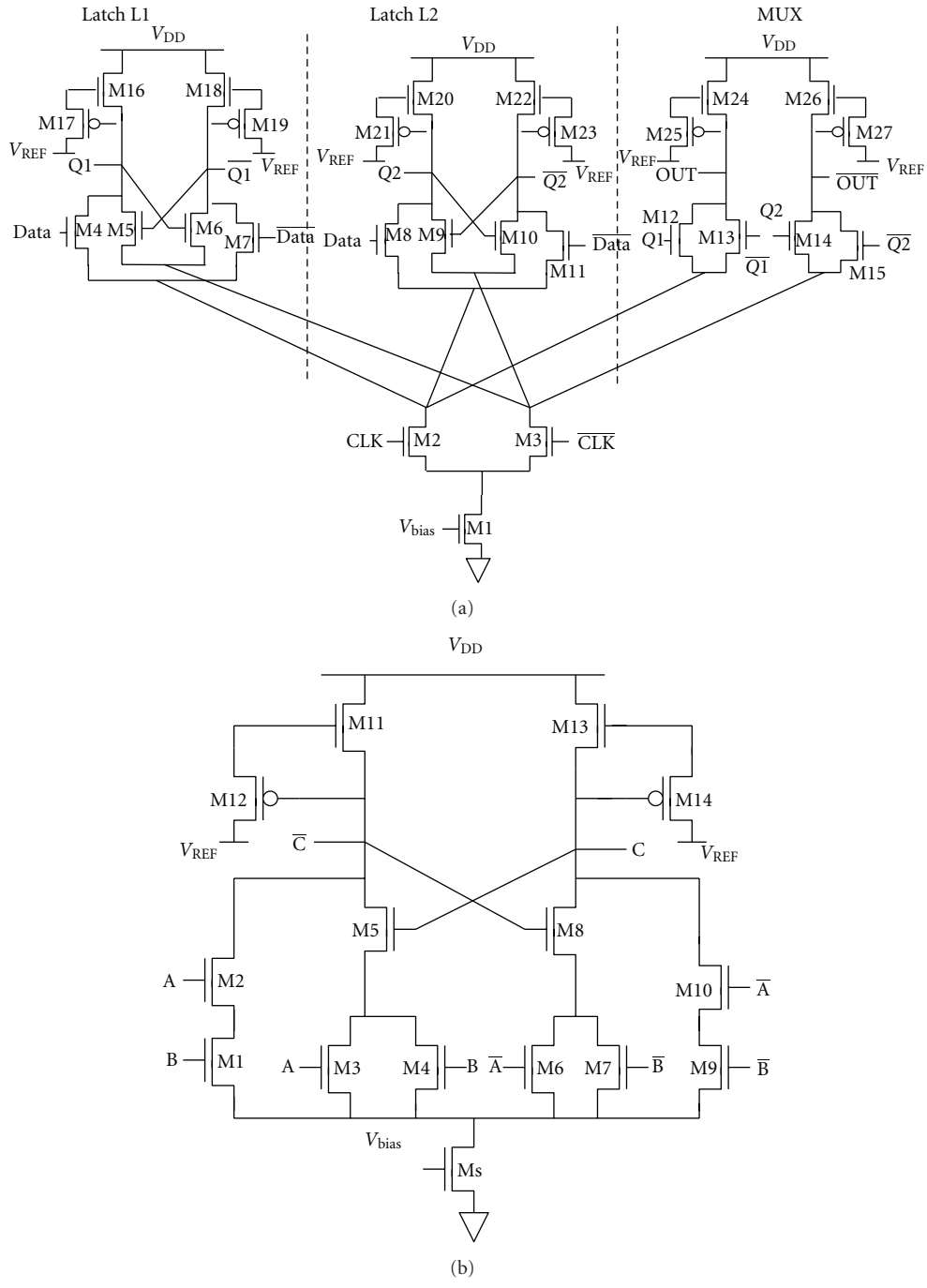


Figure 8: Control unit elements based on the proposed MCML style (a) DETFF (b) C-element.

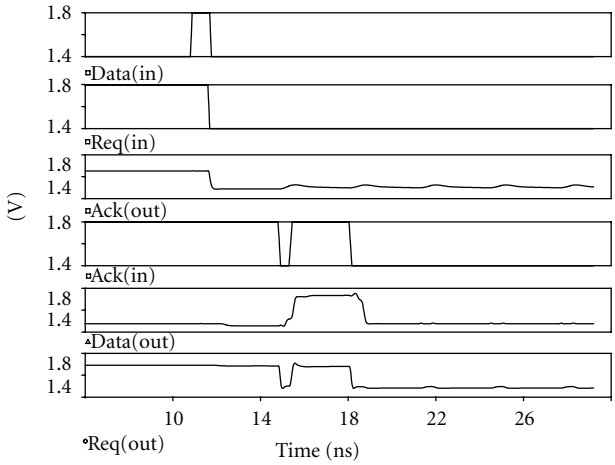


Figure 9: Transient response of the 4-stage asynchronous FIFO based on the proposed MCML style.

gates. It is found that a delay reduction of up to 23 percent delay reduction can be achieved by employing the proposed MCML style in the design of logic circuits.

## References

[1] J. M. Musicer and J. Rabaey, "MOS Current Mode Logic for low power, low noise CORDIC computation in mixed-signal environments," in *Proceedings of the Symposium on Low Power Electronics and Design (ISLPED '00)*, pp. 102–107, July 2000.

[2] S. Bruma, "Impact of on-chip process variations on MCML performance," in *Proceedings of the IEEE Conference on Systems-on-Chip*, pp. 135–140, September 2003.

[3] M. Anis, M. Allam, and M. Elmasry, "Impact of technology scaling on CMOS logic styles," *IEEE Transactions on Circuits and Systems II*, vol. 49, no. 8, pp. 577–588, 2002.

[4] M. Alioto and G. Palumbo, *Model and Design of Bipolar and MOS Current-Mode logic (CML, ECL and SCL Digital Circuits)*, Springer, New York, NY, USA, 2005.

[5] O. Musa and M. Shams, "An efficient delay model for MOS current-mode logic automated design and optimization," *IEEE Transactions on Circuits and Systems I*, vol. 57, no. 8, pp. 2041–2052, 2010.

[6] H. Hassan, M. Anis, and M. Elmasry, "MOS current mode circuits: analysis, design, and variability," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 13, no. 8, pp. 885–898, 2005.

[7] J. B. Kim, "Low-power MCML circuit with sleep-transistor," in *Proceedings of the 8th IEEE International Conference on ASIC (ASICON '09)*, pp. 25–28, October 2009.

[8] T. K. Agarwal, A. Sawhney, A. K. Kureshi, and M. Hasan, "Performance comparison of static CMOS and MCML gates in sub-threshold region of operation for 32 nm CMOS technology," in *Proceedings of the International Conference on Computer and Communication Engineering*, pp. 284–287, May 2008.

[9] M. Alioto and G. Palumbo, "Power-delay optimization of D-latch/MUX source coupled logic gates," *International Journal of Circuit Theory and Applications*, vol. 33, no. 1, pp. 65–86, 2005.

[10] S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, Tata Mcgraw Hills, 3rd edition, 2006.

[11] M. Shams, J. C. Ebergen, and M. I. Elmasry, *Asynchronous Circuits*, John Wiley's Encyclopedia of Electrical Engineering, 1999.

[12] I. E. Sutherland, "Micropipelines," *Communications of the ACM*, vol. 32, no. 6, pp. 720–738, 1989.

[13] T. W. Kwan and M. Shams, "Design of multi-ghz asynchronous pipelined circuits in MOS current-mode logic," in *Proceedings of the 18th International Conference on VLSI Design: Power Aware Design of VLSI Systems*, pp. 301–306, January 2005.