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Research Article

Numerical Simulation on Electrical-Thermal Properties of Gallium-Nitride-Based Light-Emitting Diodes Embedded in Board

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The electrical-thermal characteristics of gallium-nitride- (GaN-) based light-emitting diodes (LED), packaged by chips embedded in board (EIB) technology, were investigated using a multiphysics and multiscale finite element code, COMSOL. Three-dimensional (3D) finite element model for packaging structure has been developed and optimized with forward-voltage-based junction temperatures of a 9-chip EIB sample. The sensitivity analysis of the simulation model has been conducted to estimate the current and temperature distribution changes in EIB LED as the blue LED chip (substrate, indium tin oxide (ITO)), packaging structure (bonding wire and chip numbers), and system condition (injection current) changed. This method proved the reliability of simulated results in advance and useful material parameters. Furthermore, the method suggests that the parameter match on Shockley's equation parameters, R_s, n_{ideal}, and I_s, is a potential method to reduce the current crowding effect for the EIB LED. Junction temperature decreases by approximately 3 K to 10 K can be achieved by substrate thinning, ITO, and wire bonding. The nonlinear-decreasing characteristics of total thermal resistance that decrease with an increase in chip numbers are likely to improve the thermal performance of EIB LED modules.

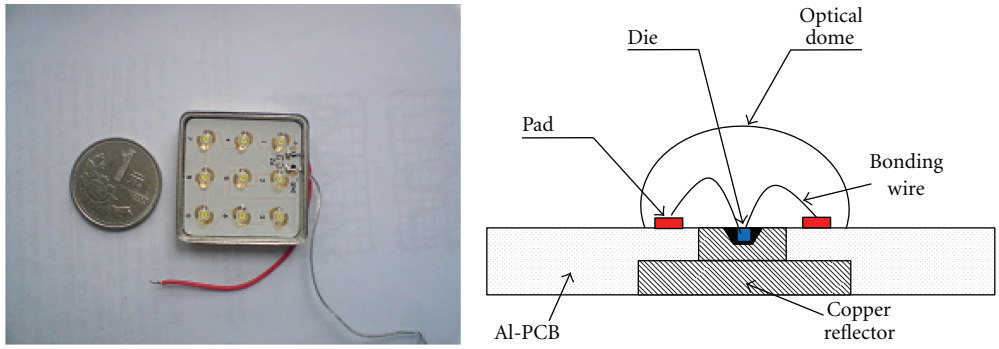
1. Introduction

Numerous simulation studies of gallium-nitride- (GaN-) based light-emitting diodes (LED) have been proposed to overcome the technical challenges in high power LED lighting [1–4]. These include thermal management, electric drive, and light extraction as well as insights into microscopic carrier transfer mechanisms [5], such as efficiency droop [6]. However, most of these studies focused on the electric, optical, or thermal problems of a single LED using a single physical field code, for instance, ANSYS [7], or general-purpose semiconductor optoelectronic simulator, such as SYNOPSYS [8]. These methods bring high-power lighting application inconvenience for simulating multichips packaged LED arrays with multiphysical field and multiscale properties [9].

Based on the proposed chips in board packaging method, where the aluminum- (Al-) core printed circuit boards (Al-PCB) with 9 round holes are embedded with copper reflectors for integrating chips [10] (see Figure 1), the finite element simulation code COMSOL [11] is adopted to address this demand. The multiphysical field and multiscale COMSOL model for the packaging structure has been proposed. The sensitivity analysis of the current crowding, the temperature distribution, and the thermal resistance to parameters of the blue chip, packaging structure, and system condition are also discussed.

2. Simulation Model

Heat generation and transfer of Joule heating in GaN-based LEDs with mass density ρ, specific heat c, and thermal



(a) Photo of the 9-chip sample

(b) A chip packaging structure.

Figure 1: Proposed chips in board packaging method.

conductivity k_T are given in [12]. The coupled thermal and electrical behavior can be modeled as follows. The Joule heating Q of a current density J with an electrical field E is

$$Q = J \cdot E, \tag{1}$$

where E the gradient of electric potential φ, $E = -\nabla\varphi$, ∇ is the gradient operator, determined by an external current density J_{ex} and electrical conductivity σ under static conditions

$$\nabla(\sigma \cdot \nabla\varphi - J_{ex}) = 0. \tag{2}$$

The distribution of temperature field T at time t is

$$\rho c \frac{\partial T}{\partial t} = \nabla \cdot k_T \nabla(T) + Q. \tag{3}$$

The temperature T at next time determines new temperature-dependent material parameters, such as heat coefficient k_T. Finally, the potential φ, temperature T, current density $J = (\sigma \cdot \nabla\varphi)$, and so on can be solved based on (1), (2), and (3), combined with temperature-dependent models of material parameters and boundary conditions.

Using the COMSOL Draw model, the 3D finite element geometry of the proposed packaging structure was created (Figure 2). The geometry model (Figure 2(a)) contained both components of centimeter-scale 9-chip LED array (Figure 2(b)): heat sink, bonding wires and reflectors, and chip properties of micron-scale structures (Figure 2(c)). The chip properties of micron-scale structures include negative/positive electrodes (n/p-Pad), GaN current spreading layers (n/p-GaN), and multiple-quantum well (MQW).

The electrical and thermal physical domains were added to the 3D multiscale geometry model by subdomain/boundary settings in COMSOL. Equations (2) and (3) were specified by heat conduction module and AC/DC module, respectively. Furthermore, (3) and the material parameters listed in Table 1 including the thickness h, k_T, and σ or sheet resistance R_{sh} $(= 1/\sigma \cdot h)$ were suggested in modeling the electricthermal physical process. Thus, the 3D COMSOL multiphysical field (electricthermal) and multiscale simulation models for the chips in board packaging method have been developed. Finally, after mesh generation and a Newton-Raphson-based solution, the parameters φ, T, and J are determined. The electrical-thermal characteristics of LEDs can also be gained from COMSOL-generated postprocessing functions.

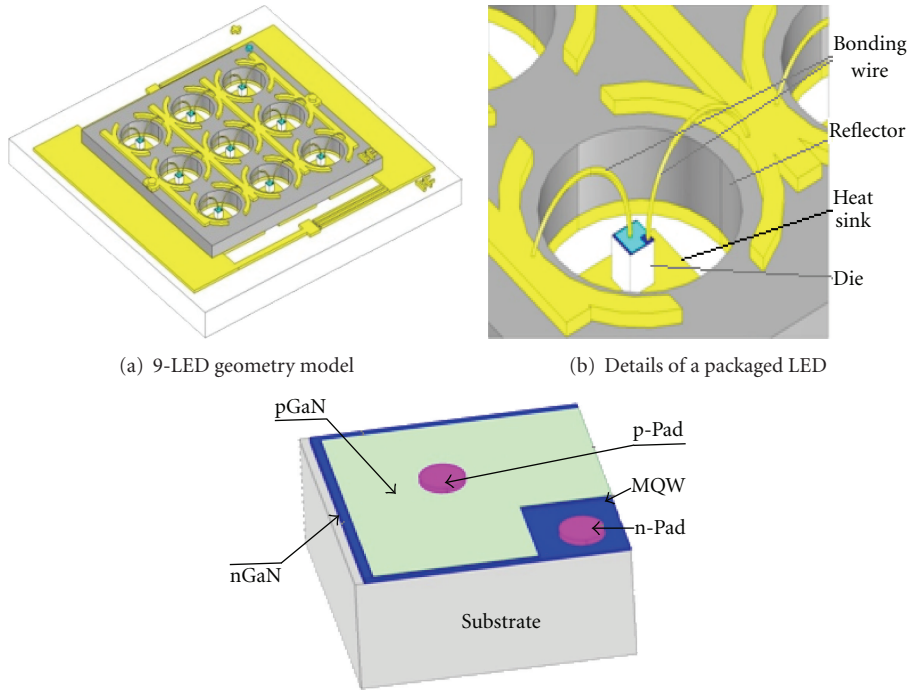
Table 1: Properties of the blue chip.

Materials	Parameter		
	h (μm)	k_T (W/m·K)	σ (S/m)
p/n-Pad	0.2	385	10^{15}
pGaN	0.1	$160 \times (T/300)^{-0.6}$	35
MQW	0.01	$177 \times (T/300)^{-0.8}$	10^3
nGaN	3.5	$160 \times (T/300)^{-0.6}$	10^4
substrate	200	$38 \times (T/300)^{-1.5}$	10^{-7}

Under constant electrical power per chips with 20 mA injection current, the lowest temperature of Al-PCB was at 300 K, which was also the default value of the samples. The model was simulated by using a computer with Core i7-2600/DDR3 8 GB. The electrical- thermal simulation results of the model are demonstrated in Figure 3. The temperature distribution in chips presented an uneven temperature profile and the maximum temperature (314.7 K) occurred at the region of p-pad electrodes (Figure 3(b)), which have been validated with experimental results [8].

3. Results and Discussion

Based on the calibrated temperature coefficient −1.82 mV/K, a multimeter RIGOL DM3052 recorded the forward voltage of the LED which had operated for 10 minutes after the 20 mA current was injected. Thus, the p-n junction temperatures of the 9-chip sample were deduced [10] and listed in Table 2. However, some differences in the p-n junction temperatures of the simulation results and the forward-voltage-based experimental results were observed. To reduce error and bias on the maximum temperature (approximately 3 K), the intermittent thermal layer is introduced into the simulation model. The simulation results based on the optimized model are shown in Table 2 (optimized results column). A decrease in temperature was observed. However, the uneven temperature distribution has not been simulated.

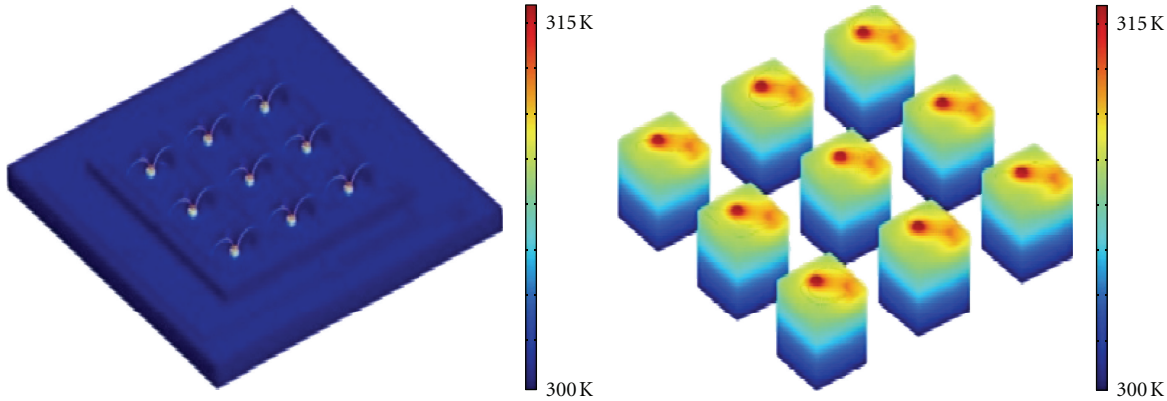


(a) 9-LED geometry model

(b) Details of a packaged LED

(c) Details of a blue chip

Figure 2: 3D COMSOL structures of the chips in board.



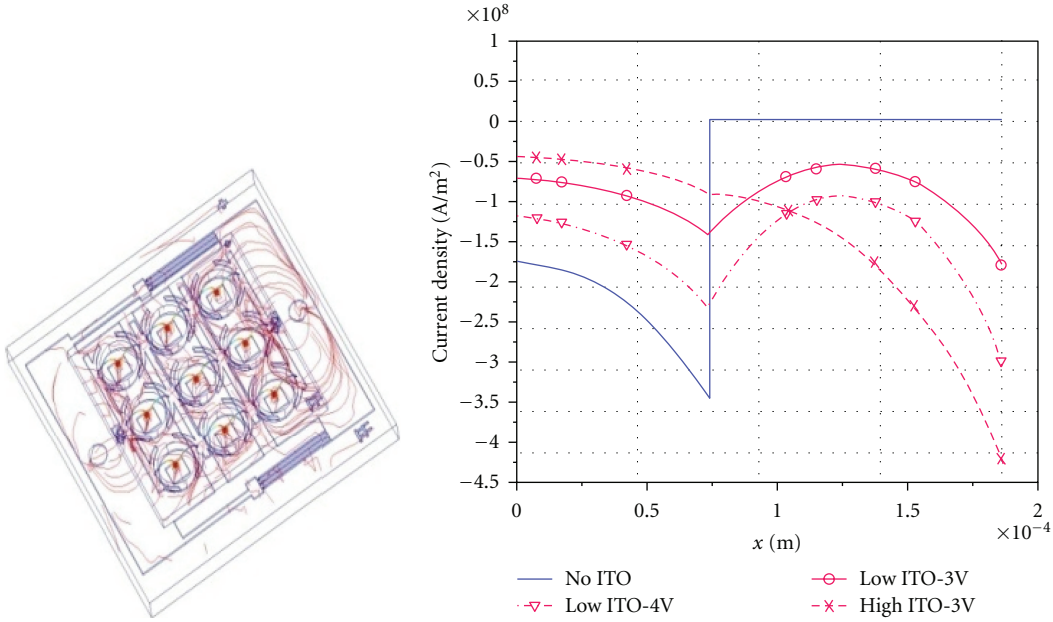
(a) Whole structure

(b) Highlighted blue chips

Figure 3: 3D electricthermal simulations.

Based on the optimized simulation model, the current crowding effect or current density distribution (red stream line) of the proposed LED array has been investigated (Figure 4(a)). We analyzed the sensitivities of the proposed model on the injection current or forward bias voltage in addition to the parameters of indium tin oxide (ITO) targeted from In_2O_3: SnO_2 in a 90/10 wt.% with different deposition conditions, such as R_{sh}, is 188 Ω/°C and 1100 Ω/°C, with annealing temperatures of 375 K and 475 K [13], denoted as "Low ITO" and "High ITO," respectively (Figure 4(b)).

The simulation results revealed several findings. First, the uneven current distribution occurred at the MQW region. The higher the forward-voltage across the LED (e.g., "Low ITO-3V" via "Low ITO-4V"), the more uneven the current density distribution becomes. The result concurred with the local high temperature and uneven light output observed in experiments. Second, the high current density occurred at the p-pad region, due to the low-doping and high-resistance properties of p-GaN material. Third, ITO can improve the uniform of current distribution in MQW, and its performance depends on the electrical conductivity of the ITO. The current distribution becomes more uniform and the current spreading along the x-axis in Figure 2(c) across the p-electrode is fit to have a Gaussian distribution with increasing electrical conductivity of



(a) Current density distribution

(b) Current density distribution in MQW

Figure 4: Current crowding simulations.

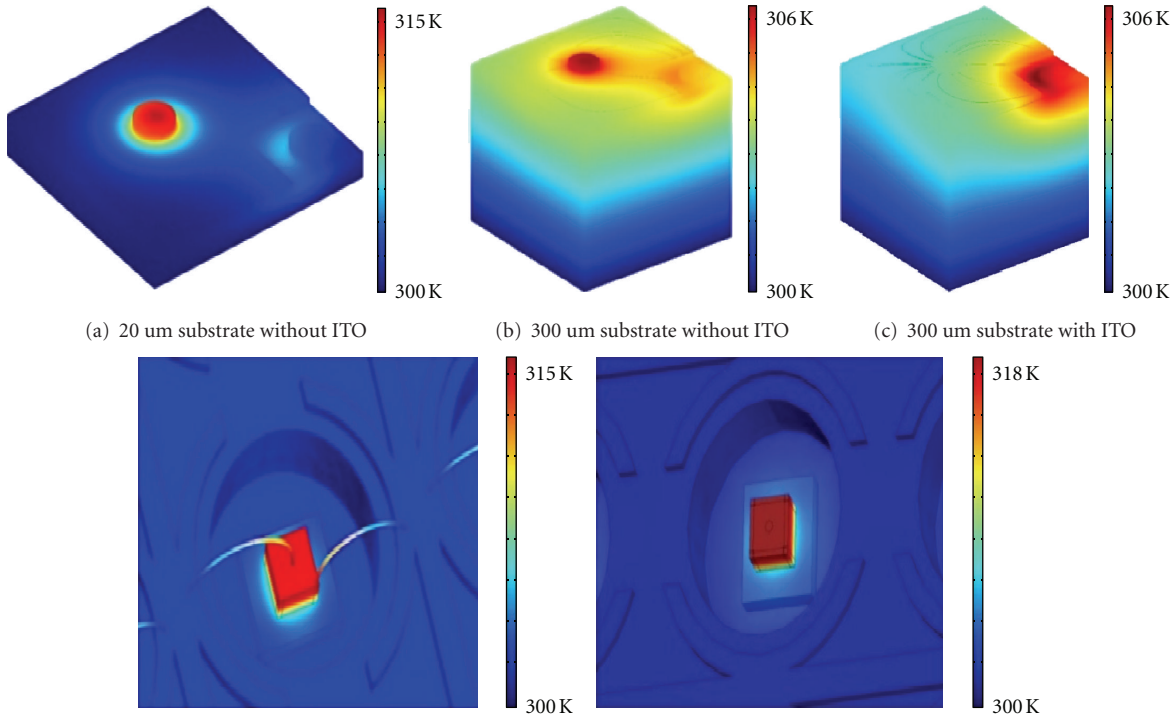
Table 2: 9-LED array junction temperatures by numerical simulation and experiment method (units: K).

Chip	Method		
	Simulated results	Experimental results	Optimized results
1	314.7	317.3	317.2
2	314.7	316.8	317.2
3	314.7	316.5	317.2
4	314.7	316.1	317.2
5	314.7	318.9	317.2
6	314.7	318.1	317.2
7	314.7	317.6	317.2
8	314.7	318.5	317.2
9	314.7	318.4	317.2

the ITO ("HighITO-3V" via "LowITO-3V" or "No_ITO"). This distribution contrasted with the exponential decay using Guo and Kirchhoff's current law [14] because the contacts have unequal potential in the 3D simulation. Lastly, the difference between maximum and minimum for the array current ΔI_f is a main reason for the current-crowding effect, and parameters (series resistance R_s ideal factor n_{ideal} and saturation current I_s) match process of the Shockley equation is of great importance. The sensitivity of ΔI_f to parallel resistance R_p has minor effects because of $|\partial(\Delta I_f)/\partial(R_p)| \approx (V_f - I_f R_s)/(R_p)^2 \to 0$. R_p is about 1000 Ω and the forward voltage is approximately 3 V in practical application. On the other hand, the sensitivities of ΔI_f to R_s, n_{ideal}, and I_s produced the same effect, for instance, the sensitivity ΔI_f to R_s is $1/R_s$.

In addition, the analysis of key structure parameters (substrate thinning, ITO, bonding wire, and chip numbers) affecting the thermal characteristics of the chips in board packaging method has been conducted. The thermal simulation results are shown in Figures 5 and 6.

These simulation results show that the thinning processing for Al_2O_3 substrate of LEDs without ITO from 300 μm to 20 μm decreased the LED temperature by approximately 10 K, as demonstrated in Figure 5(a) (maximum temperature is 314.9 K) and Figure 5(b) (maximum temperature is 305.3 K). The introduced ITO for LEDs, with 300 μm Al_2O_3 substrate, changed the positions of maximum temperature. The LED temperature will also decrease as seen in Figure 5(b) (maximum point is 314.9 K at the p-pad region) and Figure 5(c) (maximum point is 305.7 K at the n-pad region), which may explain the low sheet resistance (less than 50 Ω/°C of the ITO). The bonding of gold wires to the LEDs decreases by approximately 3 K (Figure 5(d) (maximum point is 317.84 K) and Figure 5(e) (maximum point is 314.72 K)). The thermal resistance of the packaged LEDs or total equivalent thermal resistance R_t, where $R_t = (T_j - T_a)/(P_{\text{th}}) \cdot T_j$ denotes the maximum of the junction temperatures. T_a is 300 K, and P_{th} is the total thermal power, decreasing with the increase in chip numbers, $n \in [1, 2, \ldots, 15]$. The decrease rate gradually slows down when n is greater than 5 and the simulation results are seen in the "simulation" line of Figure 6 (compared with the thermal circuits theory results [4], as seen in the "theory" line). This implies that the multiple chips package leads to the parallel effect of LED thermal resistances. Furthermore, the conductive coefficients of the external sink, intermittent layer, GaN material, and so on are the temperature sensitivities. Therefore, increasing the number of chips enhances the background temperature



(a) 20 um substrate without ITO (b) 300 um substrate without ITO (c) 300 um substrate with ITO

(d) LEDs with bonding wires (e) LEDs without bonding wires

Figure 5: Temperature distribution simulations.

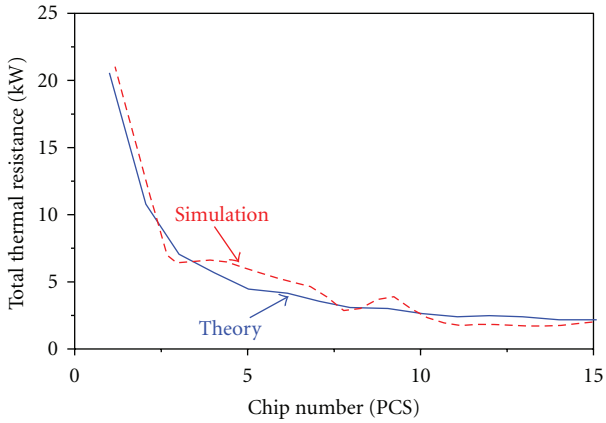


Figure 6: Relationship between the chip number n and total thermal resistance R_t.

of one of the LEDs, which benefits the decreasing thermal resistance of the LED attributed to the decreasing conductive coefficients when the temperature is increasing.

4. Conclusion

In this paper, the multi-physics and multiscale simulation model for the chips in board packaging method is presented, and the current density and temperature distribution are also discussed. The built and optimized COMSOL model can simulate the electrical-thermal characteristics of the LED array. The R_s, n_{ideal}, and I_s parameters match, substrate thinning, and structure optimization are likely to get a junction temperature decrease by about 3 K to 10 K. The chip number larger than 5 is another approach to further optimize the performance of the chips in board packaging technique.

Acknowledgments

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