Review Article

Sigma-Delta Modulation Based Digital Filter Design Techniques in FPGA

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In this paper efficient digital filter design techniques categorized as sigma-delta modulation based short word length (SWL) and multibit (or contemporary) techniques are reviewed in terms of hardware complexity, area, performance and power tradeoffs, synthesis issues, and algorithm versatility. More recent, general purpose DSP applications including classical LMS algorithms reported using sigma-delta modulation encoding are reviewed thoroughly. A small number of basic arithmetic circuits designed using sigma-delta modulation encoding and synthesized by using FPGAs are also described. Finally, recent FPGA based area-performance-power analysis of single-bit ternary FIR filtering is discussed and compared to its corresponding multi-bit system. This work shows that in most cases single-bit ternary FIR-like filters are able to outperform their equivalent multi-bit filters in terms of area, power, and performance.

1. Introduction

It is no surprise that many signal processing tasks can be accomplished by a microprocessor or a digital signal processor (commonly called DSP kits). Built-in multiplication modules are the core element of these devices. Furthermore, implementation of multiply and accumulate (MAC) circuits within signal processors can significantly improve the throughput of FIR and IIR digital filters structures (see Figures 1 and 2) that require a large number of multiply and accumulation operations per a sampling period.

An alternative solution is to use gate-level programmable devices such as field programmable gate arrays (FPGAs) to perform the digital filtering tasks. Concurrent (i.e., parallel) mode of operations of these devices is of great interest as it can improve the throughput of the digital signal processing circuits especially digital filtering modules. This higher throughput can be achieved at the cost of a higher chip area compared to the serial implementation of the circuits. Many of these FPGA devices include a number of built-in multipliers that take up a large amount of silicon area within the device. Further, the most recent FPGA devices include resources that easily support general purpose signal processing tasks even within mid-range commercial devices.

However, there is a direct tradeoff between chip area and throughput in these devices. Some obvious applications that require fast and efficient digital filters are decimation filters, audio filter banks, charge-coupled-device filters, and software defined radio, all of which require high throughput. To achieve fast and efficient implementations, many techniques have been proposed. The overarching theme of these techniques has been to reduce the complexity of the multiplication process in any possible way. One method of reducing the complexity of the multiplier is to reduce the word length in both the input and the filter coefficients. A preferred approach is to utilize the sigma-delta modulation to reduce the word length; this paper focuses on these methods. There are many techniques that use some form of sigma-delta modulation or the like to improve the efficiency of the digital filtering operations. Examples of such techniques were reported in [1–9]. In this paper we thoroughly examine the design and synthesis of such techniques including general purpose short word length (SWL) DSP techniques and its VLSI analysis in FPGA systems.

The remainder of this paper proceeds as follows. Fast FIR filters are discussed in Section 2, followed by short word length (SWL) design techniques in Section 3. In Section 4, the VLSI analysis of sigma-delta modulation based general

FIGURE 1: General structure of FIR filter.

FIGURE 2: Block Diagram of an IIR direct form II filter.

purpose arithmetic modules and single-bit ternary FIR-like filtering is covered. In Section 5, we describe a multibit hardware-efficient FIR filter design techniques that can be employed for single-bit purposes as well. Finally, we summarize and conclude the paper.

2. Fast FIR Filters

Fast and efficient filters generally fall in two classes: sigma-delta modulation ($\Sigma\Delta$) based and optimization techniques within a multibit format. A brief description of both these methods is given below.

2.1. FIR Filter Optimization Techniques. This section describes input and coefficient encoding techniques that can be exploited to implement fast and efficient DSP algorithms in FPGAs. The techniques can be applied in either a single-bit or multibit environment [10, 11].

As outlined above, it is the performance of the multiply-accumulate (MAC) stages that will have the greatest impact on the overall behaviour of digital filters. Thus, various filter design techniques have been proposed that specifically target the complexity of these stages. For example, distributed arithmetic is a common technique that has been used in FPGA designs for many years [12, 13] in which the multiplication stages are performed using look-up tables (LUTs), thereby reducing the overall size of the hardware. In [14], Systolic Distributed Arithmetic was used to improve the area-performance-power tradeoffs of a FIR filter design implemented on a Xilinx Virtex-E device at various filter orders but with a fixed coefficient bit width (i.e., $L = 8$). It was

observed that the best tradeoffs between area-performance and power can be achieved at an address length of four.

Many other techniques have been proposed: Canonical Sign Digit (CSD) [15], the Dempster Method [16], Mirror Symmetric Filter Pairs [17], two-stage parallelism [18], and Redundant Binary Schemes [19] to name just a few. Methods specifically aimed at FPGA based FIR filter implementations include the fully pipelined and full-parallel transposed form [20], Add-and-Shift method with advanced calculation [21], and hardware efficient distributed arithmetic for higher orders [12, 13]. In [18], a new design technique based on a linear phase prototype filter that exploits coefficient symmetry was shown to offer better performance at a hardware cost similar to that of linear phase filters. Further, [18] also described a transpose direct form with CSD multipliers that offers better area-performance tradeoffs when using classical methods.

Apart from the classical multiplier complexity reduction techniques, a new approach called Slice Reduction Graphs (SRG) [20], which reduces area by minimizing the multiplier block logic depth and pipeline registers, has been shown to offer improved area-performance over the Reduced Adder Graph (RAG) and Distributed Arithmetic (DA) techniques. In [20], simulations were carried out at coefficient bit widths in the range of 2–20 bits, while keeping the order of the filter constant (i.e., at 51). The order of the filter was then varied in the range 10–250 at fixed coefficient bit widths. The maximum average operating frequency achieved by the proposed technique was in the range of 175–180 MHz at the lowest filter order, further reducing towards 150–160 MHz as the filter order increased above 60.

The primary intent of the techniques mentioned above has been to improve the area-performance characteristics of parallel multibit binary filters operating at the Nyquist rate. However, it is obvious that the format of the coefficients and input data is one reason for the high complexity of the MAC stages. In [22–24], the complexity of the filter coefficients has been addressed by employing a simple single-bit coefficient format. This technique can reduce the hardware complexity of multipliers to simple AND-OR logic or small look-up table (LUT) organizations. In the subsequent sections, we have discussed such techniques which utilize sigma-delta modulation to reduce the complexity of digital filter MAC section and improve the performance of those circuits.

2.2. Sigma-Delta Modulation Based Fast Filters. Much work has been reported on the design and implementation of the sigma-delta modulation based FIR and IIR filters encompassing various forms. The work that was commenced by the authors in [22] and progressed by the ones in [8, 24] has been reported by many, such as in [1–4, 7, 25–28]. More recently sigma-delta modulation based bit-stream adder and multiplier modules have been described in [29, 30].

In [4, 7, 25], efficient FPGA implementations of narrowband FIR filters are achieved by simplifying the MAC operation using a lower precision input to the filter. This filtering operation requires that the input to the filter should be oversampled and requantized through the error feedback $\Sigma\Delta$ as shown in Figure 3. In this case, a distributed

FIGURE 3: Block diagram of the error feedback $\Sigma\Delta M$ for requantization.

arithmetic (DA) approach was used to design an error prediction FIR filter that has been placed in a negative feedback path (see Figure 3). This prediction filter has a flat pass band and a leading phase shift in the band of interest. The work also discusses the optimum prediction filter design based on statistics and a minimum-mean-squared error (MMSE) calculation. For a FIR filter input, only 3-4 bits in the requantizer output were processed as compared to the original 16-bit input bit-stream to the $\Sigma\Delta M$ (i.e., requantizer).

Overall, an efficient implementation of a narrowband digital filter through a requantizing operation has shown a 50% reduction in logic resources as compared to a traditional FIR filter implementation using an FPGA. This filter shows a great promise for FIR filter implementation. Further reduction in complexity can be gained through harsher requantization to lower precision words.

In [8, 24] fast and efficient FIR filters are presented. The authors discussed two sigma-delta filtering approaches. In the first approach, FIR filter coefficients are encoded using first-order sigma-delta modulator. Hence, the input to the filter must be interpolated and zero-padded to R times the sampling frequency. An efficient two-step interpolation process was proposed that required firstly interpolating the original signal (x_n) by 4 times, at a sampling frequency of $4f_N$ resulting in x_{of} . This signal (x_{of}) was then upsampled by $R/4$ times (R is the typical OSR) to give $\hat{x}_n$ by appending zeros. The proposed structure is shown in Figure 4. The decoder for this filter is used to reconstruct the original signal by resampling to the Nyquist rate and removing quantization noise by using a low pass filter and decimator.

The use of cascaded comb filters as reported in [31] was adopted to further simplify the decoder design whilst removing any alias introduced into the system from the FIR filter. Only two cascaded comb filters were used in this design (shown in Figure 5) because it was found that using more than two cascaded comb filters did not improve the tradeoff between signal-to-noise ratio of the coded output and the OSR.

In a second approach (Figure 6), input data was encoded into single-bit format through sigma-delta modulator whereas the filter coefficients were kept in PCM format.

FIGURE 4: Block diagram of the FIR filter with $\Sigma\Delta M$ modulated filter coefficients.

FIGURE 5: Block diagram of the decoder used in a FIR filter with $\Sigma\Delta M$ modulated filter coefficients and with $\Sigma\Delta M$ modulated input signal.

The decoder for this structure was identical to the one shown in Figure 5. Signal encoding with sigma-delta modulation worked as an ADC and single-bit coder so there is no longer a requirement for a conventional ADC. Further, no input interpolation is required in this setup as the signal passing through $\Sigma\Delta M$ will be oversampled.

To perform the filtering operation, full precision filter coefficients were zero padded by R to match the oversampling ratio of the $\Sigma\Delta M$. Decoder circuits comprising cascaded comb and baseband filters were used to remove the quantization noise and aliases from the filtered output signal. However, the output signal was in a multibit format in all of these schemes.

In [8] the authors also propose a fully sigma-delta modulated FIR filter. In this instance, it was recognized that the filter performs well if both the input and filter coefficients are sigma-delta encoded in a single-bit format. A similar structure was utilized to that shown in Figure 4 except that the interpolator was replaced with a sigma-delta modulator. It was found using simulation that the design exhibits a flat input spectrum in the Nyquist frequency range and the latter approach (Figure 6) performed well in comparison to the former (Figure 5). This structure was found to further reduce the hardware complexity of the filter implementation.

A ternary format has an extra symbol for input and filter coefficients and has been found to offer better stop band attenuation and dynamic range flexibility compared to the binary format [8, 32]. While that work illustrates the potential benefits of ternary encoded filters, the final decoder leaves the output in a multibit format that again requires complex hardware to process.

FIGURE 6: Block diagram of the FIR filter with $\Sigma\Delta$ modulated input signal.

A slightly different fast and efficient FIR filter design using sigma-delta encoding is presented in [27] in which a Look-Ahead Decision Feedback (LADF) approach is used to encode the filter coefficients into a single-bit format. In that work, the proposed technique is compared with two other $\Sigma\Delta$ architectures: the multistage (MASH) and double loop (DSM2). It was found that the proposed architecture outperforms in comparison to double loop but has poor performance against the MASH architecture. Given the lower complexity implementation of the proposed architecture, the author argues that the method is appropriate for filter encoding. However, the quantizer stage with LADF architecture is more complex than the single-bit quantizer and its associated $\Sigma\Delta$ architecture.

The last group of fast and efficient filters designs uses a canonical signed digit (CSD) quantizer with signed powers of two $\Sigma\Delta$ output [26]. It is argued that the CSD quantizer provides many more quantization levels than a single-bit quantizer, which suits the linear modelling of the system design and can improve the system stability. Thus an output in CSD format obtained from the $\Sigma\Delta$ can be used as the FIR filter coefficients and the multiplication operation becomes simple shifts. Another promising scheme presented in [33] uses a slightly more complex architecture but is essentially the same technique.

3. FIR Filter Encoding Using Sigma-Delta Modulation

Regardless of the many optimizations that have been proposed, a large number of multiplication stages is still translated into a large area, delay, and power consumption. One-bit $\Sigma\Delta$ modulators are widely used in AD and DA conversion stages due to their inherent linearity and precision. However, it is less common for the entire digital processing path to operate on single-bit data. The more usual approach has been to decimate the signal data stream after conversion and for the remaining processing to be performed in a standard

binary at the Nyquist rate and with a resolution mandated by dynamic range and noise considerations.

Sigma-delta modulation ($\Sigma\Delta$) encoding of the FIR filter coefficients has been shown to be an efficient way to reduce the complexity of the multiplier and improve its area-performance tradeoffs [34]. The simple arithmetic of single-bit DSP systems results in efficient hardware implementations that map well to FPGA resources, which tend to comprise multiple flip-flops plus simple logic blocks and/or look-up tables. The advantages of single-bit systems were first identified by the authors of [22] and further developed in [23, 24] and [26]. Recently, general purpose short word length (SWL) DSP applications including classical LMS algorithms have been described in [10, 35]. In this section we introduce and describe the techniques that have been used to filter whilst maintaining a single-bit output. This section is further divided into two sections, that is, simulation based single-bit techniques and their VLSI analysis.

3.1. Single-Bit FIR Filter Design Techniques. As the name suggests the single-bit filters produce a single-bit output. In the last decade various general purpose DSP applications are reported using single-bit sigma-delta modulation encoding including classical FIR filter in [10, 35–38]. This single-bit approach was first reported for IIR and FIR filtering in [2, 3].

In [3], a single-bit FIR filtering technique is proposed with bit-stream input and fixed or floating point coefficients similar to the one reported in [8, 24]. However, the major contribution is the replacement of the decoder in [8] by a $\Sigma\Delta$ that has a low pass signal transfer function. The single-bit FIR filter as proposed in [3] is shown in Figure 7.

Similarly, in the second approach presented in [24], the input is assumed to be in a single-bit format, while full precision filter coefficients are generated at the Nyquist rate. This newly generated impulse response was interpolated by R times, where R is the oversampling ratio of the input signal, via zero-interleaving. The R aliases that were introduced due to zero-interleaving in [24] were removed by a decoder comprised of cascaded comb filters and a baseband filter. However, in [3] a $\Sigma\Delta$ was used instead of a decoder. This $\Sigma\Delta$ was used to remove the aliasing created by the zero-interleaving process and served to remodulate the multibit output signal from the FIR filter back into the single-bit domain.

The VLSI analysis of the proposed design was carried out and the single-bit design was found to be more efficient in terms of silicon resources than a PCM digital filter up to 80 taps. The structure still has the complexity of a full precision filter coefficients, which can also increase the word length of the FIR filter output.

The remodulator complexity is discussed by the same authors in [39]. Digital $\Sigma\Delta$ low pass frequency responses are typically not easy to find in the current literature. A fourth-order $\Sigma\Delta$ was used for this purpose with various powers of two multiplications that created more complex SDM structure than a standard one. Therefore, the low pass modulator structure presented in [39] is very complex for single-bit filters.

FIGURE 7: Block diagram of the single-bit FIR filter.

The core idea of the IIR single-bit $\Sigma\Delta$ presented in [2, 40] is to multiply a one-bit oversampled input signal with a multibit fixed coefficient. The resulting multibit output must be applied to a sigma-delta modulator to get back the single-bit output. Initially the model was tested without the feed-forward integrator which resulted in a large noise gain due to its higher oversampling ratio transfer function. A modified version with an integrator inside the loop that resulted in noise reduction and kept the STF and NTF the same is shown in Figure 8. In this model, the $\Sigma\Delta$ is assumed to be a single delay element; hence, the system is a basic first-order recursive filter [2, 40].

The stability of the system in Figure 8 was assumed to be determined by a rule of thumb with an assumption that second-order sigma-delta modulators will remain stable. But due to an extra integrator inside the loop, the overall NTF becomes equivalent to a third-order $\Sigma\Delta$, making it more difficult to analyse the stability of the overall system [2]. Therefore, this system was not further studied by those authors.

However, a quasi-orthonormal state space IIR architecture was shown to have good filtering abilities with good stop band attenuation by the same authors in [41]. The downside of this structure is that it requires N $\Sigma\Delta$ blocks for an N th-order IIR filter and the structure becomes very complex as the order number increases. The proliferation of $\Sigma\Delta$ blocks only adds to the quantization noise in the band of interest and makes any stability analysis very difficult [2].

Recently, new DSP design techniques called short word length (SWL) have been reported in [10, 11, 38, 42]. Of

FIGURE 8: Block diagram of the first-order single-bit IIR filter.

FIGURE 9: General block diagram of the single-bit ternary FIR-like filter.

these SWL techniques, the so-called single-bit ternary FIR filter was first proposed in [10]. This design comprises two parts: the ternary filter and the IIR remodulator, as shown in Figure 9. A new method to generate the single-bit ternary filter was also proposed that starts with the selection of the target impulse response. This target impulse response must undergo an interpolation stage before the ternary sigma-delta modulated form of the filter can be generated. The generated ternary format of coefficients must have flat pass band frequency response in the frequency band of interest (i.e., $0 \rightarrow f_0$). The transfer function of the overall design was derived and the filter was simulated at a number of OSR values. It was found that the resulting single-bit filter produced an equivalent output to the target impulse response. Hence, it appears that single-bit ternary filters can take over from the bulky multibit systems that include complex multiplication.

Using the same approach, a narrowband band pass $\Sigma\Delta$ was proposed in [11] (Figure 10). Again it comprises two parts: the ternary filter followed by the remodulation of the multibit into single-bit format. Unlike the low pass single-bit filter, these authors have proposed a remodulation by a simple band pass $\Sigma\Delta$ that has efficient architecture and less stability sensitivity compared to the IIR remodulator. Coefficients were encoded into a ternary format by passing the band-pass target impulse response through an 8th order $\Sigma\Delta$ with optimum coefficients. Through MATLAB simulation it was found that the overall frequency response of the proposed method was very similar to the original target impulse response.

The performance of the proposed method is also discussed in [43]. It was found that FFT and spline interpolation

FIGURE 10: Single-bit narrowband bandpass FIR filter.

techniques offer superior stop band attenuation performance to other techniques. Following the same approach, single-bit resonators and BFSK demodulator designs have been reported in [37, 44]. However, this short word length approach was not verified through hardware synthesis nor was its area-performance-power compared with contemporary multibit techniques. Furthermore, that work does not extend to a rigorous stability analysis of the SWL filtering techniques.

Further to this work, an LMS-like single-bit adaptive filtering structure for noise cancelling has been presented in [35, 42, 45], in which all input, output, and filter coefficients are in a single-bit format. Overall, three short word length adaptive structures were proposed: namely, ternary, single-bit, and 2 bit. The overall weight vector equation was derived by using block LMS algorithm which has advantage of accommodating more data samples and better performance than a sample-by-sample LMS algorithm. Through MATLAB simulation it was found that short word length (SWL) adaptive filter (i.e., 2-bit format of coefficients) has a superior performance than the others, that is, single-bit and ternary, at the cost of prospect more chip area.

However, much work is still needed to explore the design using random inputs within a higher noise environment. In addition, it is still unclear what might be the optimum coefficient update rate or range of the convergence parameter (μ) or shape of the learning curves.

4. VLSI Analysis of $\Sigma\Delta$ Based Bit-Stream Circuits

Although much work has been reported on the design and analysis of single-bit systems, it appears that there has been little reported on rigorous hardware analysis of single-bit signal processing techniques using FPGAs. However, a small range of work has been reported on VLSI synthesis and analysis of bit-stream arithmetic modules and its variants that are further covered below. These arithmetic modules are building blocks of DSP algorithms but not a signal processing application itself. Furthermore, these modules have been an inherent part of the single-bit systems already proposed in [10, 35].

In [6, 46] efficient bit-stream (i.e., single-bit) arithmetic modules are presented for mobile communication in which general purpose modules including adder, multiplier, divider, and square root have been designed. A typical QPSK communication model has been demonstrated by using the proposed bit-stream arithmetic modules and a 40% reduction in logic gate count compared to conventional design has been reported.

Bit-stream arithmetic modules with bi-, tri-, and quad levels are described in [30, 32, 47, 48]. In these cases,

hardware implementation of the arithmetic modules is done in Xilinx Virtex-5 using two's complement representation. The synthesis results demonstrated that there is a significant improvement in the signal-to-noise ratio and performance with ternary format than binary at the cost of a more complex structure [32]. Bit-stream (i.e., single-bit) ternary and multibit approaches have been compared in FPGAs by synthesizing a type I digital phase locked loop (DPLL) application using a direct digital synthesis approach [49]. The bit-stream ternary approach was found to be more resource efficient than its corresponding multibit system [32].

In [47, 48], an efficient implementation of bit-stream adders and multipliers modules has been reported in FPGAs. In [47], a (4, 2) adder structure (i.e., 6-input (4 + 2)) was exploited that better suited the Altera and Xilinx 6-input LUT architectures than a conventional (2, 1) architecture. The proposed adder structure resulted in a 50% reduction in LUT count and a 20% higher clock frequency [47]. In [48], the trilevel bit-stream was extended to quad level and compared to the sorter based approach [50]. The quad-level bit-stream adder and multiplier presented in [48] were encoded using 2 bit and the truncated third bit was fed back to the adder to suppress the truncation error. Through Xilinx FPGA synthesis, the proposed adder and multiplier have shown a significant improvement in area-performance compared to the sorter approach [50]. This quad-level adder approach resulted in about a 76% LUT reduction and a 93% higher clock rate, while the proposed bit-stream multiplier showed a 82% LUT reduction and 122% higher clock frequency [48].

Regardless of the work reported on simple arithmetic modules, the drawback to all of these reported works is the limited range of their adder and multiplier modules (i.e., $L = 4$). Further, there has been no detailed comparison provided to its corresponding multibit system except for one example reported in [32]. From the general behaviour of multibit versus single-bit systems, it can be predicted that there may be a cross-over point between the two approaches, where one could be preferred over the other. This idea will be addressed later in the work.

Unlike [32, 47, 48], in [30] an existing IIR low pass filter $\Sigma\Delta$ is utilized to generate the input bit-stream and the design has been analysed to characterise the selection of the $\Sigma\Delta$ design parameter (i.e., K , shown in Figure 11). The design was extended to tri- and quad level and compared with the bilevel $\Sigma\Delta$. The noise performance was simulated for all three types of multipliers and it was found that trilevel design has a performance gain of 11.2 dB over the bilevel design, while the quad-level design has about a further 8.8 dB gain over the trilevel design [30].

Hardware implementation of all three designs was performed using the Xilinx Virtex-5 FPGA and the area-performance characteristics of the multiplier were noted. The synthesis results show a direct tradeoff between all the three designs and the two approaches for the IIR and FIR filter modules. These results indicate that the bilevel design is more resource efficient than either of the tri- and quad level and provides a higher performance at the cost of lower noise suppression and vice versa. However, this

TABLE 1: Area-performance comparison of single-bit FIR versus multibit filter: nonpipelined mode.

Device	Single-bit			N	W	Multibit	
	Number of tern. coeff	LUTs	F_{MAX}			LUTs	F_{MAX}
Cyclone-III	512	4089 (3%)	71.4	64	8	8860 (7%)	46.2
	2048	15603 (13%)	52.6		12	17045 (14%)	35.3
	4096	30894 (26%)	45.3		16	26838 (22%)	29.1
	8192	62747 (53%)	40.3		18	32547 (27%)	26.5
Stratix-III	512	3925 (1%)	129.8	64	8	5219 (2%)	86.5
	2048	14368 (5%)	97.3		12	10942 (5%)	69.1
	4096	28499 (11%)	82.8		16	17731 (7%)	57.5
	8192	55927 (21%)	69.6		18	21568 (8%)	51.2

TABLE 2: Area-performance comparison of single-bit FIR versus multibit Filter: pipelined mode.

Device	Single-bit			N	W	Multibit	
	Number of tern. coeff	LUTs	F_{MAX}			LUTs	F_{MAX}
Cyclone-III	512	3963 (3%)	125.6	64	8	9020 (8%)	94.5
	2048	15399 (13%)	122		12	17079 (14%)	67.1
	4096	30607 (26%)	120		16	26890 (23%)	53.3
	8192	61029 (51%)	118		18	32586 (27%)	47.4
Stratix-III	512	3719 (1%)	240	64	8	4923 (1%)	258.3
	2048	14453 (5%)	237		12	10353 (4%)	199.0
	4096	28745 (11%)	237		16	16916 (7%)	158.8
	8192	57362 (21%)	231		18	20662 (8%)	139.7

FIGURE 11: First order digital sigma-delta modulator [30].

assumes that the system was stable by considering the same approach described in [2]. This rule of thumb may lead to an inappropriate solution in real systems [2].

5. A Case Study: FPGA Analysis of Single-Bit Ternary FIR-Like Filter

As discussed earlier much work has been reported on the design and analysis of single-bit ternary FIR-like filters including classical LMS-like filters that are classified in general short word length (SWL) DSP systems. These have tended to be performed using high-level tools such as MATLAB, with little work reported relating to their hardware implementation, particularly in Field Programmable Gate Arrays (FPGAs). Two primary areas of interest exist here. The first is the comparative behaviour of SWL and multibit systems exhibiting equal spectral performance in terms of

their relative area, power, and throughput. The second is that it remains to be determined how chip area-performance varies with varying OSR and bit width of the hardware SWL system.

In [51, 52], a single-bit ternary FIR-like filter (SBTFF) has been designed and synthesized in Quartus-II and ModelSim using VHDL (see Figure 9). The design and implementation of the overall SBTFF have been explored in small commercial FPGAs in order to compare its power-area-performance characteristics with approximately equivalent multibit FIR filters. Both filter types were designed and simulated in pipelined and nonpipelined modes. In this set of simulations, varying OSR (32–256) was used to identify the area-performance-power analysis of two techniques.

Simulation results obtained through the set of experiments are given in Tables 1 and 2. These results are reproduced here that were reported in [52]. In this work, it is shown conclusively that single-bit ternary FIR-like filters are able to consistently outperform their equivalent multibit counterparts in terms of area, power, and performance (i.e., maximum cut-off frequency in a given technology) except at the most extreme filter orders analysed in the work. Typically single-bit ternary FIR-like filter offered reasonable area savings at lower orders and higher performance in all cases in the range of 30%–40% in pipelined and non-pipelined modes.

The power analysis of two filters was performed in two steps using clock obtained from the area-performance results (shown in Tables 1 and 2) and at multibit oversampling clock

rate as proposed in the design of [52]. In both cases it was found that SBTF dissipates lower power as compared to its counterpart multibit system. The work reported in [51, 52] provides an important analysis of the relationship between the oversampling rates, signal-to-noise ratio and chip area. It was also found that increasing OSR increases SNR at the cost of higher chip area.

In [53], three encoding techniques called canonical signed digit (CSD), 2's complement, and Redundant Binary Signed Digit (RBSD) were designed and investigated on the basis of area-performance in FPGA at varying OSR. Simulation results show that CSD encoding technique does not offer any significant improvement as compared to 2's complement as in a multibit domain. In contrast, RBSD occupies double the chip area than other two techniques and has poor performance.

6. Summary

In this survey we have described the work reported on the development of fast and efficient filter designs especially by employing sigma-delta modulation as the encoding technique. Single-bit design techniques have been studied since the early 80s, having been first reported by [54] and further enhanced by [8, 24] and in [2, 40]. Recently, new single-bit signal processing techniques have been introduced. Known in general as the Short Word Length (SWL) approach, it is more suitable to hardware implementations, especially FPGAs.

Though significant work has been reported on single-bit design techniques, few analyses of the VLSI bit-stream circuits appear in the literature. The design, analysis, and FPGA synthesis of arithmetic modules (i.e., adder, multiplier, and divider) were first reported in [46] and further advanced by the authors in [30, 32, 47, 48]. By synthesizing to the Xilinx Virtex-5, a significant improvement in logic reduction was found by using tri- and quad level for the arithmetic modules.

In [51, 52], the authors have synthesized single-bit ternary FIR-like filter (SBTF) in small commercial FPGAs. This work shows conclusively that single-bit ternary FIR-like filters are able to consistently outperform their equivalent multibit counterparts in terms of area, power and performance (i.e., maximum cut-off frequency in a given technology) except at the most extreme filter orders analysed in the work. The work provides an important analysis of the relationship between the oversampling rates, signal-to-noise ratio and chip area.

References

- [1] S. Ghanekar, S. Tantarana, and L. E. Franks, "Design and architecture of multiplier-free FIR filters using periodically time-varying ternary coefficients," *IEEE Transactions on Circuits and Systems I*, vol. 40, no. 5, pp. 364–370, 1993.
- [2] D. A. Johns and D. M. Lewis, "Design and analysis of delta-sigma based IIR filters," *IEEE Transactions on Circuits and Systems II*, vol. 40, no. 4, pp. 233–240, 1993.
- [3] S. Kershaw et al., "Realisation and implementation of a sigma-delta bitstream FIR filter," *IEE Proceedings—Circuits, Devices and Systems*, vol. 143, pp. 267–273, 1996.
- [4] C. Dick and F. Harris, "High-performance FPGA filters using sigma-delta modulation encoding," in *Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP '99)*, pp. 2123–2126, 1999.
- [5] S. S. Abeysekera and X. Yao, "Optimum Laguerre filter design technique for Sigma-Delta demodulators," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. V405–V408, May 2000.
- [6] H. Fujisaka, M. Sakamoto, and M. Morisue, "Bit-stream signal processing circuits and their application," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. 85, no. 4, pp. 853–860, 2002.
- [7] C. Dick and F. Harris, "FPGA signal processing using Sigma-Delta modulation," *IEEE Signal Processing Magazine*, vol. 17, no. 1, pp. 20–35, 2000.
- [8] P. W. Wong, "Fully sigma-delta modulation encoded FIR filters," *IEEE Transactions on Signal Processing*, vol. 40, no. 6, pp. 1605–1610, 1992.
- [9] B. Steele and P. O'Shea, "Design of ternary digital filters," in *Proceedings of the 3rd International Conference on Information, Communication and Signal Processing (ICICS '01)*, Singapore, October 2001.
- [10] A. C. Thompson, P. O'Shea, Z. M. Hussain, and B. R. Steele, "Efficient single-bit ternary digital filtering using sigma-delta modulator," *IEEE Signal Processing Letters*, vol. 11, no. 2, pp. 164–166, 2004.
- [11] A. C. Thompson, Z. M. Hussain, and P. O'Shea, "A single-bit narrow-band bandpass digital filter," *Australian Journal of Electrical and Electronics Engineering*, vol. 2, no. 1, pp. 31–40, 2005.
- [12] R. S. Grover, W. Shang, Q. Li et al., "A faster distributed arithmetic architecture for FPGAs," in *Proceedings of the ACM/SIGDA 9th international symposium on Field-programmable gate arrays in (FPGA '02)*, pp. 31–39, Monterey, Calif, USA, 2002.
- [13] H. Yoo and D. V. Anderson, "Hardware-efficient distributed arithmetic architecture for high-order digital filters," in *Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP '05)*, pp. V125–V128, March 2005.
- [14] P. K. Meher, S. Chandrasekaran, and A. Amira, "FPGA realization of FIR filters by efficient and flexible systolization using distributed arithmetic," *IEEE Transactions on Signal Processing*, vol. 56, no. 7, pp. 3009–3017, 2008.
- [15] Y. Jang and S. Yang, "Low-power CSD linear phase FIR filter structure using vertical common sub-expression," *Electronics Letters*, vol. 38, no. 15, pp. 777–779, 2002.
- [16] A. G. Dempster and M. D. Macleod, "Use of minimum-adder multiplier blocks in FIR digital filters," *IEEE Transactions on Circuits and Systems II*, vol. 42, no. 9, pp. 569–577, 1995.
- [17] S. Shanthala and S. Y. Kulkarni, "High speed and low power FPGA implementation of FIR filter for DSP applications," *European Journal of Scientific Research*, vol. 31, no. 1, pp. 19–28, 2009.
- [18] R. A. Hawley, B. C. Wong, T. J. Lin, J. Laskowski, and H. Samueli, "Design techniques for silicon compiler implementations of high-speed FIR digital filters," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 5, pp. 656–666, 1996.
- [19] T. D. Memon, P. Beckett, and Z. M. Hussain, "Analysis and design of a ternary FIR filter using sigma delta modulation,"

- in *Proceedings of the IEEE 13th International Multitopic Conference (INMIC '09)*, pp. 476–480, December 2009.
- [20] K. N. Macpherson and R. W. Stewart, "Area efficient FIR filters for high speed FPGA implementation," *IEE Proceedings: Vision, Image and Signal Processing*, vol. 153, no. 6, pp. 711–720, 2006.
 - [21] Y. Li, C. Peng, D. Yu, and X. Zhang, "The implementation methods of high speed FIR filter on FPGA," in *Proceedings of the 9th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT '08)*, pp. 2216–2219, October 2008.
 - [22] N. Benvenuto, L. E. Franks, and F. S. Hill, "Realization of finite impulse response filters using coefficients +1, 0, and -1," *IEEE Transactions on Communications*, vol. 33, no. 10, pp. 1117–1125, 1985.
 - [23] P. W. Wong, "Fully sigma-delta modulation encoded FIR filters," *IEEE Transactions on Signal Processing*, vol. 40, no. 6, pp. 1605–1610, 1992.
 - [24] P. W. Wong and R. M. Gray, "FIR filters with sigma-delta modulation encoding," *IEEE Transactions on Acoustics, Speech, and Signal Processing*, vol. 38, no. 6, pp. 979–990, 1990.
 - [25] C. Dick and F. Harris, "Narrow-band FIR filtering with FPGAs using sigma-delta modulation encoding," *Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology*, vol. 14, no. 3, pp. 265–282, 1996.
 - [26] C. L. Chen and A. N. Willson, "Higher order Σ - Δ modulation encoding for design of multiplierless FIR filters," *Electronics Letters*, vol. 34, no. 24, pp. 2298–2300, 1998.
 - [27] S. S. Abeysekera and K. P. Padhi, "Design of multiplier free FIR filters using a LADF sigma-delta (Σ - Δ) modulator," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. I-65–I-68, May 2000.
 - [28] S. S. Abeysekera and C. Charoensak, "Efficient realization of sigma-delta (Σ - δ) Kalman lowpass filter in hardware using FPGA," *Eurasip Journal on Applied Signal Processing*, vol. 2006, Article ID 52736, 2006.
 - [29] C.-W. Ng, N. Wong, and T. S. Ng, "Bit-stream adders and multipliers for tri-level sigma-delta modulators," *IEEE Transactions on Circuits and Systems II*, vol. 54, no. 12, pp. 1082–1086, 2007.
 - [30] C. W. Ng, N. Wong, H. K. H. So, and T. S. Ng, "On IIR-based bit-stream multipliers," *International Journal of Circuit Theory and Applications*, vol. 39, no. 2, pp. 149–158, 2011.
 - [31] J. C. Candy, "Decimation for sigma delta modulation," *IEEE Transactions on Communications*, vol. 34, no. 1, pp. 72–76, 1986.
 - [32] C. W. Ng, N. Wong, and T. S. Ng, "Bit-stream adders and multipliers for tri-level sigma-delta modulators," *IEEE Transactions on Circuits and Systems II*, vol. 54, no. 12, pp. 1082–1086, 2007.
 - [33] S. R. Powell and P. M. Chau, "Efficient narrowband FIR and IFIR filters based on powers-of-two sigma-delta coefficient truncation," *IEEE Transactions on Circuits and Systems II*, vol. 41, no. 8, pp. 497–505, 1994.
 - [34] T. D. Memon, P. Beckett, and Z. Hussain, "Design and implementation of ternary FIR filter using Sigma Delta Modulation," in *International Symposium on Computing, Communication and Control (ISCCC '09)*, pp. 169–173, October 2009.
 - [35] A. Z. Sadik, Z. M. Hussain, and P. O'Shea, "Adaptive algorithm for ternary filtering," *Electronics Letters*, vol. 42, no. 7, pp. 420–421, 2006.
 - [36] A. C. Thompson, *Techniques in Single-Bit Digital Filtering*, RMIT University, 2004.
 - [37] A. C. Thompson and Z. M. Hussain, "A Single-bit Resonator," in *Workshop on the Internet, Telecommunications and Signal Processing (WITSP '04)*, 2004.
 - [38] A. Z. Sadik, Z. M. Hussain, P. J. O'Shea et al., "A single-bit digital DC-blocker using ternary filtering," in *Proceedings of IEEE (TENCON '05)*, pp. 1–6, 2005.
 - [39] S. M. Kershaw, S. Summerfield, and M. B. Sandler, "On $\Sigma\Delta$ signal processing remodulator complexity," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '95)*, pp. 881–884, May 1995.
 - [40] D. A. Johns and D. M. Lewis, "IIR filtering on sigma-delta modulated signals," *Electronics Letters*, vol. 27, no. 4, pp. 307–309, 1991.
 - [41] D. A. Johns, W. M. Snelgrove, and A. S. Sedra, "Adaptive recursive state-space filters using a gradient-based algorithm," *IEEE Transactions on Circuits and Systems*, vol. 37, no. 6, pp. 673–684, 1990.
 - [42] A. Z. Sadik and Z. M. Hussain, "Short word-length LMS filtering," in *Proceedings of the 9th International Symposium on Signal Processing and its Applications (ISSPA '07)*, pp. 1–4, February 2007.
 - [43] A. C. Thompson, P. J. O'Shea, Z. Hussain et al., "Performance of a new single-bit ternary filtering system," in *Proceedings of the 8th Australian Telecommunications, Networks and Applications Conference (ATNAC '03)*, 2003.
 - [44] A. C. Thompson, Z. M. Hussain, and P. O'Shea, "A single-bit digital non-coherent baseband BFSK demodulator," in *Proceedings of the IEEE Region 10 Conference: Analog and Digital Techniques in Electrical Engineering (IEEE TENCON '04)*, pp. A515–A518, November 2004.
 - [45] A. Z. Sadik, Z. M. Hussain, and P. O'Shea, "Adaptive algorithm for ternary filtering," *Electronics Letters*, vol. 42, no. 7, pp. 420–421, 2006.
 - [46] H. Fujisaka, R. Kurata, M. Sakamoto, and M. Morisue, "Bit-stream signal processing and its application to communication systems," *IEE Proceedings: Circuits, Devices and Systems*, vol. 149, no. 3, pp. 159–166, 2002.
 - [47] C. W. Ng, N. Wong, and T. S. Ng, "Efficient FPGA implementation of bit-stream multipliers," *Electronics Letters*, vol. 43, no. 9, pp. 496–497, 2007.
 - [48] C. W. Ng, N. Wong, and T. S. Ng, "Quad-level bit-stream adders and multipliers with efficient FPGA implementation," *Electronics Letters*, vol. 44, no. 12, pp. 722–724, 2008.
 - [49] C. H. Dick and F. J. Harris, "Direct digital synthesis—some options for FPGA implementation," in *Proceedings of the Reconfigurable Technology: FPGAs for Computing and Applications*, pp. 2–10, September 1999.
 - [50] T. Katao, K. Hayashi, H. Fujisaka, T. Kamio, and K. Haeiwa, "Sorter-based sigma-delta domain arithmetic circuits," in *European Conference on Circuit Theory and Design (ECCTD '07)*, pp. 679–682, August 2007.
 - [51] T. D. Memon, P. Beckett, and A. Z. Sadik, "Efficient Implementation of Ternary SDM Filters using State-of-the-Art FPGA," *Mehran University Research Journal of Engineering and Technology*, vol. 30, pp. 207–212, 2011.
 - [52] T. D. Memon, P. Beckett, and A. Z. Sadik, "Power-Area-Performance Characteristics of FPGA based sigma-delta modulated FIR Filters," *Journal of Signal Processing Systems (JSPS)*. In press.
 - [53] T. D. Memon and P. Beckett, "The impact of alternative encoding techniques on the FPGA implementation of sigma-delta

modulated ternary FIR filters,” *Australian Journal of Electrical and Electronics*. In press.

- [54] N. Benvenuto, L. Franks, and F. Hill Jr., “Dynamic programming methods for designing FIR filters using coefficients-1, 0 and+ 1,” *IEEE Transactions on Acoustics, Speech and Signal Processing*, vol. 34, no. 4, pp. 785–792, 1986.