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Research Article

Comparison of Duty Cycle Generator Algorithms for SPICE Simulation of SMPS

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The paper presents and discusses an algorithm for average modeling of the PWM modulator in switch-mode power systems by general purpose electronic circuit simulators such as PSPICE. A comparison with previous theoretical models is conducted. To test the accuracy of the average PWM models comparison to cycle-by-cycle simulation was conducted. The proposed algorithm shows better accuracy than earlier counterparts.

1. Introduction

Today circuit simulation and computer-aided design are universally accepted engineering tools and have become industry standard method of product development. Two approaches are possible for simulation of switched mode systems: cycle-by-cycle simulation and average behavior simulation. Cycle-by-cycle simulation is a quite straightforward approach. Cycle-by-cycle simulation can be performed programming the complete power electronic circuit to the simulator. Cycle-by-cycle simulation allows studding the power stage at the switching frequency scale and observing the instantaneous voltages and currents at any point in the circuit. First disadvantage of cycle-by-cycle simulation is that simulating the detailed switching process is time consuming. This is particularly true for nontrivial practical cases. The second and by far more important limitation is that the cycle-by-cycle model of a switching circuit does not lend itself to frequency response analysis. This is because the switching stage has no stable operating point and, hence, does not allow the PSPICE simulator to perform linearization and calculate the small signal gains required for frequency response analysis. Therefore, a different approach is needed to attain frequency domain simulation of the control loop.

State Space Averaging is a classical theoretical analysis method of switch-mode power electronics systems [1–5]. Average modeling of the power stage can also be helpful in simulation as they can be readily implemented using PSPICE behavioral sources [6–8]. Average models are continuous and, hence, can be automatically linearized by the PSPICE simulator and prepared for the frequency domain analysis. The ability to obtain the frequency response of the feedback loop allows the practicing engineer to evaluate the system's stability and to design the compensator network to meet the design objectives.

The distinct characteristic of SMPS is that a switched-mode stage is employed as power processor, whereas the control circuits are mostly analog where Pulse Width Modulator (PWM) is used as an interface. A typical structure of a PWM switch-mode power system (SMPS) is illustrated in Figure 1 [8]. Here, as an example, an average current mode (ACM) system is shown. There are two major challenges in simulation of a switch-mode system. The first is modeling the switcher, whereas the second is modeling the PWM modulator. To model the average behavior of switch mode power stages Switched Inductor Model (SIM) was proposed [6–8], whereas the PWM duty cycle generation process can be modeled by software Duty Cycle Generator (DCG) approach [8]. The PWM modeling problem is that in practice the switching ripple propagates into the control loop and affects the switch on and off times. However, the average SIM model has no ripple components; therefore, in order to obtain accurate

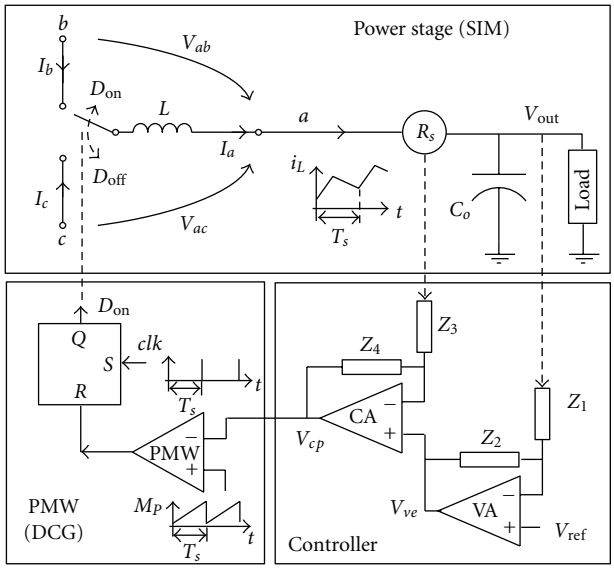

Figure 1: A typical ACM SMPS. Modeling the SMPS requires the SIM to model the power stage and the DCG to model the PWM [8].

simulation results, software DCG should be programmed to predict the switching ripple effects using only the average signals of the SIM model. Another task of the DCG is to anticipate the mode changes of the power stage and calculate the correct off duty cycle in case of CCM-DCM transition.

This paper proposes a more precise, PSPICE compatible, average DCG algorithm for modeling the PWM comparator. The operation of the proposed average PWM model is demonstrated by time domain and frequency domain simulations. The paper also conducts a comparison with previously reported results. To validate the model's accuracy, the proposed average algorithm and its earlier counterparts are compared to cycle-by-cycle simulation. Particularly, in the discontinuous current mode the proposed algorithm shows better accuracy than earlier counterparts.

2. Software Duty Cycle Generators

2.1. PWM Relationships. In recent years ACM control has become the method of choice for many advanced SMPS. The principle of ACM is to implement a multiloop control system in which the inner loop (see Figure 1), controls the average current and makes it tightly follow the outer loop command. The inner/current loop amplifier, CA, provides higher gain in the low-frequency region and extends the inner loop bandwidth. These features are very desirable and provide good tracking performance.

Usually, the average current loop amplifier (CA) is designed to have a high/low-frequency gain and a flat response in the vicinity of the switching frequency as shown in Figure 2 [9]. Consequently, the current programming signal at the output of CA, v_{cp}, has an average component, $\langle v_{cp}\rangle$, with a superimposed attenuated inductor current ripple, as shown in Figure 3. The ripple is scaled by the gain of the

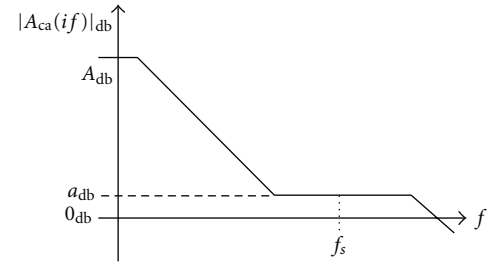

Figure 2: The inner loop amplifier, CA, frequency response.

current sensing network, R_s, and the CA amplifier gain at the switching frequency, $a = |A_{ca}(f_s)|$.

Referring to Figures 1 and 3, the switch on time is initiated by a clock pulse and terminated by the PWM comparator at the moment the current programming signal, v_{cp}, intersects the external ramp. The comparator is usually followed by a latch, which remains reset till the end of the switching cycle and prevents output chatter. A real world comparator uses instantaneous ramp and CA output voltages, whereas in the average system represented by SIM these variables do not exist. The essence of the modeling problem is to accurately determine the on duty cycle, D_{on}, relaying on the knowledge of the average CA output voltage, $\langle v_{cp}\rangle$, the ramp amplitude, V_p, and other average system parameters.

Let the external, charging, and discharging slopes of PWM comparator input signals (see Figure 3), be defined following the notation of [8]:

$$\begin{aligned} S_e &= \frac{V_p}{T_s}, \\ S_{on} &= \frac{aR_s}{L} V_{ab}, \\ S_{off} &= \frac{aR_s}{L} V_{ac}, \end{aligned} \tag{1}$$

where (see Figure 1) V_{ab} and V_{ac} are the SIM terminal voltages; L is the SIM inductor value; T_s is the switching cycle; V_p is the external ramp peak voltage; a, R_s are as defined above.

The intersection instance of current error amplifier and the ramp voltages (see Figure 3) uniquely determines the on duty cycle, D_{on}, as well as all the average quantities for the given switching cycle. Investigating the modulator waveforms of Figure 3(a), and applying basic geometrical considerations to calculate the area under the v_{cp} curve, as suggested in [10], reveals that the average current programming signal, $\langle v_{cp}\rangle$, D_{on} and D_{off} duty cycles and other circuit parameters are related as follows:

$$\begin{aligned} \left\langle v_{cp} \right\rangle = T_s \Bigg[& S_e D_{on} + \frac{S_{on} D_{on}^2}{2} + \frac{S_{off} D_{off}^2}{2} \\ & + S_{off} D_{off} (1 - D_{on} - D_{off}) \Bigg]. \end{aligned} \tag{2}$$

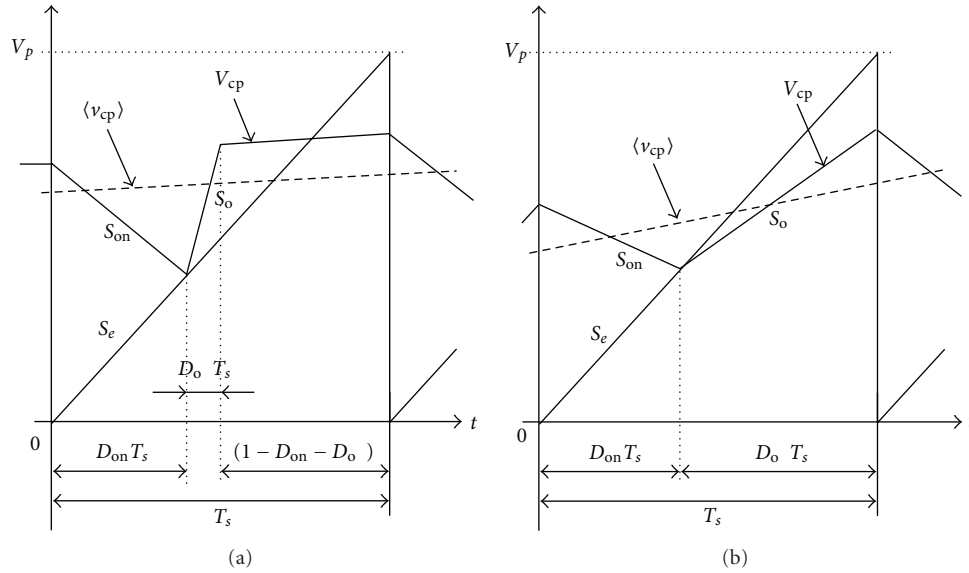

Figure 3: PWM comparator input waveforms in DCM (a) and CCM (b) modes.

The required on duty cycle, D_{on}, is the solution of the quadratic equation (2), which takes into consideration the CA average current programming signal $\langle v_{cp}\rangle$ as well as other operating conditions. The switcher terminal voltages are imbedded in the slopes S_{on} and S_{off}, as defined in (1), whereas D_{off} in DCM depends on D_{on} as well as on the average current and system's parameters.

2.2. Comparison with Other Theoretical Results. The proposed software DCG algorithm (2) can generate the required average duty cycle, D_{on}, in the steady state, in transient conditions, CCM or DCM modes.

Inspection of (2) reveals that under CCM conditions, the term $(1 - D_{on} - D_{off})$ vanishes and (2) is reduced to the expression, previously reported in [10]:

$$\left\langle v_{cp}\right\rangle = T_s\left[\ S_eD_{on} + \frac{S_{on}D_{on}^2}{2} + \frac{S_{off}D_{off}^2}{2}\ \right]. \tag{3}$$

DCG based on (3) can be used in CCM under transient conditions for which S_{on} and S_{off} may assume an arbitrary value. Obviously, with the term $(1 - D_{on} - D_{off})$ missing, (3) is less accurate than (2) in DCM.

Considering that the power stage is operating with slow varying signals in the vicinity of the CCM steady-state equilibrium so that $S_eD_{on} \approx S_{off}D_{off}$, (2) takes the following form:

$$\left\langle v_{cp}\right\rangle = T_s\left[\ S_eD_{on} + \frac{1}{2}S_{on}D_{off}\right], \tag{4}$$

which is identical to that suggested in [11].

For a CA amplifier with a significant attenuation of the switching ripple, $S_e \gg S_{on}$, S_{off}, (2) is further simplified yielding

$$\left\langle v_{cp}\right\rangle = T_sS_eD_{on}, \tag{5}$$

which is identical to the classical Voltage Mode PWM function [12].

2.3. On Duty Cycle Programming. Algorithms (2)–(5) are arranged in a descending order of accuracy and programming complexity. Explicit solution for D_{on} duty cycle could be obtained from (4) and (5). The case of (5) could be implemented in PSPICE by a simple "E" source yielding D_{on} duty cycle, *coded in voltage* at the output. The "E" source should have a gain constant $(1/V_P)$ and controlled by a single input variable, that is, by the average current programming signal $\langle v_{cp}\rangle$:

$$D_{on} = \left(\frac{1}{V_p}\right)\left\langle v_{cp}\right\rangle. \tag{6}$$

The modulator model (6) totally disregards the ripple component. As it is clearly shown at Figure 3, (6) aims at the intersection of the ramp and the average CA voltage, $\langle v_{cp}\rangle$, somewhat to the right of the correct value of D_{on}, thus, providing only an approximate results for both the CCM and the DCM modes. Therefore, (6) is generally recognized as a simplistic model that can be used under low current ripple conditions arising in Voltage Mode converters, whose loop gain provides heavy attenuation of the switching ripple.

Implementation of (4) requires E-value source performing a division:

$$D_{on} = \frac{\left\langle v_{cp}\right\rangle}{V_p + kV_{ab}}. \tag{7}$$

Here, the constant $k = aR_s/2Lf_s$, V_p, and the switching frequency, $f_s = 1/T_s$, should be defined as parameters in PSPICE program. This result is analogous to that suggested by [11]. DCG programmed according to (7) is relatively simple; however, it accounts for the current ripple. Implementation of (7) requires an E-value source governed by two

control variables $\langle v_{cp} \rangle$ and V_{ab}. Note that application of (7) requires a preliminary calculation or simulation to correctly establish the system constant k [7, 8].

A different programming approach is required in order to apply the nonlinear DCG algorithms (2). Using (1) and rearranging terms, the proposed DCG algorithm (2) could be realized as follows:

$$D_{on} = \frac{\left\langle v_{cp} \right\rangle - kV_{ac}D_{off}(2 - 2D_{on} - D_{off})}{V_p + kV_{ab}D_{on}}. \quad (8)$$

Due to its relative complexity, the proposed DCG implementation (8) is hardly useful as an analytical tool; however, PSPICE can obtain a numerical solution of recursive equations of the $D_{on} = f(D_{on}, \ldots)$ type. Equation (8) holds several advantages for simulation purposes. First is that accurate D_{on} duty cycle could be generated of the given average current programming signal, $\langle v_{cp} \rangle$, and the average SIM terminal voltages V_{ab} and V_{ac}.

As suggested by [6], in order to take account of the DCM-CCM mode transitions frequently encountered in switch-mode systems, the Don generator should also be accompanied by the Doff software generator. A quick reference to Doff generator programming is given in the Appendix.

3. Simulation Results

3.1. Comparison of the DCG Algorithm's Performance through Simulation. In order to compare the performance of the previously described software duty cycle generator algorithms, a PSPICE simulation program was created. The program simulated the time domain response of an ACM dc-dc boost converter in DCM and CCM regimes. Simulation diagram of the circuit is shown in Figure 4(a). The circuit parameters were input dc voltage 12 Vdc, output dc voltage 48 Vdc, boost inductor 200 uHy, switching frequency 100 kHz, peak ramp voltage 5 Vpk. Other circuit parameters are given in the diagram. The circuit was commanded to operate in the DCM and in CCM modes by appropriately stepped current reference signal. The simulation was run cycle-by-cycle to obtain the exact time domain behavior of a real circuit. The obtained results were used as a reference for comparison. The average values of the current amplifier output signal and the inductor current were obtained by heavily filtering. The filtering was done using ORCAD lowpass filter ABM blocks with passband attenuation of 1 db up to 75 kHz, whereas attenuation of 50 db was attained at 100 kHz which effectively removed the switching ripple components. The so-obtained averaged variables were used to command the average models of the DCG generators according to (6), (7) and (8). Doff duty cycle was obtained using (A.5) as described in the Appendix.

The simulated waveforms of the key variables in both the DCM and the CCM modes are shown in Figures 4(b)–4(e). The normalization of the saw-tooth ramp and the current programming signals was done relatively to the peak ramp voltage, V_p. The average duty cycles, generated from the averaged variables, were compared to the waveforms of the cycle-by-cycle-simulated PWM comparator. The closer the average D_{on} signal is to the intersection point of the ramp and CA voltage, the accurate the D_{on} algorithm is. As expected, for both CCM and DCM modes DCG generator (8) proved to be the most accurate, (7) had good accuracy and (6) was only fairly accurate. Particularly, in DCM, see Figure 4(c), the accuracy of the proposed algorithm (8) is noticeably better than that of (7), and much better than that of (6). In CCM (see Figure 4(e)) algorithm (6) achieves only fair accuracy, whereas both algorithms (7) and (8) are of comparable performance providing excellent results where only a negligible advantage in favor of (8) can be seen.

3.2. Demonstration of Autonomous Operation of the Proposed DCG. Next, a complete model of the inner loop of an ACM Boost PFC converter based on benchmark design [9] was derived using the methodology described in the previous sections. The SIM equivalent circuit was used to model the boost power stage and DCG duty cycle generators to model the PWM. The DCGs (7) and (8) were compared. The simulation diagram of the circuit is shown in Figure 5(a). The simulation program operates only with the average variables and allows performing Transient as well as AC study of the current loop. The circuit should be prepared for the frequency response analysis by properly placing an AC test source, V_{test}, within the current loop as shown and introducing offset value to the Vline source to preserve the operating point. Introducing initial conditions helps guiding the simulator to settle on a correct operating point. Comparisons of the simulated frequency response plots due to the DCG (7) and DCG (8) of the inner loop are shown in Figure 5(b) and are hardly distinguishable from each other. The steady-state time domain waveforms of the average APFC model with DCG (8) are shown in Figure 5(c).

4. Conclusion

The paper presented a PSPICE software algorithm for modeling the average behavior of PWM modulator in switch-mode systems. The proposed duty cycle algorithm describes the PWM function in both CCM and DCM operating modes and correctly predicts the duty cycle under any operating conditions. Comparison with previously published results supports the theoretical validity of the proposed approach. The proposed average PWM model (8) was implemented in PSPICE software and compared with cycle-by-cycle simulation yielding excellent results. The proposed algorithm (8) was also compared to the earlier counterparts and was indeed found to be more accurate. Particularly, in DCM, the accuracy of the proposed algorithm (8) is noticeably better than that of (7), whereas in CCM (7) and (8) are of comparable performance with only a negligible advantage in favor of (8). In the frequency domain, which uses log scale for the amplitude, the responses were comparable. However, the higher accuracy of the proposed algorithm (8) comes at the price of added programming complexity, which is its main disadvantage. The proposed algorithm (8) can be

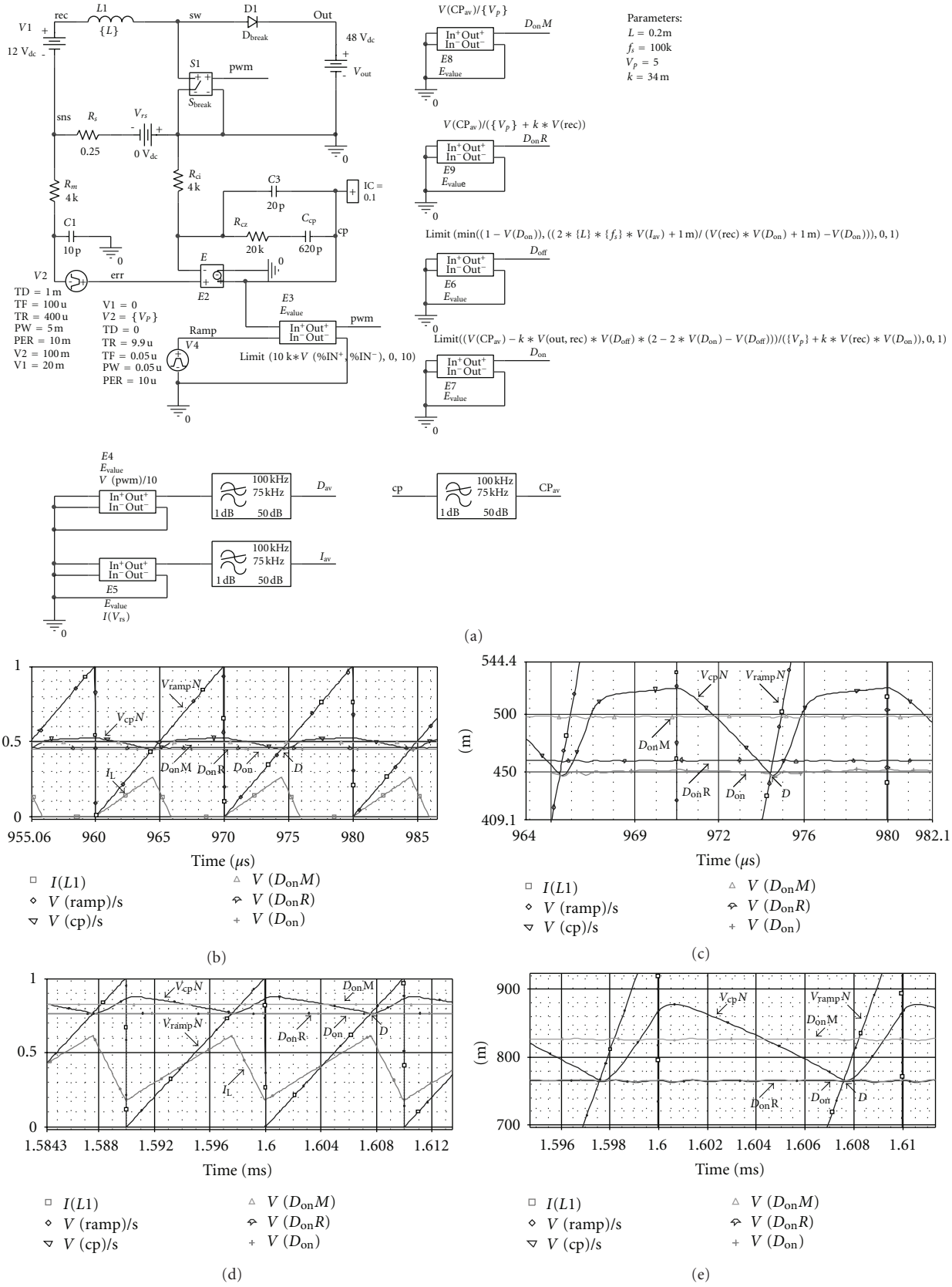

Figure 4: Simulation diagram of the ACM Boost converter (a): simulated waveforms of the instantaneous inductor current IL, instantaneous normalized ramp voltage VrampN, instantaneous normalized current programming voltage VcpN, cycle-by-cycle duty cycle D, average duty cycle DonM according to (6), average duty cycle DonR according to (7), average duty cycle Don according to (8). The DCM mode waveforms (b); exploded view of the DCM mode waveforms (c); the CCM mode waveforms (d); exploded view of the CCM mode waveforms (e).

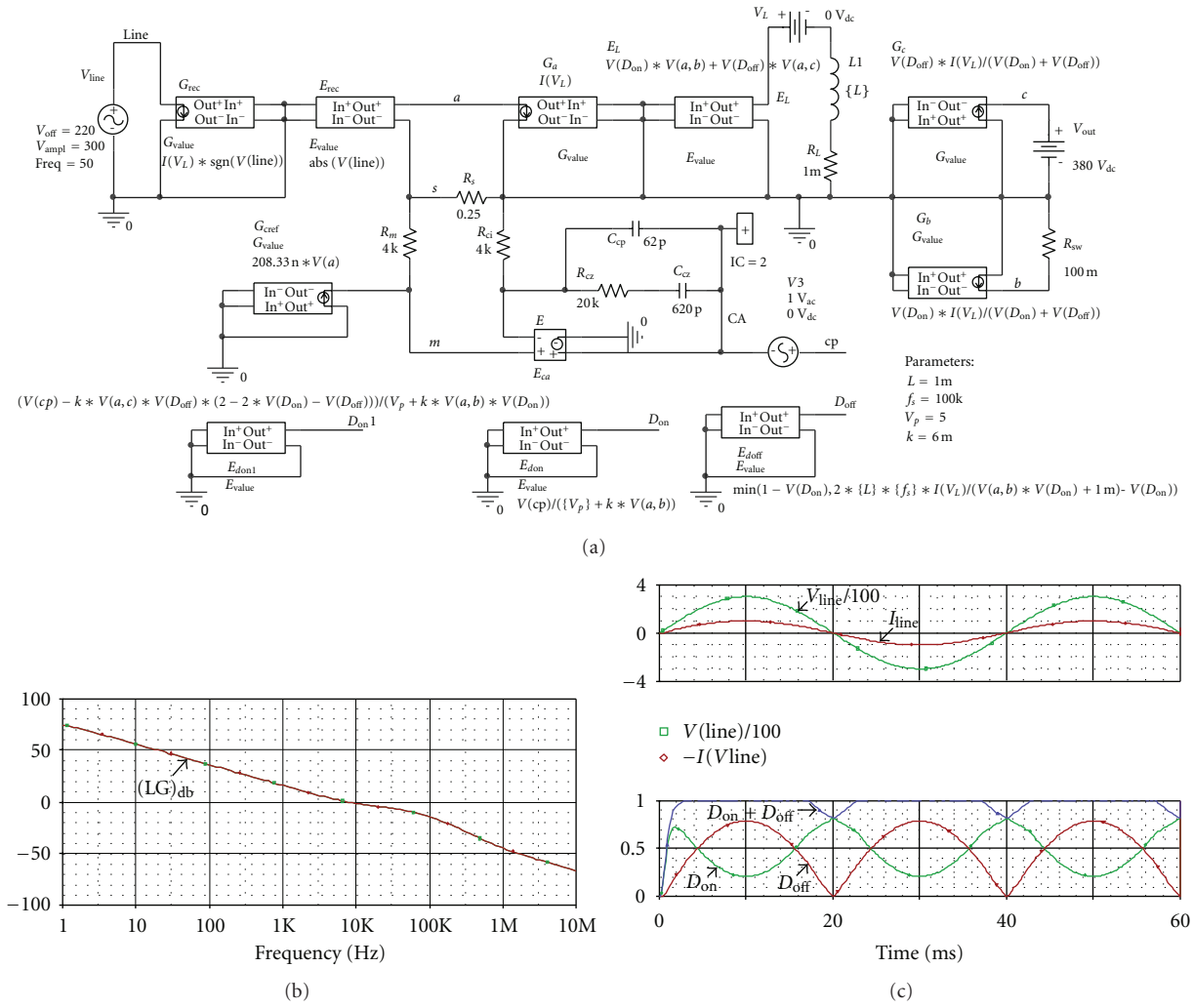

Figure 5: PSPICE simulation diagram of the Average Current mode APFC current loop (a); Simulation of the current loop frequency responses (b); time domain waveforms of the scaled line voltage Vline/100 and line current I(Vline) (top), and the duty cycles Don, Doff; note that the sum $D_{\text{off}} + D_{\text{off}} < 1$ as DCM commences (bottom) (c).

successfully applied in simulation; however, it is inconvenient to be used as a theoretical tool. Also, the recursive nature of (8) aggravates convergence problems. While having somewhat lesser accuracy in DCM, the software duty cycle generation algorithm (7) has the advantage of simplicity and lesser convergence problems. Moreover, the expression (7) is identical to the PWM modulator function proposed by [11], which is currently considered as a widely accepted method for theoretical analysis of current mode converters. Therefore, the results of this study provide an additional verification and support the validity and soundness of [11].

Appendix

A. A Quick Reference to SIM and D_{off} DCG

Energy transfer in hard switched power converters is accomplished by periodic charging and discharging of an inductor. The topology of the switched inductor is shown in Figure 6(a). The switched inductor model (SIM) is an average behavioral model of the switched inductor block. SIM was developed by [6] and is shown in Figure 6(b).

SIM derives the average inductor current applying an average voltage, E_L, across the power stage inductor, L [6]. The average voltage, E_L, is a function of the terminal voltages, V_{ab} and V_{ac}, and the duty cycles D_{on} and D_{off}:

$$E_L = V_{\text{ab}} D_{\text{on}} + V_{\text{ac}} D_{\text{off}}. \tag{A.1}$$

The physical feature of current steering between the terminals b and c is modeled by the dependent current sources of the SIM model [8] (Figure 6(b)) which are defined as follows:

$$\begin{aligned} G_a &= I_L, \\ G_b &= \frac{I_L D_{\text{on}}}{D_{\text{on}} + D_{\text{off}}}, \\ G_c &= \frac{I_L D_{\text{off}}}{D_{\text{on}} + D_{\text{off}}}. \end{aligned} \tag{A.2}$$

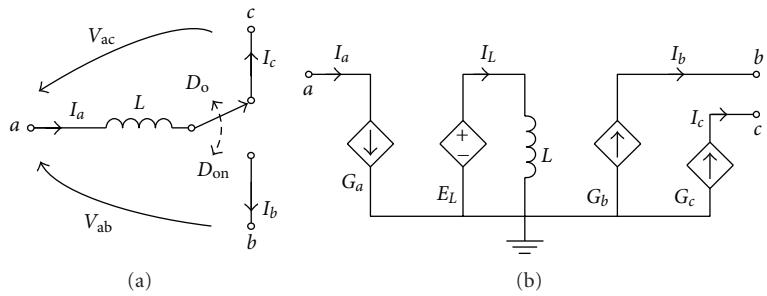

Figure 6: The topology of the switched inductor in PWM converters (a); and the Switched Inductor Model (SIM) equivalent circuit (b) [6].

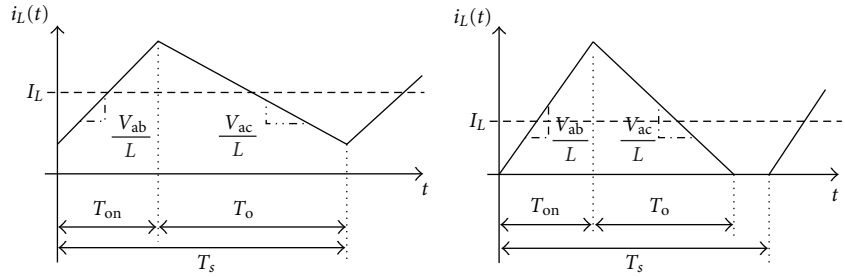

Figure 7: Definition of the inductor discharge duty cycle Doff: CCM mode (a) and the DCM (b).

To implement (A.2) the simulation program is also required to produce the D_{off} duty cycle. In case the power stage operates in CCM (see Figure 7(a)) the Off Duty Cycle depends solely on D_{off}:

$$D_{off} = 1 - D_{on}. \tag{A.3}$$

In the case of DCM, however (see Figure 7(b)), D_{off} depends also on other system parameters and operating conditions:

$$D_{off} = \frac{2Lf_sI_L}{V_{ab}D_{on}} - D_{on} < 1 - D_{on}. \tag{A.4}$$

The DCM D_{off} by (A.4) is always smaller than CCM D_{off} by (A.3). Hence, the software Off-Duty Cycle Generator is programmed to calculate both expressions (A.3) and (A.4) and decide on the proper, D_{off}, using the PSPICE minimum function [7]:

$$D_{off} = \min\left\{(1 - D_{on}), \left(\frac{2Lf_sI_L}{V_{ab}D_{on}} - D_{on}\right)\right\}. \tag{A.5}$$

As a result, PSPICE is able to identify CCM-DCM mode changes and calculate the correct D_{off} under any operating conditions.

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