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Research Article

Single OTRA Based Analog Multiplier and Its Applications

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This paper presents an analog multiplier using single operational transresistance amplifier (OTRA). The proposed circuit is suitable for integration as it does not use any external passive component. It can be used as a four-quadrant multiplier. Theoretical propositions are verified through PSPICE simulations using 0.5 μm CMOS parameters provided by MOSIS (AGILENT). The simulation results are in close agreement with theoretical predictions. The workability of the proposed multiplier is also tested through two applications, namely, a squarer and an amplitude modulator.

1. Introduction

Analog multipliers find extensive application in the field of telecommunication, control, instrumentation, measurement, and signal processing [1]. A number of circuits are reported in literature relating to analog multipliers [1–12]. Circuits presented in [2–7] are based on Gilbert multiplier [12] and are suitable for CMOS integrated technology. The other class of the circuits is implemented using active analog blocks such as operational transconductance amplifier [1], differential difference current conveyors [8], current feedback amplifiers [9], current-controlled current conveyor [10], and current difference buffered amplifier [11].

Recently the OTRA has emerged as an alternate analog building block [13–26] which inherits all the advantages of current mode techniques. The OTRA is a high gain current input voltage output device. The input terminals of OTRA are internally grounded, thereby eliminating response limitations due to parasitic capacitances and resistances [13] at the input. Several high performance CMOS OTRA topologies have been proposed in the literature [13–16]. In the recent past OTRA has been extensively used as an analog building block for realizing a number of analog signal processing [17–21] and generation circuits [22–24]. This paper presents a single OTRA based low voltage analog multiplier which does not use any external passive components and hence is suitable for integration. The proposed circuit can be used as a four quadrant multiplier without any change of topology. The workability of the proposed multiplier is demonstrated through two applications, namely, a squarer and an amplitude modulator.

2. The Proposed Multiplier Circuit

2.1. OTRA. OTRA is a three-terminal device, shown symbolically in Figure 1 and its port relations are characterized by the following matrix:

$$\begin{bmatrix} V_p \\ V_n \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_O \end{bmatrix}, \quad (1)$$

where R_m is transresistance gain of OTRA. For ideal operations R_m approaches infinity and forces the input currents to be equal. Thus OTRA must be used in a negative feedback configuration.

Figure 2 Shows the CMOS realization of OTRA [15] which consists of the cascaded connection of the modified differential current conveyor (MDCC) [8] and common source amplifier. MDCC performs the current differencing operation and forces the two input terminals to be virtually

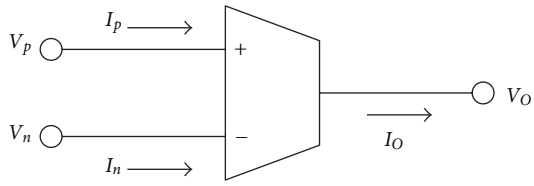


Figure 1: OTRA circuit symbol.

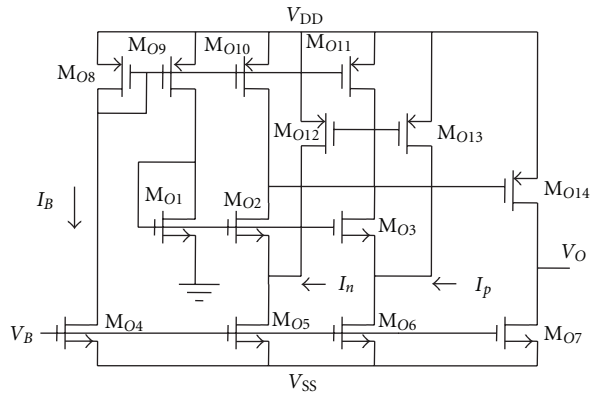


Figure 2: Figure 6 CMOS implementation of OTRA [15].

grounded whereas the common source amplifier provides high gain.

2.2. Basic Multiplier Circuit. Figure 3 Shows OTRA based multiplier structure. The transistors M_1, M_2, M_3, and M_4 are matched transistors and operate in the linear region. In this paper v_1 and v_2 represent small signals, whereas V_{C1}, V_{C2}, and V_{DC} are the bias voltages. OTRA inputs keep the sources of the two transistors M_1 and M_2 virtually grounded. The drain current for the MOS transistor operating in triode region is given by [27]

$$I_D = k\frac{W}{L}\left((V_{GS} - V_T) - \frac{V_{DS}}{2}\right)V_{DS}, \tag{2}$$

where k is transconductance; W and L respectively represent the channel width and length of the of the MOSFET. The other terms have their usual meaning.

Using (2) the currents through p and n terminals of OTRA, that is, i_p and i_n, respectively, can be expressed as

$$\begin{aligned} i_p &= K_n\frac{W}{L}\left(((V_{DC} + v_1) - V_T) - \frac{v_2}{2}\right)v_2 \\ &\quad + K_n\frac{W}{L}\left((V_{C1} - V_T) - \frac{v_o}{2}\right)v_o, \end{aligned} \tag{3}$$

$$\begin{aligned} i_n &= K_n\frac{W}{L}\left((V_{DC} - V_T) - \frac{v_2}{2}\right)v_2 \\ &\quad + K_n\frac{W}{L}\left((V_{C2} - V_T) - \frac{v_o}{2}\right)v_o. \end{aligned} \tag{4}$$

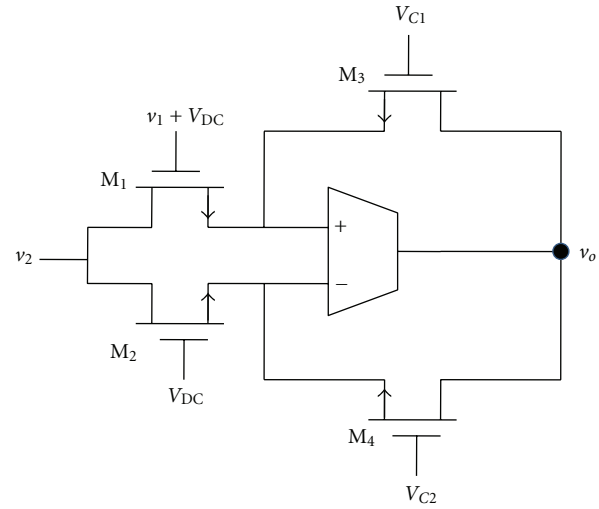


Figure 3: Proposed OTRA based multiplier structure.

As R_m approaches infinity the input currents are forced to be equal resulting in

$$v_o = \frac{v_1 v_2}{(V_{C2} - V_{C1})} = K v_1 v_2, \tag{5}$$

where K is a proportionality constant and is the inverse of difference of gate voltages of M_3 and M_4.

2.3. Implementation Scheme for Superimposition of a Small Signal on DC Bias. As can be seen from Figure 3 the gate voltage of M_1 is $(V_{DC} + v_1)$ which is a small signal superimposed over a dc bias. This voltage addition can be implemented using a scheme proposed in Figure 4 wherein v_x is a small signal voltage and V_C is a bias voltage.

If M_{P1} and M_{P2} are matched transistors and are operating in saturation then their drain currents will be equal resulting in

$$\frac{1}{2}K_p\frac{W}{L}\left((v - V_C) - V_{tp}\right)^2 = \frac{1}{2}K_p\frac{W}{L}\left((v_x - v) - V_{tp}\right)^2, \tag{6}$$

which gives

$$v = \frac{(V_C + v_x)}{2}. \tag{7}$$

The voltage given by (7) can be used as the gate voltage for transistor M_1 of Figure 3. Similarly gate voltage for transistor M_2 can be obtained from (7) by making $v_x = 0$. Substituting these values of gate voltages in (5) the output of the multiplier gets modified to

$$v_o = K' v_1 v_2, \quad \text{where } K' = \frac{K}{2}. \tag{8}$$

2.4. The Proposed MOS Based Multiplier Structure. The complete MOS based multiplier structure is depicted in Figure 5 which incorporates the voltage addition scheme of Figure 4.

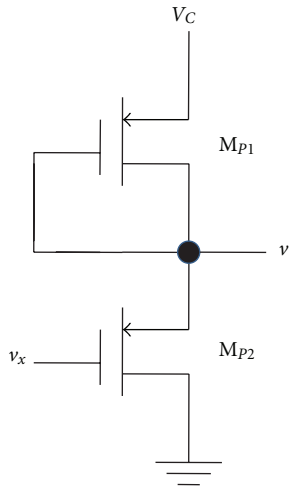


Figure 4: Scheme for implementing an ac superimposed on dc bias.

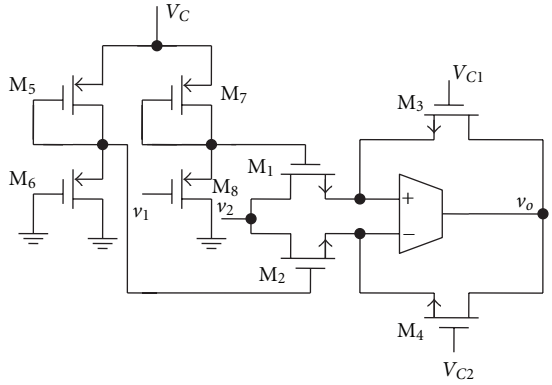


Figure 5: Complete multiplier circuit.

As the transistors M_1, M_2, M_3, and M_4 need to operate in the triode region for proper operation of the multiplier the following conditions should be satisfied:

$$\begin{aligned}\left(\frac{(V_C+v_1)}{2}-V_{tn}\right)&>v_2,\\ \left(\left(\frac{V_C}{2}\right)-V_{tn}\right)&>v_2,\\ (V_{C1}-V_{tn})&>v_o,\\ (V_{C2}-V_{tn})&>v_o.\end{aligned}\tag{9}$$

Now using (7) along with (9) the conditions for input signals v_1 and v_2 can be computed as

$$\begin{aligned}V_{tp}<v_1&<\left(V_C+2V_{tp}\right),\\ v_2&<\frac{(V_C+v_1)}{2}-V_{tn}\,.\end{aligned}\tag{10}$$

These equations suggest that the dynamic input range of the multiplier is controlled by V_C.

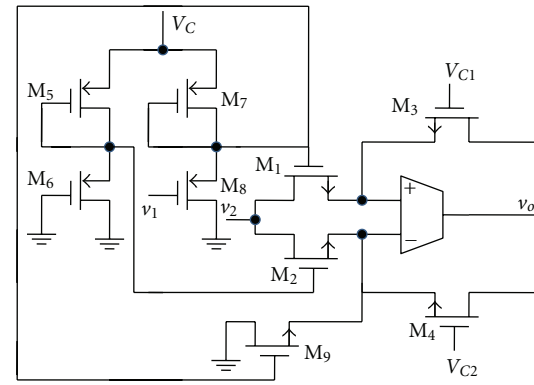


Figure 6: Complete multiplier circuit with C_{gs} compensation of transistor M_1.

3. Nonideal Analysis

In this section the effect of finite transresistance gain of OTRA on multiplier is considered and compensation is employed for high frequency applications. Ideally the transresistance gain R_m is assumed to approach infinity. However, practically R_m is a frequency dependent finite value [13]. Considering a single pole model for the transresistance gain, R_m can be expressed as

$$R_m(s)=\left(\frac{R_0}{1+s/\omega_0}\right).\tag{11}$$

For high frequency applications the transresistance gain $R_m(s)$ reduces to

$$R_m(s)\approx\left(\frac{1}{sC_p}\right),\quad \text{where } C_p=\frac{1}{R_0\omega_0}.\tag{12}$$

For high frequency applications the effect of transistor capacitances needs to be considered. Taking this effect into account the currents i_p given by (3) modifies to

$$\begin{aligned}i_p=K_n\frac{W}{L}\left(((V_{DC}+v_1)-V_T)-\frac{v_2}{2}\right)v_2\\ +K_n\frac{W}{L}\left((V_{C1}-V_T)-\frac{v_o}{2}\right)v_o+v_1sC_{gs1},\end{aligned}\tag{13}$$

where C_{gs1} is the gate to source capacitance of M_1; however, the current i_n remains the same as (4). The effect of C_{gs1} can be compensated by adding a MOSFET M_9, operating in triode region, at the inverting terminal of OTRA as shown in Figure 6. The effective gate to source capacitance of M_9 should be equal to C_{gs1}. This would result in i_n as

$$\begin{aligned}i_n=K_n\frac{W}{L}\left((V_{DC}-V_T)-\frac{v_2}{2}\right)v_2\\ +K_n\frac{W}{L}\left((V_{C2}-V_T)-\frac{v_o}{2}\right)v_o+v_1sC_{gs1}.\end{aligned}\tag{14}$$

The third term in (14) results due to gate to source capacitance of M_9.

Table 1: Aspect ratio of the transistors in OTRA circuit.

Transistor	W (μm)/L (μm)
M_{O1}–M_{O3}	100/2.5
M_{O4}	10/2.5
M_{O5}, M_{O6}	30/2.5
M_{O7}	10/2.5
M_{O8}–M_{O11}	50/2.5
M_{O12}, M_{O13}	100/2.5
M_{O14}	50/0.5

Substituting (12), (13), and (14) in (1), v_o, the output of multiplier can be evaluated as

$$v_o = \frac{v_1 v_2/(V_{C2} - V_{C1})}{1 + sC_p/\{K_n(W/L)(V_{C2} - V_{C1})\}}. \quad (15)$$

And hence the 3 dB bandwidth of the multiplier can be expressed as

$$\frac{K_n(W/L)(V_{C2} - V_{C1})}{C_p}. \quad (16)$$

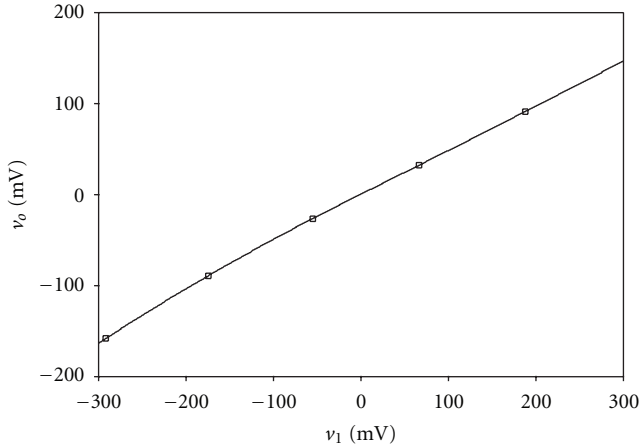
4. Simulation Results

The performance of the proposed multiplier of Figure 5 is verified through SPICE simulation using 0.5 μm CMOS process parameters provided by MOSIS (AGILENT). CMOS implementation of the OTRA [15] shown in Figure 2 is used and supply voltages are taken as ± 1.5 V. Aspect ratios used for different transistors of OTRA are the same as in [15] and are given in Table 1. All the transistors M_1–M_8 were used with equal aspect ratios having $W/L = 1\,\mu/0.5\,\mu$. Control voltage is taken as $V_C = 2$ V, $V_{C1} = 1$ V, and $V_{C2} = 1.25$ V.

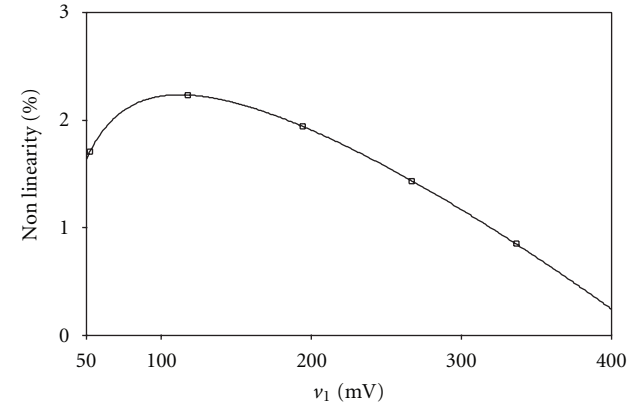
Figure 7 depicts the dc transfer characteristics of the proposed multiplier. The transfer curve v_o versus v_1, with v_2 kept constant at 250 mV, is shown in Figure 7(a). It is observed that v_o varies almost linearly with v_1. The nonlinearity curve representing maximum percent deviation of the ideal transfer characteristic as a function of input voltage v_1 is shown in Figure 7(b). It is observed that the maximum nonlinearity over the entire input range does not exceed 2.05%. In Figure 7(c) v_o is plotted with respect to v_1 for different values of v_2. Voltage v_1 is swept from -300 mV to 300 mV while v_2 is varied from -150 mV to 150 mV in steps of 50 mV. It shows that the proposed circuit is a four-quadrant multiplier.

The frequency response of the proposed multiplier is shown in Figure 8 for which v_1 is kept constant at 200 mV whereas v_2 is taken as an ac source having amplitude 250 mV. The 3 dB bandwidth is found to be 8 MHz.

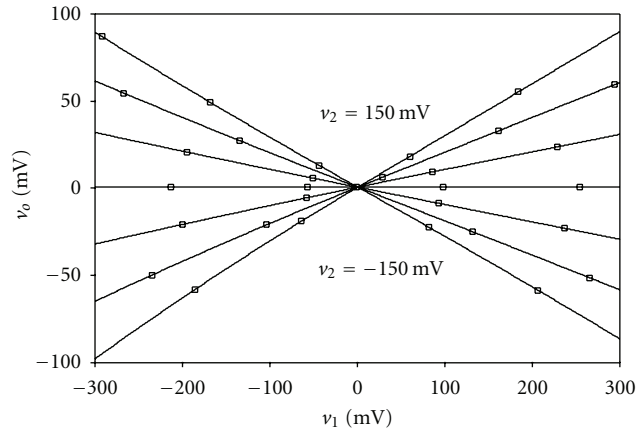
Figure 9 shows the total harmonic distortion (THD) as a function of input signal amplitude when a constant dc voltage (250 mV) is applied to v_2 while a 1 KHz sinusoidal signal is applied to v_1 with varying amplitude. It can be seen that the maximum THD remains under 0.2% for the entire input range. Total power consumption of the proposed multiplier is 0.83 mw when $v_1 = v_2 = 0$ V, $V_C = 2$ V, $V_{C1} = 1$ V, and $V_{C2} = 1.25$ V.



(a) v_o versus v_1 with $v_2 = 250$ mV



(b) Nonlinearity curve with $v_2 = 250$ mV



(c) v_o versus v_1 when v_2 is varied from -150 mV to 150 mV

Figure 7: DC transfer characteristic.

5. Applications

5.1. Squarer. The proposed multiplier can be used as a squarer circuit if $v_1 = v_2 = v_{in}$. The output of the multiplier is given by

$$v_o = K' v_{in}^2. \quad (17)$$

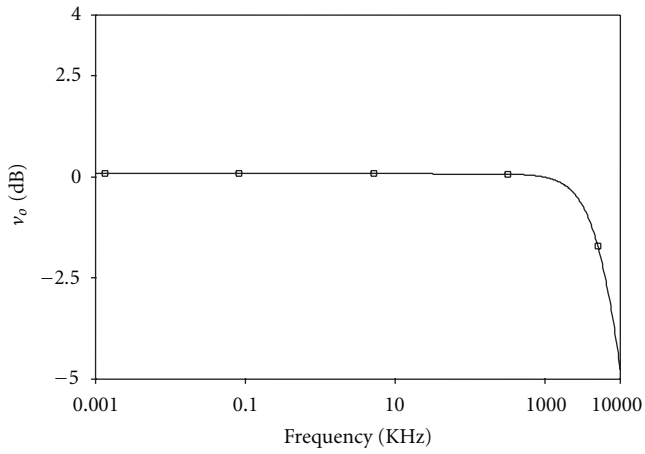


Figure 8: AC characteristic of the proposed multiplier.

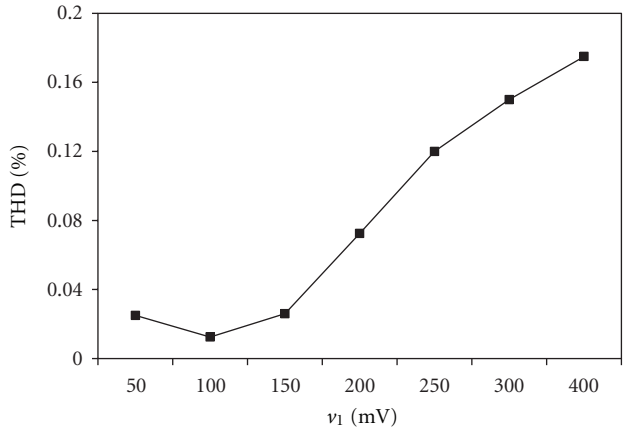


Figure 9: THD versus input signal amplitude.

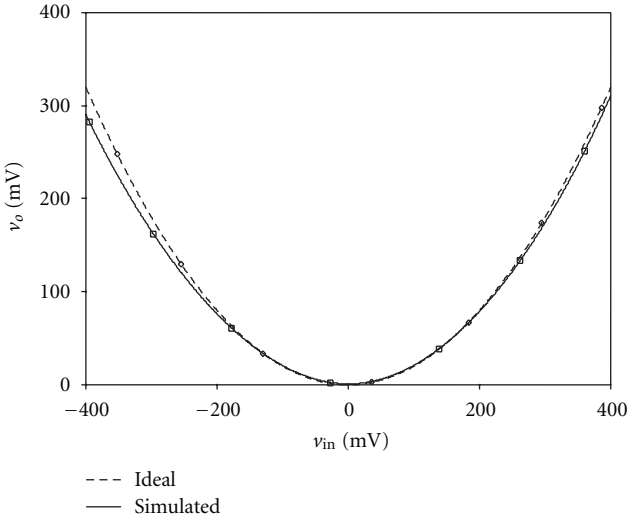
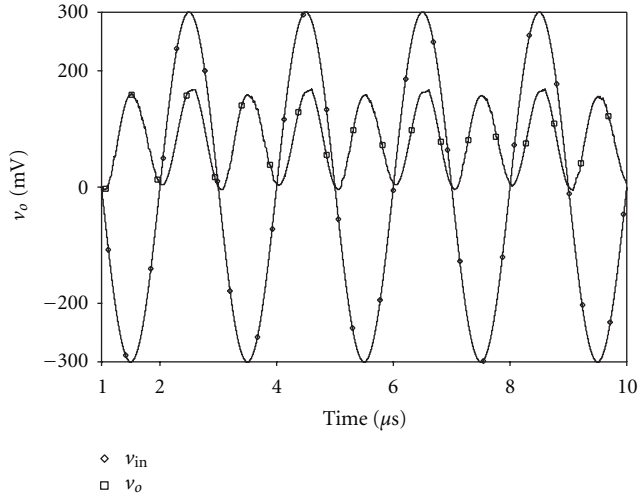
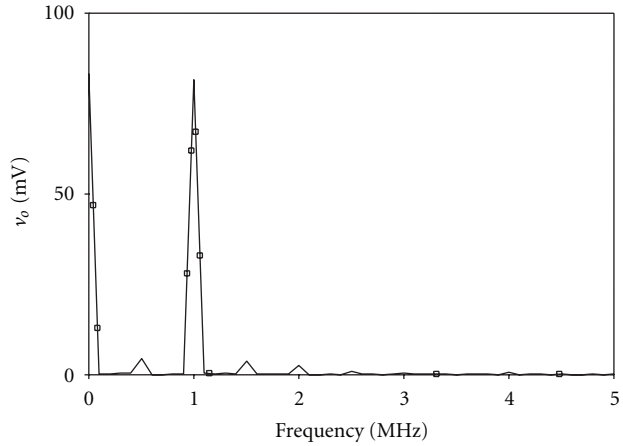


Figure 10: Square transfer characteristics.



(a) Time domain output of the squarer



(b) Spectrum of squared sine wave

Figure 11: Output of the squarer.

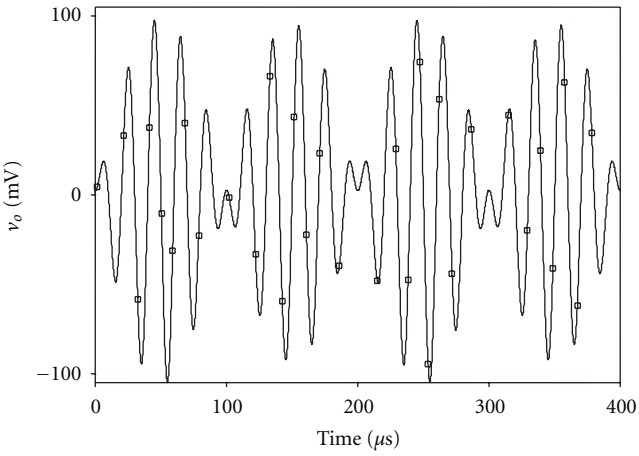
Figure 10 shows the square transfer characteristics wherein v_{in} is varied from −400 mV to 400 mV.

The observed output of the squarer is shown in Figure 11. The input signal is taken as a 300 mV, 500 KHz sinusoid. The squared output is shown in Figure 11(a) and the spectrum of the squared output is shown in Figure 11(b).

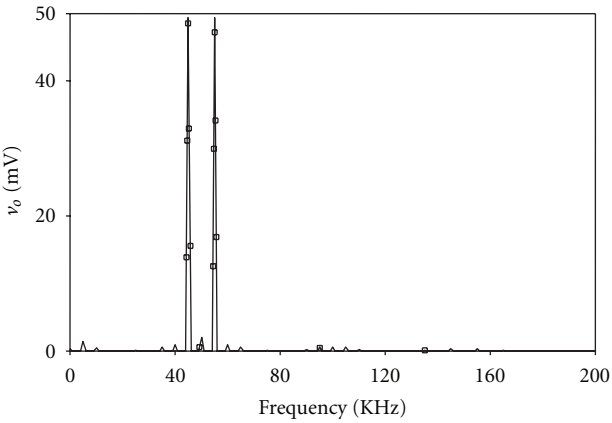
5.2. Amplitude Modulator. The proposed multiplier, being a four-quadrant multiplier, can be used as an amplitude modulator (AM). A 5 KHz signal with 200 mV amplitude is multiplied by 250 mV, 50 KHz signal. Figure 12 shows the output of the proposed multiplier confirming the modulation function. The time domain response of the multiplier is shown in Figures 12(a) and 12(b) displays the frequency spectrum.

6. Conclusion

A single OTRA based analog multiplier is proposed which can be used as a four-quadrant multiplier also. The circuit does not require any passive element thus making it suitable



(a) Time domain response



(b) Frequency spectrum

Figure 12: Multiplication of two sinusoids.

for integration. Its application as a squarer and an amplitude modulator is also discussed. Theoretical propositions are verified through PSPICE simulations using 0.5 μm CMOS parameters provided by MOSIS (AGILENT). Various performance parameters are analyzed through simulations and are found in close agreement to theoretical predictions.

References

[1] K. Kaewdang, C. Fongsamut, and W. Surakampontorn, "A wide-band current-mode OTA-based analog multiplier-divider," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '03)*, vol. 1, pp. I349–I352, May 2003.

[2] S. I. Liu and D. J. Wei, "Analogue squarer and multiplier based on MOS square-law characteristic," *Electronics Letters*, vol. 32, no. 6, pp. 541–542, 1996.

[3] S. I. Liu and C. C. Chang, "Low-voltage CMOS four-quadrant multiplier based on square-difference identity," *IEE Proceedings Circuits, Devices and Systems*, vol. 143, pp. 174–176, 1996.

[4] G. Weixin, C. Hongyi, and E. Seevinck, "Quadratic-translinear CMOS multiplier-divider circuit," *Electronics Letters*, vol. 33, no. 10, pp. 860–861, 1997.

[5] I. Baturone, S. Sanchez-Solano, and J. L. Huertas, "A CMOS current-mode multiplier/divider circuit," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '98)*, pp. 520–523, June 1998.

[6] A. Demosthenous and M. Panovic, "Low-voltage MOS linear transconductor/squarer and four-quadrant multiplier for analog VLSI," *IEEE Transactions on Circuits and Systems I*, vol. 52, no. 9, pp. 1721–1731, 2005.

[7] C. Chen and Z. Li, "A low-power CMOS analog multiplier," *IEEE Transactions on Circuits and Systems II*, vol. 53, no. 2, pp. 100–104, 2006.

[8] H. O. Elwan and A. M. Soliman, "CMOS differential current conveyors and applications for analog VLSI," *Analog Integrated Circuits and Signal Processing*, vol. 11, no. 1, pp. 35–45, 1996.

[9] S. I. Liu and J. J. Chen, "Realisation of analogue divider using current feedback amplifiers," *IEE Proceedings Circuits, Devices and Systems*, vol. 142, no. 1, pp. 45–48, 1995.

[10] M. T. Abuelma'atti and M. A. Al-Qahtani, "A current-mode current-controlled current-conveyor-based analogue multiplier/divider," *International Journal of Electronics*, vol. 85, no. 1, pp. 71–77, 1998.

[11] A. U. Keskin, "A four quadrant analog multiplier employing single CDBA," *Analog Integrated Circuits and Signal Processing*, vol. 40, no. 1, pp. 99–101, 2004.

[12] B. Gibert, "A precision four-quadrant multiplier with sub-nanosecond response," *The IEEE Journal of Solid-State Circuits*, vol. 3, no. 6, pp. 353–365, 1968.

[13] J. J. Chen, H. W. Tsao, and C. C. Chen, "Operational transresistance amplifier using CMOS technology," *Electronics Letters*, vol. 28, no. 22, pp. 2087–2088, 1992.

[14] K. N. Salama and A. M. Soliman, "CMOS operational transresistance amplifier for analog signal processing," *Microelectronics Journal*, vol. 30, no. 3, pp. 235–245, 1999.

[15] H. Mostafa and A. M. Soliman, "A modified CMOS realization of the operational transresistance amplifier (OTRA)," *Frequenz*, vol. 60, no. 3-4, pp. 70–76, 2006.

[16] A. K. Kafrawy and A. M. Soliman, "A modified CMOS differential operational transresistance amplifier (OTRA)," *International Journal of Electronics and Communications*, vol. 63, no. 12, pp. 1067–1071, 2009.

[17] K. N. S. Ahmed and A. M. Soliman, "Active RC applications of the operational transresistance amplifier," *Frequenz*, vol. 54, no. 7-8, pp. 171–176, 2000.

[18] S. Kılınc and U. Çam, "Cascadable allpass and notch filters employing single operational transresistance amplifier," *Computers and Electrical Engineering*, vol. 31, no. 6, pp. 391–401, 2005.

[19] S. Kılınc, A. U. Keskin, and U. Çam, "Cascadable voltage-mode multifunction biquad employing single OTRA," *Frequenz*, vol. 61, no. 3-4, pp. 84–86, 2007.

[20] S. Kilinc, K. N. Salama, and U. Cam, "Realization of fully controllable negative inductance with single operational transresistance amplifier," *Circuits, Systems, and Signal Processing*, vol. 25, no. 1, pp. 47–57, 2006.

[21] U. Çam, F. Kaçar, O. Cicekoglu, H. Kuntman, and A. Kuntman, "Novel two OTRA-based grounded immitance simulator topologies," *Analog Integrated Circuits and Signal Processing*, vol. 39, no. 2, pp. 169–175, 2004.

[22] K. N. Salama and A. M. Soliman, "Novel oscillators using the operational transresistance amplifier," *Microelectronics Journal*, vol. 31, no. 1, pp. 39–47, 2000.

[23] U. Çam, "A novel single-resistance-controlled sinusoidal oscillator employing single operational transresistance amplifier,"

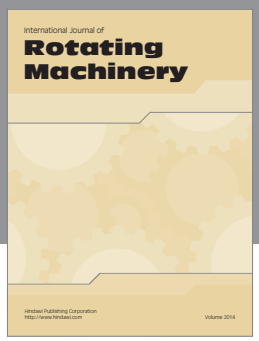
Analog Integrated Circuits and Signal Processing, vol. 32, no. 2, pp. 183–186, 2002.

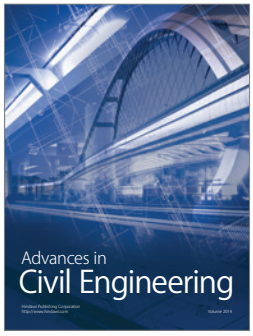
[24] R. Pandey, N. Pandey, M. Bothra, and S. K. Paul, "Operational transresistance amplifier-based multiphase sinusoidal oscillators," *Journal of Electrical and Computer Engineering*, vol. 2011, Article ID 586853, 8 pages, 2011.

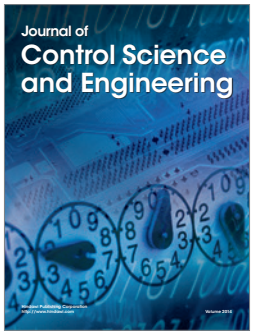
[25] C. Sanchez-Lopez, E. Tlelo-Cuautle, and E. Martinez-Romero, "Symbolic analysis of OTRAs-based circuits," *Journal of Applied Research and Technology*, vol. 9, no. 1, pp. 69–80, 2011.

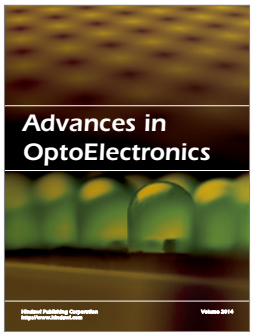
[26] C. Sánchez-López, F. V. Fernández, and E. Tlelo-Cuautle, "Generalized admittance matrix models of OTRAs and COAs," *Microelectronics Journal*, vol. 41, no. 8, pp. 502–505, 2010.

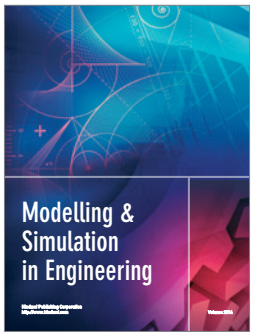
[27] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, Oxford University Press, New York, NY, USA, 2004.

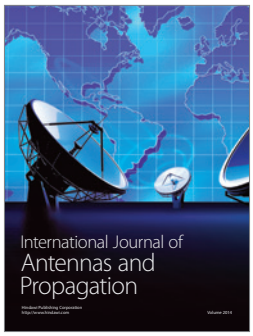


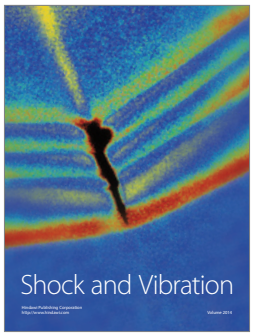


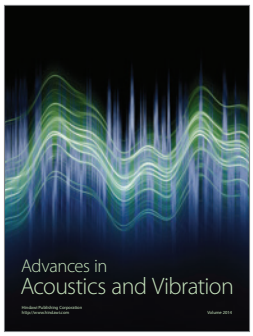












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