International Scholarly Research Network
ISRN Electronics
Volume 2012, Article ID 891480, 7 pages
doi:10.5402/2012/891480

Research Article

Fabrication of Self-Aligned Graphene FETs with Low Fringing Capacitance and Series Resistance

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Received 23 July 2012; Accepted 9 August 2012

Academic Editors: L. Belostotski, J. Solsona, and E. Tlelo-Cuautle

Graphene FETs with top-gate and buried-gate structure has been studied. The buried-gate structure shows less fringing capacitance and more reliable contacts. High-performance graphene transistors with self-aligned buried gates have been fabricated. The graphene transistor shows field-effect mobility of over 6,000 $cm^2/V \cdot s$ according to the transconductance measurement. The contact resistance and intrinsic mobility have been extracted from both curve fitting and transfer length measurement, and the two results agree well. This result paves the way of high-quality graphene transistor technology for the RF application.

1. Introduction

As a two-dimensional material composed of a layer of carbon atoms packed in a honeycomb crystal lattice, graphene has attracted much attention in recent years [1–4]. Graphene shows great potential as a candidate for high-frequency devices application due to its high intrinsic carrier mobility (>10,000 $cm^2/V \cdot s$) [5], large saturation velocity (5.5×10^7 cm/s) [6], and high on-state current density (>3 A/mm) [7, 8]. Graphene-based field-effect transistors (FETs) with a cut-off frequency of 300 GHz [8, 9] have been achieved. High-mobility grapheme FET (6,000 $cm^2/V \cdot s$ and 23,600 $cm^2/V \cdot s$ before and after the extraction of the contact resistance) and different synthesis methods of graphene (epitaxial graphene on SiC, CVD grapheme, and mechanical exfoliated graphene) have been reported [7, 10, 11]. Scalable synthesis of graphene on patterned Ni has been reported [12].

Parasitic capacitance, series resistance, and mobility are the major factors to influence the high-frequency performance of graphene FETs. Self-aligned technique will minimize the series resistance and overlap capacitance, as well as simplify the lithography process. Top-gate graphene FETs with self-aligned structure have been reported by many groups [8, 13, 14]. In these structures, the gate dielectric profile will separate the thin source/drain metal during the source/drain evaporation. However, since the gate and source/drain are on the same side of graphene, this will address several issues for the devices. First, the fringing capacitance in these structures could become an important portion for short-channel devices. Secondly, these structures will restrict the thickness of source/drain otherwise, the source/drain will become shorted. The thin source/drain contact will increase the series resistance and also raise a reliability issue for the RF application of graphene FET since the thin source/drain contact is more vulnerable under large current density.

Graphene FET with buried-gate structure has been published [15–17]. Compared with the top-gate structure, the buried-gate structure enables gate stack and source/drain on different sides, which can reduce the negative effect from the top-gate structures. First, the buried-gate structure can reduce the fringing capacitance between gate and source/drain. Second, thicker source/drain metal could be used

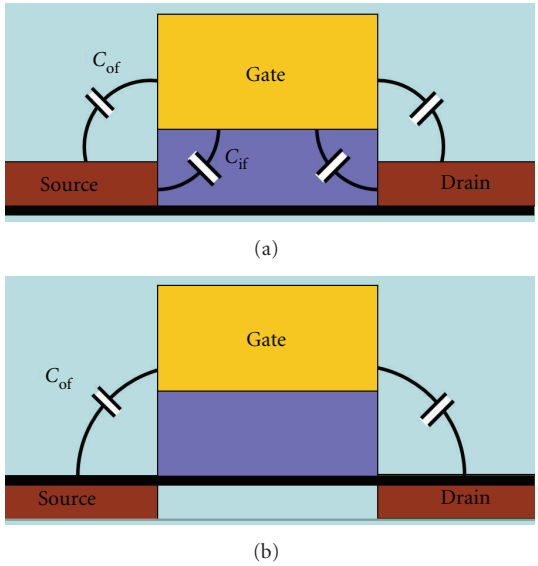

Figure 1: Fringing capacitance in for top-gated (a) and buried-gated (b) structure.

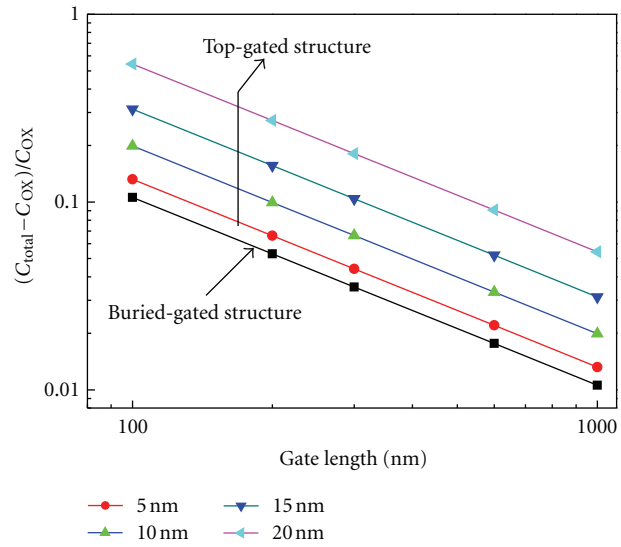

Figure 2: The fringing capacitance at different gate length and source drain thickness for buried- and top-gated devices.

to improve the reliability and reduce the series resistance. Buried-gate graphene FET with "T-" gate structure has been fabricated [15], which will reduce the gate resistance and therefore improve the unit power gain frequency. In light of the benefits of buried-gated structure, buried-gated graphene FETs with self-aligned structure is studied in this paper.

2. Comparison between Buried- and Top-Gate Structure

The unity-current-gain frequency f_T and unity-power-gain frequency f_{max} are two important figures of merits for RF transistors. The parasitic resistances and capacitance will degrade f_T and f_{max} in FET. In graphene FET, the parasitic capacitance composed mainly of direct overlap capacitance and fringing capacitance (between gate and source/drain). Self-aligned process can minimize the direct overlap capacitance and parasitic resistance. In self-aligned structures, the fringing capacitance between gate and source/drain becomes the major parasitic capacitance in the devices. This fringing capacitance composed of outer fringing capacitance C_{of} and inner fringing capacitance C_{if}, as shown in Figure 1. For top-gated devices (Figure 1(a)), both C_{of} and C_{if} exist. For buried-gated devices (Figure 1(b)), the inner fringing capacitance become negligible since the carriers in graphene will effectively shield any electrostatic coupling between the gate and the inner edges of the source or drain junction [18]. Therefore, the influence of the source/drain metal thickness on the fringing capacitance can be ignored for devices' structure of Figure 1(b).

The fringing capacitance for top-gate and buried-gate devices has been simulated with finite element method. In this simulation, the parameters used here are from [13], where the gate metal thickness is 60 nm, gate dielectric is 25 nm Al_2O_3, and the source/drain metal thickness is 10 nm. C_{total} is the total gate capacitance and C_{OX} is the gate oxide capacitance calculated from parallel plate capacitance relation.

Figure 2 plotted the fringing capacitance at different gate length for buried- and top-gated devices. It can be seen that the fringing capacitance becomes an unnegligible capacitance source especially for short channel devices. For 100 nm channel length and 10 nm thick source/drain contact metal, the fringing capacitance is about 20% and 10.6% of the gate capacitance for top-gated and buried-gate structure, correspondingly. In this case, the buried-gate structure reduced the fringing capacitance by 47% compared with the top-gate structure. The influence of the source/drain thickness on the fringing capacitance is also plotted in Figure 2. For buried-gate devices, the fringing capacitance equals that of top-gate devices at zero source/drain thickness and will not increase with increasing of the source/drain thickness. For top-gate devices with 100 nm channel length, the fringing capacitance ratio increases from 13.2% to 54% with the thickness of source drain increase from 5 nm to 20 nm.

In order to avoid current shortage through sidewall region, thin source/drain is used for the self-aligned top-gate device. Current published results for these devices all have the thickness of the source/drain of around 10 nm [13, 14]. We have studied the dependence of the electrode breakdown with the metal thickness, which is shown in Figure 3. Figure 3(a) shows the breakdown current for 10 nm (Ti 0.5 nm/Pd 9.5 nm) and 30 nm (Ti 0.5 nm/Pd 20 nm/Au 9.5 nm) metal. The break-down current for 10 nm metal is about 3.17 mA/μm, and the breakdown current for 30 nm metal is about 8.2 mA/μm. Since it has been reported that the on-state current of graphene FET can reach 1.5 to 3 mA/μm [7, 8], the break-down current for 10 nm metal is close to the on-state current of graphene FET. This will raise the reliability issue of the graphene FET which limits the lifetime

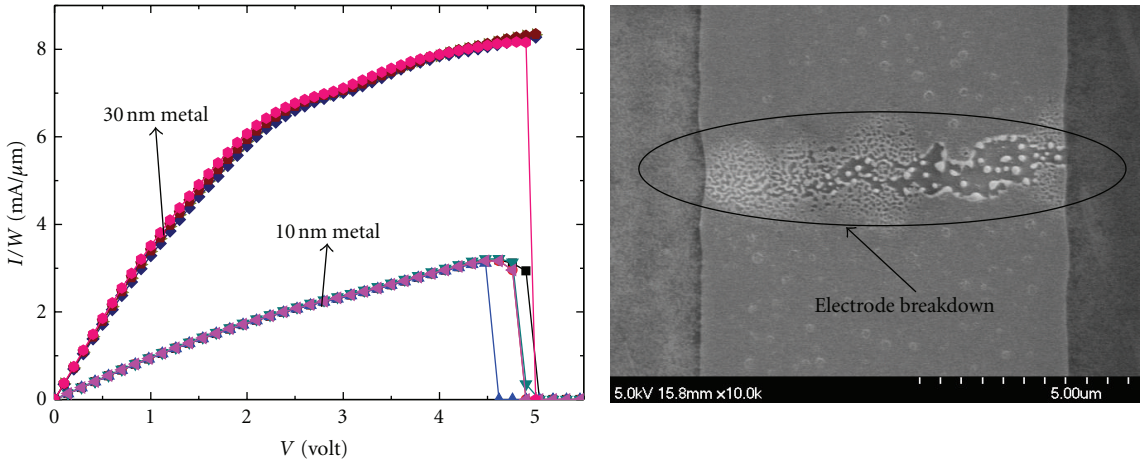

Figure 3: Electrode break-down current for 10 nm and 30 nm metal.

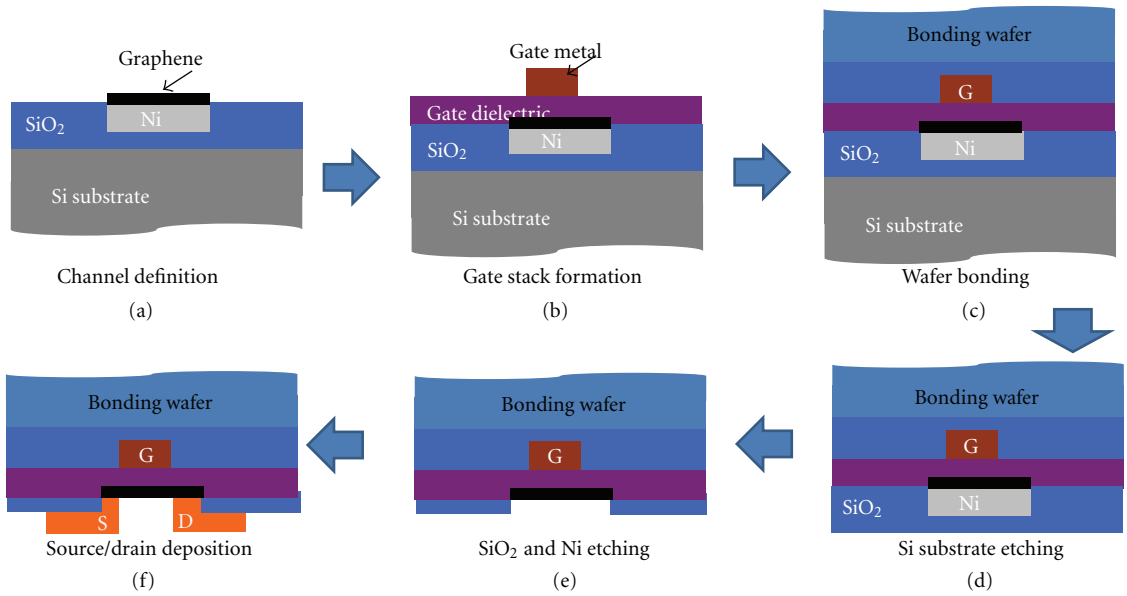

Figure 4: Process flow of self-aligned graphene FET.

of these devices. Figure 3(b) is an SEM picture which shows the electrode breakdown of 10 nm metal (Ti 0.5 nm/Pd 9.5 nm). There is a clear region that the electrode burned and became noncontinuous, which make the electrode to be opened. Also bubbles appear on the electrode outside the break-down region which indicates the electrode outside of the breakdown region is also damaged.

We have demonstrated a self-aligned process to fabricate graphene FET in order to reduce the fringing capacitance and source drain resistance as well as improve the reliability of the contact.

3. Materials and Device Fabrication

The process of fabricating self-aligned buried-gate graphene FET is discussed below. The channel graphene material was synthesized from patterned Ni substrate by chemical vapor deposition (CVD) method with methane catalyst [12]. Gra-phene film was first patterned by oxygen plasma etching to define the channel width (Figure 4(a)). Then, 15 nm SiO_2 (with e-beam evaporation) and 10 nm Al_2O_3 (with atomic layer deposition) were deposited on top of graphene to form gate dielectric. The equivalent oxide thickness (EOT) of the gate dielectric was found to be 20 nm, according to capacitance-voltage measurement. The metal gate was processed with e-beam evaporation of Ti/Au/Ti (5/50/5 nm) and etching (Figure 4(b)). After this step, graphene and the gate stack were transferred with wafer bonding and etch-back method [12] (Figures 4(c), 4(d), and 4(e)). A back-side (glass wafer side) exposure was performed with the buried-gate electrode as the photomask to make the source and drain region self-aligned with gate electrode. The source/drain

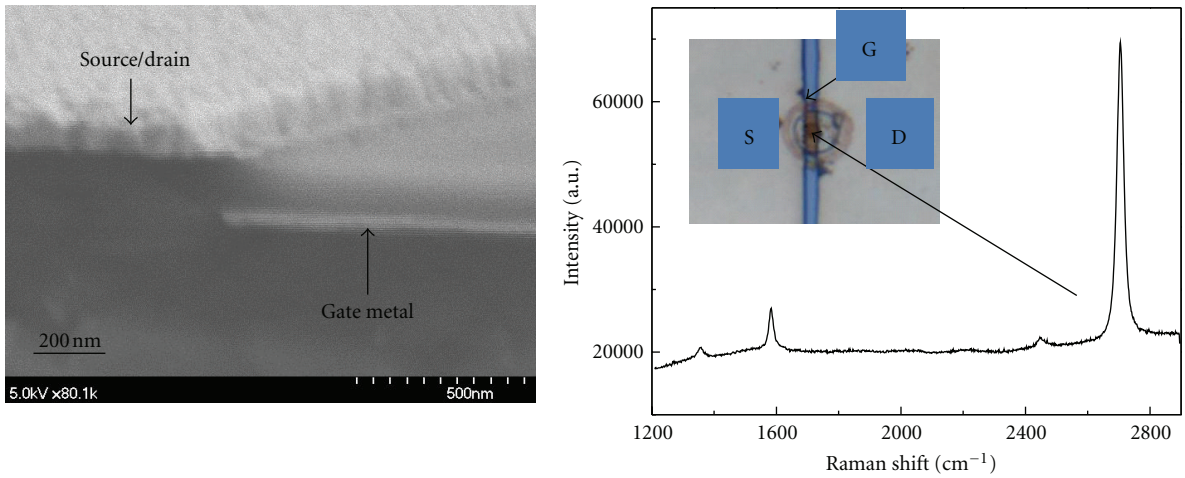

Figure 5: The cross-section of self-aligned structure and the Raman spectra on graphene channel.

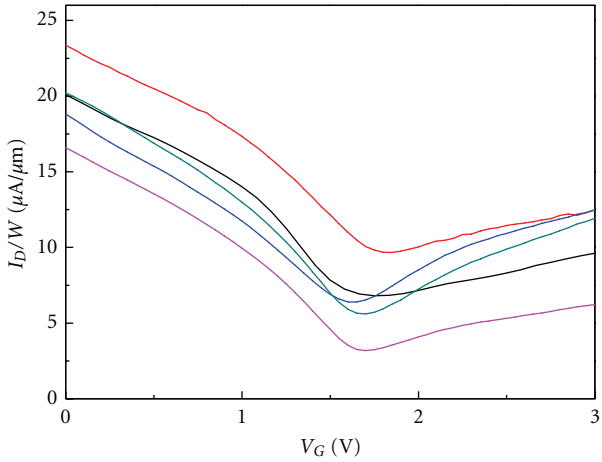

Figure 6: Measured transfer curves of 1.5 μm gate-length graphene FETs at $V_D = 0.01$ V.

metal pads (0.5 nm Ti/60 nm Pd/60 nm Au) were then formed by e-beam evaporation and lift-off process (Figure 4(f)). Here we chose Ti/Pd/Au as the contact metal because of its low contact resistivity with graphene [19, 20]. Device fabrication is completed through open-the-gate contact to expose buried-gate metal pads.

4. Results and Discussion

The cross-section scanning electron microscope (SEM) picture of a graphene FET showing self-aligned source/drain with the gate metal is shown in Figure 5(a). The Raman spectra on the channel region of graphene FETs is shown in Figure 5(b), with an inset of optical microscope (OM) image. The intensity of the D-peak (1354 cm^{-1}) is negligible compared to that of G-peak (1581 cm^{-1}), indicating that disorder in these samples is negligible. The $2D$ peak at ~2705 cm^{-1} shows single Lorentzian distribution with full width at half maximum (FWHM) of 30 cm^{-1}, demonstrating the absence of interlayer coupling. The peak intensity ratio of I_{2D}/I_G is about 7. This characteristic indicates that single-layer graphene was transferred onto gate dielectric with little material damage.

Electrical measurement was performed at room temperature. Figure 6 shows five transfer curves of graphene FETs with gate length equals gate width equals 1.5 μm, which were measured at $V_D = 0.01$ V. The gate leakage currents were on the order of <40 pA/μm, which is negligible in the device characterization presented here. Generally, the devices shows p-channel operation at $V_G = 0$ V, and the ambipolar behavior was observed with the Dirac point located between 1.6 to 1.8 V of gate voltage. The hole branch current is typically larger than electron branch current, which translates into field effect mobility of 5000 to 6000 cm^2/V · s derived from transconductance method ($\mu_{DEV} = g_m L/V_D WC$).

Figure 7(a) shows measured I_D-V_G characteristics of a graphene FET at three top-gate voltages: −1 V, 0.15 V, and 1.3 V. The gate length (L_G) and the channel width (W) are both 1.5 μm. The gate bias is below 1.3 V, displaying pFET hole-like conduction. Under different gate bias, the film conductance varies from 1150 to 3900 μS per square calculated at 0.1 V drain voltage (without taking contact resistance into account). The output characteristics indicate that this device can deliver a large on-current of 1.5 mA/μm at a drain voltage of 1 V.

The dotted lines in Figure 7(b) shows transfer characteristics of the graphene FET. The gate leakage current was in the range of approximately 30 pA per micrometer or less. The Dirac point was reached at $V_G = 1.7$ V. Under 0.01 V drain voltage, the on-state current at $V_G = 0$ V was 20.2 μA/μm. The off-state current was 5.6 μA/μm at $V_G = 1.7$ V, yielding an I_{on}/I_{off} ratio of 3.6. The maximum transconductance g_m is 21 μS/μm for holes and 10 μS/μm for electrons; this translates into field effect mobility of 6,100 cm^2/V · s for holes and 3,000 cm^2/V · s for electrons ($\mu_{DEV} = g_m L/V_D WC$).

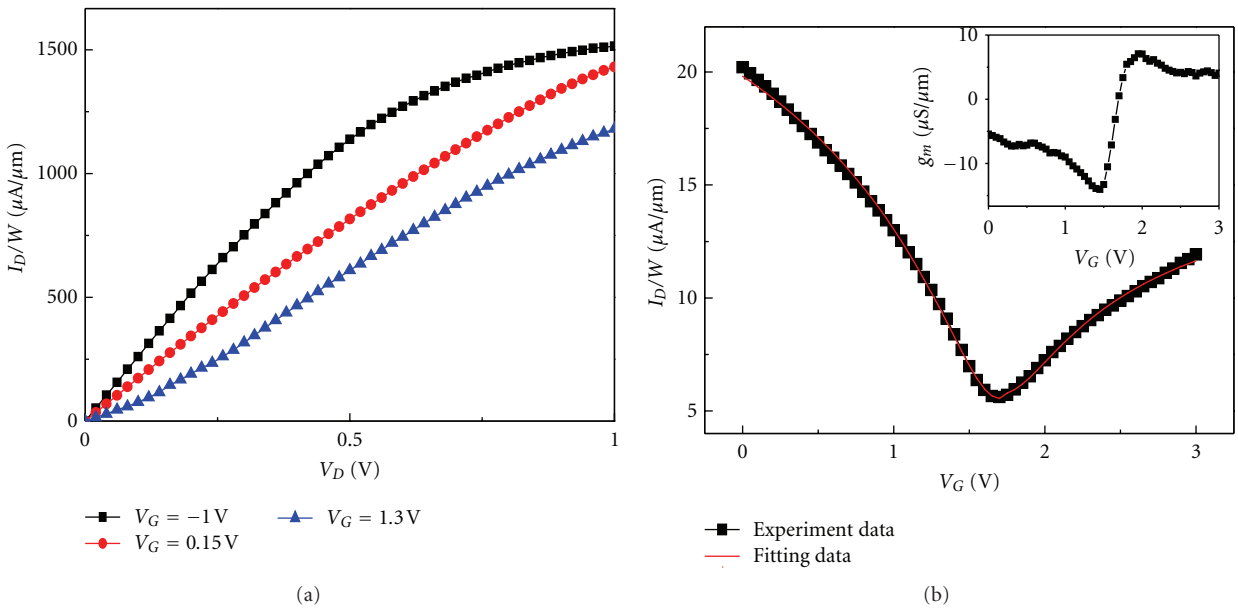

FIGURE 7: Output I_D-V_D (a) and transfer I_D-V_G characteristics (b) of graphene FET.

The electron-hole asymmetry may partially result from the series resistance of the source drain contact [21]. Pd may dope graphene to be p-type which will favor hole conduction and restrict the current injection of electron branch, which results in a low electron mobility extracted from g_m method.

There are many factors which will cause underestimate of the mobility extracted from the transconductance, such as parasitic resistance in source/drain region and the existence of traps in the channel region [22]. In order to get a more accurate mobility value, we subtracted the contact resistance by fitting the measured data with the following relation [13, 23]:

$$R_{\text{Total}} = 2R_C + \frac{L}{We\mu\sqrt{n_0^2 + n^2}}, \quad (1)$$

where $R_{\text{Total}} = V_D/I_D$ is the total resistance of the device, e is the electron charge, L is channel length, W is channel width, n is the carrier concentration induced by top-gated bias, n_0 is the residual carrier concentration of graphene, μ is the intrinsic field-effect mobility of top-gated graphene channel, and R_C is the metal/graphene contact resistance. In order to take the electron-hole asymmetry into consideration, we assigned different contact resistance for electron and hole branch on the transfer characteristics.

The fitted results (Figure 7(b)) give a mobility of μ_h = 25,735 cm^2/V · s for holes and μ_e = 26,538 cm^2/V · s for electrons. The contact resistance ($R_C \cdot W$) was found to be 306 Ω · μm for electron and 153 Ω · μm for hole. According to the fitting results, the mobility for electrons and holes is similar while the contact resistance for holes is about twice of that for electrons. This indicates that the asymmetry properties for electron-hole mainly originated from the contact resistance difference between electron and hole, rather than that of mobility.

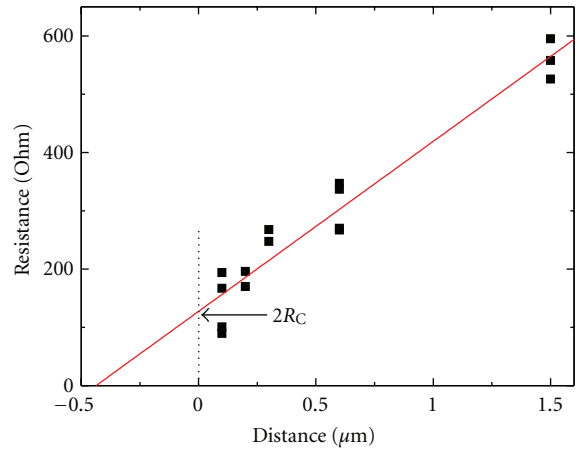

FIGURE 8: Plot of the total resistance of transistors under different channel length.

To further proof the validity of the curve fitting, we performed transfer length measurement (TLM) on graphene FET with different contact space (100 nm, 200 nm, 300 nm, 600 nm, and 1500 nm). A plot of the total resistance versus the contact space is shown in Figure 8. Here the graphene width is 1.5 μm. A linear fitting was performed to extrapolate the contact resistance, which give the total contact resistance of $2R_C$ = 127 Ω, with the slope giving the sheet resistance of graphene of R_{SH} = 436 Ω. Since the graphene resistance underneath the metal contact could be different with the sheet resistance of graphene between the contacts, the TLM method cannot extrapolate the transfer length and specific contact resistivity. The normalized contact resistance $R_C W$ is 95 Ωμm, which is 38% smaller than the value extracted

from the curve fitting ($153\,\Omega \cdot \mu$m). The possible reasons which result in this difference could come from the following factors. First, the TLM method gives a statistical result on many data points, which could be different from a single transistor shown in Figure 7. Second, The TLM measurement was performed at zero gate voltage and the curve fitting in Figure 7 was performed with gate voltage from 0 to 1.7 V. At 0 gate voltage there are more holes in the channel than the other positive gate voltages, which will give a smaller contact resistance. Taking these factors into consideration, we claim that the curve fitting method gives a reasonable extraction of the contact resistance, as well as the mobility.

5. Conclusion

We have fabricated high-performance graphene FETs with self-aligned buried-gates. The buried-gate structure offers following benefits compared with the top-gate structures: the buried-gate structures have lower fringing capacitance, which is due to larger vertical spaces between the source/drain contact and the gate metal as well as the suppressed inner fringing capacitance by the channel carrier. On the other hand, the source/drain contact metal is more robust under large current operation since thicker source/drain could be used. The maximum field-effect mobility determined by transconductance method was found to be $6{,}100\,\text{cm}^2/\text{V} \cdot \text{s}$ and over $25{,}000\,\text{cm}^2/\text{V} \cdot \text{s}$ at room temperature before and after subtraction of contact resistance. The asymmetry properties in the I_D-V_G curve for electrons and holes branches were found to be primarily due to the contact resistance difference. The contact resistance of electrode/graphene was also measured from TLM method, which gives a reasonable agreement with the curve fitting result. This result provides a possible way to scalable fabricate high-performance graphene transistors for RF applications from CVD graphene.

Acknowledgments

This work was supported in part by the Defense Advanced Research Projects Agency under the Space and Naval Warfare Systems Center San Diego under Contract N66001-08-C-2047 (CERA). The device fabrication was performed at the Nanoelectronics Research Facility, University of California, Los Angeles.

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