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Research Article

Novel Low Complexity Pulse-Triggered Flip-Flop for Wireless Baseband Applications

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A low complexity dual-mode pulse-triggered FF design for wireless baseband processing is presented in this paper. It supports both single-edge- and double-edge-triggered operations subject to a mode select control. Due to the novelty in pulse generator design, the layout area overhead is only 8% when compared with other single-mode counterpart design. Postlayout simulations in TSMC 1P6M 0.18 μm CMOS process model also indicate that the proposed design is as efficient as its single-mode counterpart in various performance metrics.

1. Introduction

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules such as register file and shift register. FFs thus contribute a significant portion of gate count to the overall system design. To reduce the circuit complexity, pulse-triggered FFs have been considered as a popular alternative to the conventional master-slave-based FF these days. A pulse-triggered FF consists of a pulse generator (also called transition detector) for strobe signals and a latch for data storage. Since the pulses are generated on the transition edges of the clock signal and very narrow in pulse width, the latch acts like an edge-triggered FF. The circuit complexity of a pulse-triggered FF is thus greatly simplified since only one latch, as opposed to two latches in master-slave configuration, is needed. It can thus provide higher toggle rate than the conventional FF can and is found useful in high speed applications. Another advantage of pulse-triggered FFs is that they allow time borrowing across cycle boundaries and feature zero or even negative setup time [1–3].

Pulse-triggered FFs (P-FFs) can be classified into two types, that is, implicit and explicit, depending on the implementation of pulse generator [4]. In implicit type P-FF, the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In explicit type P-FF, the designs of pulse generator and the latch are separate. Although implicit pulse generation is often considered as more power efficient, the lengthened signal discharge path in latch design leads to inferior timing characteristics. In design practices, one pulse generation circuitry can be shared among FFs within the same register in explicit pulse generation. This gives the explicit type designs advantages in both circuit complexity and power consumption. In this paper, we will therefore focus on the explicit type designs only. Various explicit type P-FFs supporting either single- or double-edge-triggered operations have been proposed [1–6]. None of them can provide both triggering modes in one design. An FF with dual triggering modes is useful in many applications. For example, in many communication baseband circuits, data oversampling is required in the initial synchronization acquiring phase, while the clock rate is reduced to a normal frequency later on for power saving. A dual-mode FF can perfectly serve the purpose without employing two FFs working on different clock frequencies. FFs used in FPGAs or structured ASIC are another example where the selection of triggering mode is required [7, 8].

Herein, in this paper, we will present a novel dual-mode pulse-triggered FF design, with emphasis on low circuit complexity. The circuit overhead of dual-mode operations is

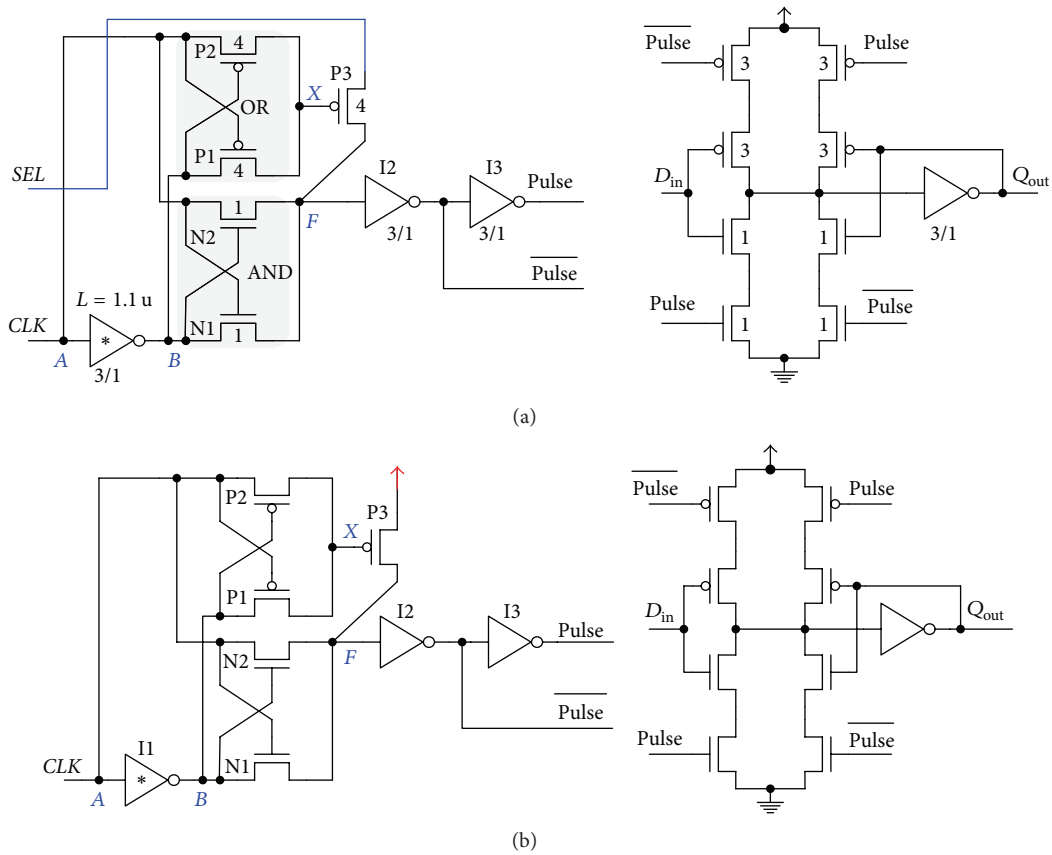

Figure 1: Pulse-triggered base FF designs. (a) Proposed pulse-triggered base dual-mode FF design. (b) Design [6].

minimized by successfully integrating both pulse generation logics into a unified module. The proposed design also exhibits competitive power and speed performance when compared with other single-mode P-FF design.

2. Proposed Design

The proposed dual-mode pulse generator is shown in Figure 1(a). It includes a 5-transistor core logic (N1, N2, P1, P2, and P3) responsible for pulse generation at the clock edges, a delay inverter I1 to create a delay skew between the *CLK* signal and its complement, and two trailing inverters, I2 and I3, to ensure the driving capability and to restore the degraded voltage swing of the generated pulses. The pulse generation core logic has 3 inputs, two complementary and delay skewed clock signals and a triggering mode select control signal. The core logic contains an OR module and an AND module, both implemented in simple pass transistor logic (PTL) circuits. The operation of the proposed 5-T core logic is as follows.

When the mode select signal *SEL* is set to "1," the core logic is working in a dual-edge pulse generation mode. The P3 transistor serves as a pull-up transistor for level restoring and provides signal negation to the output of the OR module. When combining with the OR module, it becomes a NOR module without a pull down circuitry at its output. The outputs of the NOR and the AND modules are tied together and form a wired OR function. It leads to an XNOR function at node *F*. The resultant circuit resembles the dual-edge pulse generator design presented in [6] as shown in Figure 1(b). The NOR and the AND modules, taking complementary clock signals as input, have their outputs normally kept at "0" except for the time instances of clock transition when both input signals are temporarily identical. In these time instances, a transient signal "1" with its pulse width equal to the delay created by inverter I1 will appear at node *F*. The AND module is responsible for pulse generations when both inputs are "1," which corresponds to the rising edges of the *CLK* signal. The height of the generated pulses, however, is one V_{TN} short from the V_{DD} due to the threshold voltage loss effect caused by nMOS pass transistors N1 and N2. This problem, however, is remedied by the inverter buffer I2. Since the pulse duration is short, the incurred static power overhead of I2 due to threshold voltage loss is small. Similarly, the NOR module is responsible for pulse generations when both inputs are "0," which corresponds to the falling edges of the *CLK* signal. The height of the generated pulses is level intact due to the pull-up P3 transistor.

When signal *SEL* is "0," the NOR module is disabled. As a result, the pulse generation is carried out solely by the AND module, which operates only on the rising edges of the clock. However, it should be noted that the AND module implemented in only two nMOS pass transistors is not a full blown logic. What seems problematic is the case when

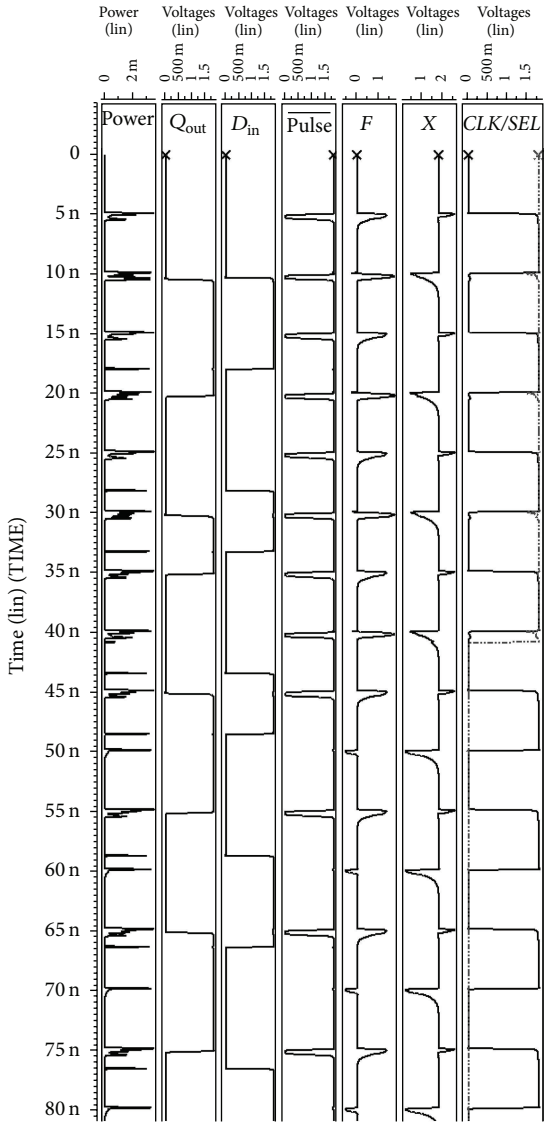

Figure 2: Simulation waveforms of proposed FF design @100 MHz.

inputs (A, B) equal $(0, 0)$, while signal *SEL* is set to "0." Both the AND module and the P3 transistor are turned off, and node *F* is technically left floating. This problem, nonetheless, will not affect the functioning of pulse generation. Firstly, the duration of inputs (A, B) equal to $(0, 0)$ is too short to cause any significant voltage drift at node *F*. Secondly, the case of (A, B) equal to $(0, 0)$ is always preceded by the case of (A, B) equal to $(1, 0)$. Node *F* is thus always discharged to "0" by the AND module in the first place, and the value retains when (A, B) becomes $(0, 0)$. This ensures the correct functioning of pulse generation, and a novel dual-mode pulse generator design can be obtained in 5 transistors. Combining the presented pulse generator with a simple transparent latch, as shown in Figure 1(a), leads to a triggering mode programmable pulse-triggered FF design.

Since the mode select signal *SEL* drives the P3 transistor directly, the incurred power consumption of the driving circuit and the speed impact due to *SEL* must be analyzed as well. When signal *SEL* is set to "1," it assumes the role of V_{DD} and provides signal pull-up to node *F*. The incurred power can be mostly offset by the saving in V_{DD} power. When signal *SEL* is set to "0," P3 transistor remains off and no extra power will be drawn from signal *SEL*. In terms of the speed metrics, as signal *SEL* is normally static, it will not cause any speed penalty arising from signal propagation.

3. Simulation Results

Since the generated pulse width is crucial to the correctness of data capturing and hold time in the trailing latch, transistor of the pulse generator is sized carefully to cope with any process variation [9]. The two buffer designs are optimized subject to the tradeoff between power and data-to-Q delay. Figure 2 shows the postlayout simulation waveforms (at 100 MHz) of the presented pulse-triggered FF design implemented on a TSMC 0.18 μm 1P6M CMOS technology. The output is loaded with a 20 fF capacitor. The operating conditions used in simulations are (500 MHz/250 MHz @1.8 V). The 500 MHz and 250 MHz settings are used, respectively, in the single- and the double-edge triggered modes for a fair comparison in power consumption.

Besides the typical condition (TT), simulations under different process corners (FF, SS, SF, and FS) were also conducted to ensure the adequacy of the generated pulse clock width. Dynamic power occurs on the time instances of pulse generation and input data transition. Simulation waveforms also reveal the occurrences of small spikes in both node *X* and node *F* due to the bootstrap effect. These spikes of node *F* were removed by inverter I2, and no power penalty was identified on the buffer stage [9].

To elaborate more on the power consumption behavior of the proposed design, six test patterns, each exhibiting a different data switching probability, are applied. Five of them are deterministic patterns with 0% (all-zero and all-one), 25%, 50%, and 100% data transition probabilities, respectively [1]. The 6th one is a random test pattern with 30% bit "1" population. Besides the proposed design, we also include a single-mode (double-edge triggered only) design [6] as a reference in simulations. The results are illustrated as a bar chart in Figure 3. Since the power consumption of the pulse generator is constant regardless of the data pattern, the total FF power consumption increases mildly with respect to the data switching activities. The single-edge triggered mode operation is less power efficient than the double-edge counterpart. This is mainly attributed to the pulse generator power consumption on the unused falling edges in single-edge-triggered mode operation. The proposed design, after including the incurred power overhead in mode control, still exhibits a slight power advantage over the design [6] in double-edge triggered mode operation. Figure 4 shows both design PDP_{DQ} performance at different process corners. The proposed design will keep their advantages through process corners from these simulation results.

Table 1 summarizes the transistor counts, the layout areas, the setup times, the hold time, the D-to-Q delays, and the power-delay product (PDP) under 25% data switching probability of both FF designs. The transistor count of the

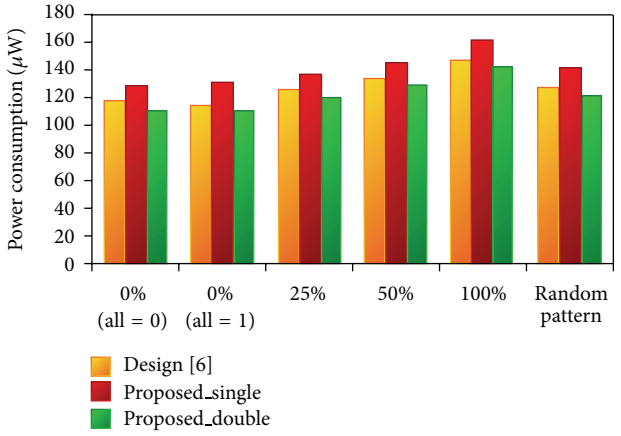

Figure 3: Power consumption under different test patterns.

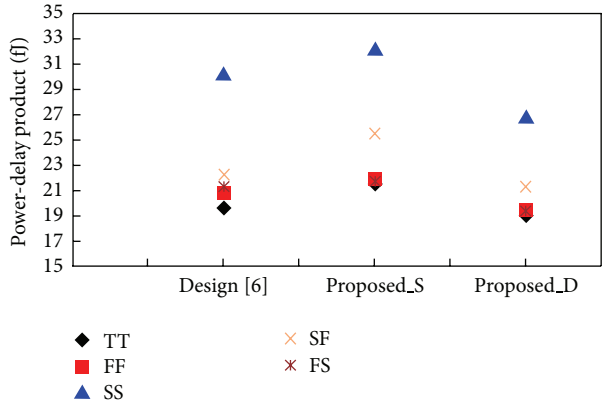

Figure 4: Power-delay product comparisons at different process corner.

Table 1: Features summarized of flip-flop designs.

Pulse-triggered flip-flop Designs	Design [6]	Proposed design	
Edge triggering mode	Double	Single	Double
Number of transistors	21	21 + 2 (Inverter)	
Layout area (um^2)	249.21	271.09	
Setup time (pS)	−216	−225	−220
Hold time (pS)	70	79	73
Data-to-Q (pS)	157	157	158
PDP_{DQ} (fJ)	20.81	21.53	19.08

proposed design is slightly larger than the single-mode design in [6]. The layout area overhead is about 8%. The setup time, hold time, and the data-to-Q delay are comparable in both designs. The power-delay product (PDP) of the proposed design is superior to the reference design in double-edge triggered mode operation. This shows that the proposed FF design, featuring dual triggered mode operations, can perform as efficiently as those single-mode designs.

4. Conclusion

In conclusion, in this paper, a novel dual-mode edge triggered FF design was presented. It features a low complexity 5-T core logic design supporting two modes of pulse generation. Elaborate circuit analyses were provided to prove the design functioning correctly and free from common pass transistor logic circuit pitfalls. Postlayout simulations were also conducted to show the correctness and the effectiveness of the design.

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References

[1] V. Stojanovic and V. G. Oklobdzija, "Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 4, pp. 536–548, 1999.

[2] H. Partovi, R. Burd, U. Salim, F. Weber, L. DiGregorio, and D. Draper, "Flow-through latch and edge-triggered flip-flop hybrid elements," in *Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC '96)*, pp. 138–139, February 1996.

[3] F. Klass, C. Amir, A. Das et al., "A new family of semi-dynamic and dynamic flip flops with embedded logic for high-performance processors," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 712–716, 1999.

[4] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, "Comparative delay and energy of single edge-triggered & dual edge-triggered pulsed flip-flops for high-performance microprocessors," in *Proceedings of the International Symposium on Low Power Electronics and Design*, pp. 147–152, Huntington Beach, Calif, USA, August 2001.

[5] B. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statistical power reduction," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 8, pp. 1263–1271, 2001.

[6] Y. H. Shu, S. Tenqchen, M. C. Sun, and W. S. Feng, "XNOR-based double-edge-triggered flip-flop for two-phase pipelines," *IEEE Transactions on Circuits and Systems II*, vol. 53, no. 2, pp. 138–142, 2006.

[7] C. Villa, D. Vimercati, S. Schippers et al., "A 65 nm 1 Gb 2b/Cell NOR flash with 2.25 MB/s program throughput and 400 MB/s DDR interface," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 1, pp. 132–140, 2008.

[8] J. Bauer, S. M. Trimberger, and S. P. Young, "FPGA memory element programmably triggered on both edges," U.S. Patent 6072348, 2000.

[9] Y. T. Hwang, J. F. Lin, and M. H. Sheu, "Low-power pulse-triggered flip-flop design with conditional pulse-enhancement scheme," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 20, no. 2, pp. 361–366, 2012.