Research Article

Design a Bioamplifier with High CMRR

Yu-Ming Hsiao, Miin-Shyue Shiau, Kuen-Han Li, Jing-Jhong Hou, Heng-Shou Hsu, Hong-Chong Wu, and Don-Gey Liu

Department of Electronic Engineering, Feng Chia University, Taichung 40724, Taiwan

Correspondence should be addressed to Don-Gey Liu; dgliu@fcu.edu.tw

Received 23 December 2012; Accepted 5 April 2013

Academic Editor: Yeong-Lin Lai

Copyright © 2013 Yu-Ming Hsiao et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

A CMOS amplifier with differential input and output was designed for very high common-mode rejection ratio (CMRR) and low offset. This design was implemented by the $0.35\ \mu\text{m}$ CMOS technology provided by TSMC. With three stages of amplification and by balanced self-bias, a voltage gain of 80 dB with a CMRR of 130 dB was achieved. The related input offset was as low as $0.6\ \mu\text{V}$. In addition, the bias circuits were designed to be less sensitive to the power supply. It was expected that the whole amplifier was then more independent of process variations. This fact was confirmed in this study by simulation. With the simulation results, it is promising to exhibit an amplifier with high performances for biomedical applications.

1. Introduction

For biomedical applications, a voltage amplifier with a gain of 80 dB and a high CMRR is required as a building block in front-end subsystems [1, 2]. Since the voltage level of physiologic signals at the front-end subsystem is very weak, processes for analog signals usually include several steps of amplification, filtering, offset adjustment, and electrical conditioning. After suitable processing, the signal will then be large enough and effectively suitable for analog-to-digital conversion at later stages [3–5].

In considering the physiological signals extracted from human bodies, the amplitude of an electrocardiographic (ECG) signal is usually less than $100\ \mu\text{V}$. Such value is very weak as compared to the noise floor and imperfection of the commonly used operational amplifiers (OPAs). An instrumentation amplifier (IA) is usually employed to achieve the required performances.

In addition to the requirement of high voltage gain in constructing the amplifiers for an IA, another important requirement for the amplifiers is CMRR. According to the recommendations of Association of the Advancement of Medical Instrumentation (AAMI), CMRR is required to be higher than 90 dB with the open-loop voltage gain higher than 80 dB.

In this study, the $0.35\ \mu\text{m}$ CMOS technology of TSMC was employed in designing a high performance amplifier.

In our study, a high-voltage-gain amplifier was tried with a self-biasing technique to have a high CMRR and low input offset and to be less sensitive to process variations. The simulation was performed based on the models supported by Chip Implementation Center (CIC). The related results will be illustrated.

2. Design Details

2.1. Design of the Differential Amplifier. For the purposes of high CMRR and low offset at the input, differential configuration with a symmetrical floor planning in layout will be preferred in the design of an amplifier.

Figure 1 shows the schematic of an amplifier with the differential configuration both at the input and at the output. In this circuit, transistors M_1 and M_2 are the differential pair for amplification. The block with I_T and R_T forms a tail current bias. The resistors R_{D1} , R_{D2} , R_{L1} , and R_{L2} are taken as the loads.

Figure 2 shows an alternative representation of the amplifier in Figure 1. The input and output signals can be decomposed into the common and the differential modes. With this decomposition, the performance of the amplifier in the common mode and the differential mode can be discussed separately.

FIGURE 1: Schematic of the differential amplifier.

FIGURE 2: Representation of the amplifier in the common and the differential modes.

In the common mode, the two output voltages will be the same if the circuit is ideal in a form of total symmetry. This requires that the branches for I_{D1} and I_{D2} are matched with $R_{L1} = R_{L2}$ and $R_{D1} = R_{D2}$.

For the current bias as the tail, a current mirror with a stable reference current, I_{REF} , can be employed in the integrated circuits to give a high output resistance, R_T .

Other techniques to improve the performance of this amplifier will be discussed in detail in the following.

For practical design, there exist variations in the devices even with the integrated circuit technology. The output voltage will not be zero for the common input condition. For example, the imperfections in the threshold voltage and the transconductance of the MOS transistors and the variation in R_D are uncorrelated. The resulted input offset voltage can be expressed as

$$V_{OS} \equiv \frac{V_{OUT}|_{V_d=0}}{A_d} = \frac{V_{OV}}{2} \sqrt{\left(\frac{\Delta R_D}{R_D}\right)^2 + \left(\frac{\Delta(W/L)}{(W/L)}\right)^2 + \left(\frac{\Delta V_{TH}}{(V_{OV})/2}\right)^2}. \quad (1)$$

According to the analysis in the common mode and the differential mode, the output voltage can be expressed as the

sum of the amplification of the signals of both modes. The relations for the outputs can be written at follows:

$$V_{O1} = \frac{A_d}{2} \times v_d + A_{cm} \times v_{cm}, \quad (2a)$$

$$V_{O2} = -\frac{A_d}{2} \times v_d + A_{cm} \times v_{cm}, \quad (2b)$$

where $v_d \equiv v_{in1} - v_{in2}$, $v_{cm} \equiv (v_{in1} + v_{in2})/2$, A_d is the differential-mode voltage gain, and A_{cm} is the common-mode gain. It is similar for the expression for V_{O2} . The common-mode rejection ratio (CMRR) is then defined as

$$CMRR \equiv \left| \frac{A_d}{A_{cm}} \right|. \quad (3)$$

A good amplifier is required to have a high A_d with a nearly zero A_{cm} . Due to the variations in the fabrication process, it is a big challenge to achieve a high CMRR with a low input offset. In this study, a balanced bias technique was employed to reduce the sensitivity to the process variation. Good properties of this amplifier have been confirmed in the postlayout simulation.

2.2. Tristage Amplifier. In this design, three stages of amplification were employed to achieve the required voltage gain and CMRR at the same time for weak biosignals. Figure 3 shows the detailed circuit in this design. Table 1 gives the specifications for this design.

As seen in Figure 3, the first stage is composed of M_1 – M_5 . The second stage includes M_6 – M_{12} . These two stages can be used as an operational transconductance amplifier (OTA) [6, 7] or a folded cascade amplifier [8]. The third stage comprising M_{13} and M_{14} forms a type A common-source (CS) amplifier to drive loads.

Transistors M_{S1} – M_{S6} provide a bias current for the first-stage amplifier. The source of biasing for the second-stage amplifier comes from the balanced self-bias current mirror, M_8 – M_{11} , in Figure 3. In this part, the biasing currents were less sensitive to the level of the power supply. In addition, the complementary arrangement of the loads at the first-stage and the second-stage amplifiers would reduce the variation of the amplification if there are changes in the NMOS and PMOS. The bias voltage for the third stage comes from M_9 in the second stage. Since the bias currents in M_9 and M_{11} were constant, the gate bias for M_{13} would be constant. Therefore, the properties of the whole amplifier would be less affected by the uncertainties in fabrication.

For the design strategy, the first stage was designed to achieve a high CMRR rather than a high voltage gain. The overall voltage gain was boosted at the second and the third stages. Since this amplifier was designed for biomedical applications, the voltage gain was tried to be as high as possible with a moderate small bandwidth around 100 Hz. At the third stage, a clamping circuit can keep dynamic tracking of the output gain such that the voltage gain would be less affected by variations in the transistors.

In addition to the electrical considerations, the layout and circuit for the first and second stages were designed as

FIGURE 3: Structure of the tristage amplifier.

TABLE 1: Specifications for the bioamplifier.

Parameter	Spec.	Value
V_o/V_i	$\geq$	20 kV/V
A_{VO}	$\geq$	80 dB
PM	$\geq$	60°
UGF	$\geq$	2 MHz
CMRR	$\geq$	90 dB
PD	$\leq$	1 mW

symmetrical as possible. In this way, the common signals would be cancelled out in the differential structure. Therefore, the equivalent input offset would be suppressed effectively.

With the above techniques, an amplifier with high voltage gain, high CMRR, low offset, and low drift voltage can be achieved and confirmed in the simulation.

For our circuit, the level of the power supply was set at 3.3 V by setting V_{DD} at 1.65 V and $-V_{SS}$ at -1.65 V. In the meanwhile, the power dissipation was specified below 1 mW for portable operations. With this constraint, as explained by (4), the total current consumed in this circuit cannot be more than 0.303 mA:

$$I_{\text{Supply}} \leq \frac{P_{D,\text{Spec.}}}{V_{\text{Supply}}} = 0.303 \text{ mA}. \quad (4)$$

As for the stability consideration, the phase margin (PM) of this amplifier was tuned to be 60° in our simulation [9]. In this design, we select $G_{m3} \geq 10G_{m2}$. And the second pole was set as $\omega_{p2} \geq 2.2 \times \omega_T$. Therefore, the Miller compensation capacitor, C_C , was selected to be 18 pF by the following calculation:

$$C_C \geq 2.2 \times \frac{G_{m1}}{G_{m2}} \times C_{O2} = 0.22C_{O2}. \quad (5)$$

2.3. Transistor Dimensions. In general, the tail current was required to be higher than the product of the screw rate and C_C . In this study, this product was 10 μA for the second stage. Since the screw rate for the case of light loads is not required strictly, the tail current at stage 2 was selected as 15 μA .

The bias currents for the two branches through M_6 and M_7 equally divide the tail current into $I_{D6} = I_{D8} = I_{D10} = I_{D7} = I_{D9} = I_{D11} = 7.5 \mu\text{A}$.

With this bias current, the transconductance, g_m , and the gate-to-source voltage, V_{GS} , can be designed by a suitable dimension ratio, W/L , by the following relations:

$$I_D = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_{OV})^2 \cdot (1 + \lambda V_{DS}), \quad (6)$$

$$\begin{aligned} g_m &= (\mu_n \cdot C_{ox}) \cdot \left(\frac{W}{L}\right) \cdot (V_{OV}) \cdot (1 + \lambda V_{DS}) \\ &= \sqrt{2\mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right) \cdot I_D \cdot (1 + \lambda V_{DS})} \\ &= \frac{2 \times I_D}{V_{OV}}, \end{aligned} \quad (7)$$

where the overdrive voltage $V_{OV} \equiv V_{GS} - V_{th}$.

For the third stage, its transconductance gain, G_{m3} , is the same as g_{m13} of M_{13} . We chose $G_{m3} \geq 10G_{m2}$; that is, $G_{m3} \geq 590 \mu\text{A/V}$ and $g_{m13} = G_{m3} = 600 \mu\text{A/V}$. In addition, the overdrive voltage for M_{13} was selected as $V_{OV13} = 0.2 \text{ V}$; that is, $V_{GS13} \equiv V_{OV13} + V_{tn} = 0.85 \text{ V}$. Therefore, $V_{DS13} = V_{DS14} = 1.65 \text{ V}$. The dimension ratio for $(W/L)_{13}$ can be determined by (6).

In this design, we used $M_{S1} \sim M_{S6}$ and a resistor R_S to form a self-bias circuit with a boot-strapping positive

TABLE 2: Variations of the simulated properties of the bio-amplifier with 5 fabrication corners.

Items	SS	SF	TT	FS	FF
V_o/V_i	-33.1 k	-29.7 k	-29.3 k	-27.7 k	-22.6 k
A_{VO} (dB)	90.4	89.5	89.3	88.9	87.1
PM	88.8°	89.8°	89.7°	89.7°	91.0°
f_{H3db} (Hz)	63.0	63.1	79.4	63.1	82
UGF (Hz)	1.41E + 06	1.47E + 06	1.46E + 06	1.44E + 06	1.52E + 06
CMRR (dB)	136.4351	136.2238	136.7342	136.5733	135.778
PD (μ W)	357	332	328	324	316
V_{os} (μ V)	10.8	10.1	5.2	0.033	20.8

feedback. The current controlled by I_{REF} can be expressed as

$$I_{REF} \times R_S = V_{GS_{S6}} - V_{GS_{S5}} = \sqrt{\frac{I_{REF}}{K_{S6}}} - \sqrt{\frac{I_{REF}}{K_{S5}}} \quad (8)$$

By (8), we selected the dimension ratio of M_{S5} to be 1/4 of that of M_{S6} , that is,

$$\left(\frac{W}{L}\right)_{S5} = \frac{1}{4} \left(\frac{W}{L}\right)_{S6} \quad (9)$$

The resistance can be obtained as follows:

$$R_S = \frac{1}{I_{REF}} \sqrt{\frac{I_{REF}}{K_{S5}}} \quad (10)$$

The reference current was set as $I_{REF} = 5 \mu A$. The dimension ratio for $M_{S1} \sim M_{S4}$ can also be derived by (6).

3. Simulation and Verification before Fabrication

In this study, HSPICE with the device models for $0.35 \mu m$ CMOS technology from TSMC was employed for the simulation and analysis. The performance of the whole circuit was verified first in the prelayout simulation. Then, the physical layout was implemented and the related parameters were extracted. With the obtained information of the physical layout, the postlayout simulation was performed to check the feasibility of our layout. Corner simulations were also performed to check the effect of the process variation on the performance of our amplifier.

Figures 4–7 illustrate the related performances with 5 corner conditions in fabrication. Table 2 lists other performance items with the 5 corners. With these results, we can find that the voltage gain in Figure 6 can be kept higher than 80 dB. And the variation of the obtained gains due to the uncertainty in fabrication can be smaller than 5 dB. It can also be found in Figures 4 and 5 that the phase margin is much larger than 60° . In Figure 5, we can confirm that the variation of phases is insignificant. As shown in Figure 7, the obtained CMRR is as high as 130 dB for frequency up to 10 kHz. The variation of CMRR due to the fabrication is also insignificant. With these results, a bio-amplifier both with a very high CMRR and a high voltage gain at the same time can be expected for the fabricated chips.

FIGURE 4: Frequency response for the bio-amplifier in the typical fabrication condition (TT).

FIGURE 5: Simulated phases for the bio-amplifier in 5 corner conditions.

4. Conclusion

A bio-amplifier with high gain and high CMRR was designed and verified in this study. According to the obtained performance properties in Table 2, it is promising that a process independent performance can be obtained for this amplifier.

FIGURE 6: Simulated gains for the bio-amplifier in 5 corner conditions.

FIGURE 7: Simulated CMRRs for the bio-amplifier in 5 corner conditions.

Acknowledgments

The authors acknowledge the support from Chip Implementation Center (CIC) and Chang Bin Show Chwan Memorial Hospital with the research resources. Partial financial support from National Science Council (NSC), republic of china, is also acknowledged.

References

- [1] K. A. Ng and P. K. Chan, "A CMOS analog front-end IC for portable EEG/ECG monitoring applications," *IEEE Transactions on Circuits and Systems I*, vol. 52, no. 11, pp. 2335–2347, 2005.
- [2] B. Wang, H. Ji, Z. Huang, and H. Li, "A high-speed data acquisition system for ECT based on the differential sampling

method," *IEEE Sensors Journal*, vol. 5, no. 2, pp. 308–311, 2005.

- [3] C. H. Chan, J. Wills, J. LaCoss, J. J. Granacki, and J. Choma Jr., "A novel variable-gain micro-power band-pass auto-zeroing CMOS amplifier," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '07)*, pp. 337–340, May 2007.
- [4] B. Premanode, N. Silawan, and C. Toumazou, "Drift reduction in ion-sensitive FETs using correlated double sampling," *Electronics Letters*, vol. 43, no. 16, pp. 857–859, 2007.
- [5] J. Wu, G. K. Fedder, and L. R. Carley, "A low-noise low-offset chopper-stabilized capacitive-readout amplifier for CMOS MEMS accelerometers," in *Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC '02)*, pp. 428–425, February 2002.
- [6] G. Nicollini and C. Guardiani, "3.3-V 800-nV rms noise, gain-programmable CMOS microphone preamplifier design using yield modeling technique," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 8, pp. 915–921, 1993.
- [7] V. Ivanov, J. Zhou, and I. M. Filanovsky, "A 100-dB CMRR CMOS operational amplifier with single-supply capability," *IEEE Transactions on Circuits and Systems II*, vol. 54, no. 5, pp. 397–401, 2007.
- [8] P. C. de Jong, G. C. M. Meijer, and A. H. M. van Roermund, "A 300°C dynamic-feedback instrumentation amplifier," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 1999–2008, 1998.
- [9] K. N. Leung and P. K. T. Mok, "Analysis of multistage amplifier-frequency compensation," *IEEE Transactions on Circuits and Systems I*, vol. 48, no. 9, pp. 1041–1056, 2001.