Research Article

An FPGA Based Controller for a SOFC DC-DC Power System

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Fuel cells are an attractive option for alternative power and of use in a variety of applications. This paper proposes a state space model for the solid oxide fuel cell (SOFC) based power system that comprises fuel cell, DC-DC buck converter, and load. In this investigation we have taken up a case study for SOFC feeding a DC load where a DC-DC buck converter acts as the interface between the load and the source. A proportional-integral (PI) controller is used in conjunction with pulse width modulation (PWM) that computes the pulse width and switches the MOSFET at the right instant so that the desired voltage is obtained. The proposed model is validated through extensive simulation using MATLAB/SIMULINK. Controller for the fuel cell power system (FCPS) is prototyped using XC3S500E development board containing a SPARTAN 3E Xilinx FPGA that simplifies the entire control circuit besides providing additional flexibility for further improvement. The results clearly indicate improved performance and validate our proposed model.

1. Introduction

Nowadays, people depend on electrical energy more than ever; thus the importance of generating electrical energy increases significantly. Fuel cells are alternative power sources that have recently attracted a great deal of attention. Fuel cell generates dc voltage from the chemical reaction of hydrogen and oxygen and the by-products are water and heat [1–3]. Fuel cell can serve as another source of energy in the event of power outage. People use fuel cells in a vast range of applications because of their clean and efficient way of supplying electric power. The fuel cells are used in standalone purposes at homes, schools, and hospitals and in numerous vehicles.

Different types of fuel cells exist in the world. From these fuel cells, solid oxide fuel cell (SOFC) is an important one [4, 5] because of its high efficiency and solid material (electrolytic material is ceramic) it uses. In SOFC, electric power is generated by passing hydrogen gas from anode and oxygen from cathode. There is an electrolyte between anode and cathode which fastens the electric charge as shown in Figure 1 [6]. In modelling a fuel cell powered system, it is necessary to optimize not only the design of the SOFC but also the related power conditioning circuits

along with required controllers. Mainly, these conditioning circuits include a DC-DC converter and a load. The DC-DC converter is designed to convert the unregulated DC output voltage of the SOFC to a lower/higher and stable DC voltage. Many researchers have proposed fuzzy logic control (FLC) schemes for regulating the conditioning circuits. It maintains a constant electrical power for a wide range of applications [7–10]. Use of PI controllers in a fuel cell power system is also available in the literature [11]. However, in this paper we adopt a state space modelling approach that facilitates modelling and control in a better way. We have also developed an FPGA based controller that makes the control circuit fairly simpler and adaptable. In this investigation we have restricted to PI controller, that is, usually accepted as industry standard.

The PI controller provides the compensation in the feedback loop of the closed loop system of SOFC model. PI controller is a particular case of lag-lead compensator which guarantees reduced steady-state error with acceptable rise times. A buck converter has good stability margin but poor steady-state accuracy. It is one of the most common types of feedback controllers used in many dynamic systems. It is widely used in different areas such as process control, manufacturing, robotics, and power systems. Due to its simple structure and robust performance, PI controller is

FIGURE 1: Basic working principle of fuel cell.

mostly preferred in industries as it does not require precise analytical model of the system to be controlled. It is quite easy to tune the parameters as well.

To facilitate the complete design of a fuel cell powered systems, this paper presents a comprehensive MATLAB/SIMULINK model that comprises a SOFC fuel cell stack, a DC-DC buck converter, and associated controllers. An FPGA based control scheme is proposed for the DC-DC buck converter to guarantee the stable and low output voltage against load variations in the output voltage of SOFC model [12]. FPGAs are configurable ICs and are used to implement logic functions. They ensure ease of design, lower development costs, more product revenue, and the opportunity to speed products to the market. At the same time, they are superior to software-based controllers as they are more compact, power-efficient while adding high speed capabilities [13]. The conventional microprocessors are serial machines which perform one instruction at a time, while the structure of FPGA is adapted to parallel, which means that the performance is several degrees better. Another advantage is that only one FPGA chip is capable of performing multiple functions including control, signal processing, and system input and output. This greatly reduces the number of ICs required and increases the reliability. We are using VHDL as our coding language to implement the proposed controller onto the FPGA. VHDL is a hardware description language that can be used to model a digital system at a different level of abstraction, ranging from the algorithmic level to the gate level with different modelling styles. It gives us freedom of describing a digital system in the concurrent or sequential or mixed behaviour with or without timing.

The extensive simulation results confirm that the FPGA control scheme provides an effective means of regulating the output voltage of SOFC in accordance with the changes in the load demand. Detailed mathematical equations are presented

for all of the major SOFC components, conditioning circuits, and controllers.

2. Fuel Cell Description and Performances

Fuel cells are static energy conversion devices that convert the chemical energy of fuel cell into DC electrical energy. They are promising to be an important distributed generation source of the future due to their advantages, such as high efficiency, zero or low emission, and flexible modular structure. The model of the SOFC power plant used in this paper is based on the dynamic stack model developed and validated in [14, 15] the earlier literature. One major operating variable is the utilisation factor (U_f), referring to the fraction of the total fuel (oxidant) introduced into a fuel cell that reacts electrochemically:

$$U_f = \frac{q_{H_2}^{in} - q_{H_2}^{out}}{q_{H_2}^{in}} = \frac{q_{H_2}^r}{q_{H_2}^{in}}, \quad (1)$$

where q_{H_2} is the hydrogen molar flow. High utilisations are considered desirable because they minimize the required fuel and oxidant flow. However, utilisation factors that are pushed too high result in significant voltage drops. The SOFC model consists of a number of cells connected in series or parallel according to the DC output voltage/current requirements. Output voltage of each cell in normal condition is 1.1 volts. Hydrogen and air passes through the cells. By controlling the amount of hydrogen fed into the fuel cell system and then output voltage of fuel can be controlled. Nernst's equation and Ohm's law determine the voltage magnitude of the fuel cell

stack [16]. The stack DC output voltage of fuel cell system can be written as

$$V_{FC} = N_0 \left(E_0 + \frac{RT}{2F} \left(\ln \left(\frac{P_{H_2} \cdot \sqrt{P_{O_2}}}{P_{H_2O}} \right) \right) \right) - r I_{FC}, \quad (2)$$

where N_0 is the number of cells connected in series; E_0 is the standard reversible voltage; R is the universal gas constant; T is the operating temperature; I_{FC} is the fuel cell stacks current; F is the faraday's constant.

P_{H_2} , P_{O_2} , and P_{H_2O} are determined by the following differential equations:

$$\begin{aligned} \dot{P}_{H_2} &= -\frac{1}{\tau_{H_2}} \left(P_{H_2} + \frac{1}{K_{H_2}} (q_{H_2}^{in} - 2 \cdot K_r \cdot I_{FC}) \right), \\ \dot{P}_{O_2} &= -\frac{1}{\tau_{O_2}} \left(P_{O_2} + \frac{1}{K_{O_2}} (q_{O_2}^{in} - K_r \cdot I_{FC}) \right), \\ \dot{P}_{H_2O} &= -\frac{1}{\tau_{H_2O}} \left(P_{H_2O} + \frac{2}{K_{H_2O}} \cdot (K_r \cdot I_{FC}) \right). \end{aligned} \quad (3)$$

The relationship between the fuel cell stack current and the molar flow of hydrogen can be written as

$$q_{H_2} = \frac{N_0 I_{FC}}{2 \cdot F \cdot U}. \quad (4)$$

The polarisation curve presents the fuel cell output voltage as function of the current density in the steady state. The result obtained through simulation is presented in Figure 2. The total output voltage of SOFC stack can be obtained as

$$V_{FC,Total} = N_0 \cdot V_{FC}. \quad (5)$$

Electrical power in watts supplied by the fuel cell to the load can be determined using the following equation:

$$P_{FC} = V_{FC} \cdot I_{FC}. \quad (6)$$

The fuel cell efficiency can be determined using standard formulae [17]:

$$\eta = U \cdot \frac{V_{FC}}{1.48}, \quad (7)$$

where U is the utilisation factor, generally in the range of 85%, and 1.48 V represents the maximum voltage that can be obtained using the higher heating value for the hydrogen enthalpy.

2.1. V-I Characteristics Curve SOFC Stack. The response of the fuel cell stacks which produces DC electric power from the chemical reaction of hydrogen and oxygen is much faster than that of the reformer [18, 19]. A voltage-current characterisation curve of a fuel cell stack is represented in Figure 2. The cell voltage decreases as the stack current increases. Figure 2 shows a static voltage-current polarisation curve of a single fuel cell. There are three regions in the

FIGURE 2: V-I Characteristic curve of single fuel cell.

curve such as region of active polarisation, region of ohmic polarization, and region of concentration polarisation. In the region of active polarisation, the cell voltage drops suddenly with even small current increase. In the region of ohmic polarisation, the cell voltage linearly decreases as current increases. The fuel cell normally operates in this region. That is why we consider ohmic loss in fuel cell modelling. Finally, in region of concentration polarisation, the voltage collapses steeply when current exceeds the upper limit of safe operation. Here, we are not considering this region as it will damage the fuel cell, as primarily starvation of hydrogen (fuel) will occur.

In this paper, the solid oxide fuel cell (SOFC) is modelled and investigated. The fuel cell polarisation curve is generated using regression models with current, vapour saturation pressure, and oxygen and hydrogen partial pressure. The hydrogen and oxygen pressure can calculate the cathode pressure, cathode relative humidity, and vapour saturation pressure.

To obtain the voltage-current characterisation curve of the SOFC stack, the following limitations are made:

- (i) stable fuel cell temperature;
- (ii) uniform gas distribution;
- (iii) Nernst's equation is applied;
- (iv) Fuel cell utilisation factor below 90%.

2.2. SOFC Model with DC-DC Buck Converter. A model for SOFC and DC-DC buck converter is presented in [6, 20]. In the present investigation, we take up a state space modelling approach to gain greater insights. The circuit of this model is illustrated in Figure 3. In this system, i_l , V_c , and V_{CFC} are the state variables. E_{Nernst} of fuel cell (controlled by pressure of H_2 and O_2) and switching signal "S" of DC-DC buck converter are assumed to be control signals. Output current of SOFC stack current (i_l) and output voltage of DC-DC converter (V_c) are treated as output of the systems. We consider the state variables as

$$\dot{x} = [x_1 \ x_2 \ x_3]^T = [i_l \ V_c \ V_{CFC}]^T$$

$$\text{Control signals } u = [u_1 \ u_2]^T = [E_{Nernst} \ S]^T \quad (8)$$

$$\text{Outputs } y = [y_1 \ y_2]^T = [i_l \ V_c]^T.$$

FIGURE 3: Fuel cell with DC-DC buck converter.

For reaching state space equations of proposed system, switching signal “S” is treated to be either 0 or 1.

Case 1. for “S” = 1, the circuit can be redrawn as shown in Figure 4; the corresponding state space equations can be derived from KVL and

$$\begin{aligned} V_{FC} - L \frac{di_l}{dt} - V_c &= 0, \\ \dot{i}_l &= \frac{1}{L} (V_{FC} - V_c), \\ \dot{V}_c &= \frac{1}{C} \left(i_l - \frac{V_c}{R_L} \right), \\ \dot{V}_{CFC} &= \frac{1}{C} \left(i_l - \frac{V_c}{R_L} \right) \end{aligned} \quad (9)$$

Case 2. For “S” = 0, the circuit gets modified as shown in Figure 5; the state space equations now are from KVL and KCL:

$$\begin{aligned} V_c + L \frac{di_l}{dt} &= 0, \\ \dot{i}_l &= -\frac{V_c}{L}, \\ \dot{V}_c &= \frac{1}{C} \left(i_l - \frac{V_c}{R_L} \right), \\ \dot{V}_{CFC} &= \frac{1}{C} \left(i_l - \frac{V_c}{R_L} \right). \end{aligned} \quad (10)$$

With control signal u_2 , (9) and (10) can be written as

$$\begin{aligned} \dot{i}_l &= \frac{1}{L} (-V_c + (V_{FC} - V_c) u_2) \\ \dot{V}_c &= \frac{1}{C} \left(\left(i_l - \frac{V_c}{R_L} \right) + \left(i_l - \frac{V_c}{R_L} \right) u_2 \right) \\ \dot{V}_{CFC} &= \frac{1}{C} \left(i_l - \frac{V_c}{R_L} \right). \end{aligned} \quad (11)$$

FIGURE 4: Buck converter when switch is ‘ON’.

FIGURE 5: Buck converter when switch is ‘OFF’.

With considering KCL equation in the fuel cell as it was mentioned in (12) and substituting it in (11), we obtained

$$\begin{aligned} V_{FC} &= N * V_{FC} \text{ (for each cell)}, \\ V_{FC} &= u_1 + V_{CFC} - N \cdot R_{ohm} \cdot i_l, \end{aligned} \quad (12)$$

$$\begin{aligned} \dot{i}_l &= \frac{1}{L} [-V_c + (u_1 + V_{CFC} - N \cdot R_{ohm} \cdot i_l - V_c)], \\ \dot{V}_c &= \frac{1}{C} \left(i_l - \frac{V_c}{R_L} + i_l \cdot u_2 - \frac{V_c}{R_L} \cdot u_2 \right), \\ \dot{V}_{CFC} &= \frac{1}{C} \left(i_l - \frac{V_c}{R_L} \right). \end{aligned} \quad (13)$$

FIGURE 6: Block diagram of fuel cell with DC-DC buck converter.

FIGURE 7: DC output voltage of fuel cell.

For converting (13) in standard form of (14), defined as

$$\begin{aligned} \dot{x} &= A \cdot x + B \cdot u, \\ y &= C \cdot x + D \cdot u, \end{aligned} \quad (14)$$

where

$$A = \begin{bmatrix} -\frac{N \cdot R_{ohm}}{L} & -\frac{1}{L} & \frac{1}{L} \\ \frac{1}{C} & -\frac{1}{R_L \cdot C} & 0 \\ \frac{1}{C} & -\frac{1}{R_L \cdot C} & 0 \end{bmatrix}, \quad (15)$$

$$B = \begin{bmatrix} \frac{1}{L} & \frac{V_{Fc} - V_c}{L} \\ 0 & i_l - \frac{V_c}{R_L} \\ 0 & 0 \end{bmatrix},$$

$$C = [0 \ 1 \ 0], \quad D = 0.$$

The complete model of solid oxide fuel cell power system is shown in Figure 6.

In the example, we have considered 39 cells which are connected in series. Each cell gives 1.12 V in normal condition. Figure 7 shows the DC output voltage of SOFC model. This DC output voltage from SOFC model is fed to DC-DC buck converter as an input. It steps down the voltage from 40 V to 19 V which is stable. Figure 8 shows the buck converter output voltages.

FIGURE 8: Output voltage of buck converter.

3. Control Strategies

3.1. PI Controller. The ideal continuous time PI controller can be expressed as

$$y(t) = K_P \cdot e(t) + K_I \cdot \int e(t) \cdot dt, \quad (16)$$

where $y(t)$ is the control output, K_P is the proportional constant, K_I is the integral constant, and $e(t)$ is the error between the references $V_{dc\text{ref}}$ and V_{dc} . The s -domain expression of the corresponding PI controller can be written as

$$Y(s) = \left[K_P + \frac{K_I}{s} \right] E(s). \quad (17)$$

3.2. PWM Technique. Switch-mode DC-DC converters utilize one or more switches to transform DC from one level to another. In a DC-DC converter with a given input voltage, the average output voltage is controlled by controlling duty cycle of the switch pulse. There are two methods for the generation of PWM, one by switching at a constant frequency and adjusting the on duration of the switch to control the average output voltage. The other method is where both the switching frequency and the on duration of the switch are varied. Variation in the switching frequency makes it difficult to filter the ripple components in the input and the output waveforms of the converter.

In this paper, a fixed frequency PWM technique is used. The working principle of this technique is shown in Figure 9. A repetitive signal which decides the frequency of PWM is compared with the PI output which acts as a reference signal. When PI output is more than the repetitive signal, the PWM signal is high and vice versa. When PI output changes, the ON period of the PWM signal changes as shown in Figure 9. Hence, we can control the buck converter output voltages.

3.3. FPGA Implementation of Controller. Fuel cell controller (PI in conjunction with PWM) is implemented in FPGA using VHDL. The PI and PWM controller when configured on field programmable gate arrays (FPGAs) improves the speed, accuracy, power, compactness, and cost effectiveness of the system (see Figure 10).

3.3.1. FPGA Implementation of PI Controller. Implementation equations (16) and (17) of PI controller in FPGA using VHDL

FIGURE 9: PWM duty cycle control structure.

FIGURE 10: Block diagram of FPGA controller for DC-DC buck converter.

FIGURE 11: RTL schematic of PI controller.

FIGURE 12: Test bench waveform of PI controller.

FIGURE 13: RTL schematic of PWM controller.

FIGURE 14: Test bench waveform of PWM controller.

TABLE 1: Design summary of PI controller.

Logic utilization	Used	Available	Utilization
Number of slices	76	4656	1%
Number of slice flip flops	48	9312	0%
Number of 4 input LUTs	139	9312	1%
Number of bonded IOBs	40	232	17%
Number of GCLKs	1	24	4%

needs to be written in discrete time form as FPGA is a digital device.

For this purpose, we used numerical method approach, that is, trapezoidal method that approximates $1/s$ by

$$\frac{1}{s} \Rightarrow \frac{T}{2} \cdot \left(\frac{Z+1}{Z-1} \right), \quad (18)$$

FIGURE 15: Analog capture circuit.

FIGURE 16: SPI control interface of preamplifier.

where T is the sample time. This discrete integral term can be written as

$$y(n) = x(n) + K_I \cdot \frac{T}{2} \cdot u(n), \quad (19)$$

$$x(n+1) = y(n) + K_I \cdot \frac{T}{2} \cdot u(n), \quad (20)$$

where $y(n)$ is the output, $u(n)$ is the error input, and $x(n)$ is the state (see Figures 11 and 12 and Table 1). The complete discrete-time expression of PI controller is written as

$$y(n) = y(n-1) + K_P \cdot u(n) + K_I \cdot \frac{T}{2} \cdot [u(n-1) + u(n)]. \quad (21)$$

3.3.2. FPGA Implementation of PWM Control. The PWM signal generation is done by comparing a stable reference signal which is here taken from a PI controller with a repetitive saw-tooth signal. A repetitive signal is generated by a counter, which counts from zero to maximum value and when it reaches the maximum count, the counter is reset to

TABLE 2: Design summary of PWM controller.

Logic utilization	Used	Available	Utilization
Number of slice flip flops	16	9312	1%
Number of 4 input LUTs	26	9312	1%
Number of Occupied Slices	16	4656	1%
Number of slices containing only related logic	16	16	100%
Total Number of 4 input LUTs	27	9312	1%
Number of bonded IOBs	3	232	1%

zero again. This process is repeated concurrently in a process block. The frequency of the PWM signal is decided by the frequency of this repetitive signal. The N -bit comparator is used, which compares the counter count and the reference signal input. When the reference input is higher than the repetitive signal, the output of PWM signal is low, and when the reference input is lower than the repetitive signal the output of PWM signal is high. In this way, the PWM signal is generated which drives the power switch of the converter. In the SPARTAN 3E Xilinx board, a 14-bit ADC is available that

FIGURE 17: AMP configuration FSM.

FIGURE 18: ADC SPI control interface signals.

gives a precision of 14 bits. The error input is fed to this ADC which gives a 14-bit digital data. The K_I value used in our simulation model in MATLAB/SIMULINK is 500; this can be represented in 9 bits, after the addition and multiplication is done in the PI block; it will give a 24-bit output without any data losses. So a 24-bit counter and comparator are taken. The ADC which can give 14-bit data maximum at the rate of 1.5 MHz is quite sufficient for this type of application (see Figures 13 and 14 and Table 2).

3.3.3. ADC Interface Module. The XC3S500E development board is having an on-board ADC module for digitalizing the analog signal which is interfaced with the board. Figure 15 shows the detailed ADC capture circuit. It consists of a LTC1407A-1 ADC with a programmable preamplifier LTC6912-1. The purpose of the amplifier is to scale the incoming voltage so that it is compatible to the ADC input. Both the preamplifier and ADC are dual channel and are serially programmed or controlled by the FPGA. So, an interface

FIGURE 19: Timing diagram of ADC signal.

FIGURE 20: ADC control FSM.

module is written in VHDL for the serial communication. Serial communication can perform perfectly if the timing constraints are well considered. Figure 16 shows the timing diagram or constraint of the preamplifier.

An FSM is written for configuring the gain of preamplifier. Initially the state will be in IDLE mode and it will wait until CE_AMP signal goes high. Within this state all the signals are in disable mode as AMP_CS is high, MOSI is low, and SCK is low. As CE_AMP goes to high state, it moves to next state where the AMP_CS goes to low state, and in this way the serial communication is done to configure the gain of preamplifier. When the gain is set it generates a signal which is

sent to the main control module which controls all the FSMs. FSM is required for amplifier gain setting, ADC sampling, an FSM for PI and PWM controller, and a main control FSM to control all the FSM. Figure 17 is the FSM for configuring the gain of preamplifier (see Figure 18).

After the GAIN is set, the main control sends a signal to FSM of ADC control to start taking samples and after each sample is captured it is available in 14-bit two's complement after 34 cycles. Then, this 14-bit data is sent to PI which generates reduced error or a reference for PWM signal generator. After a clock cycle, when the data is sent to the PI and PWM module it again goes to take next sample. On the

FIGURE 21: Main control FSM.

FIGURE 22: RTL schematic of ADC (part 1).

FIGURE 23: RTL schematic of ADC (part 2).

FIGURE 24: Chipscope proanalysis of internal signal of ADC.

FIGURE 25: Prototype of buck converter with FPGA based PI and PWM controller.

other side, the PI controller calculates the reference output and that value is used by the PWM module till another sample is not available to PI from ADC. Figure 19 shows the SPI signal timing diagram.

Figure 20 explains the FSM of ADC control. We have used an interacting FSM for the controller design where different

state machines are written which communicates and controls each other (see Figures 22, 23, and 24).

Figure 21 is the state machine diagram of main control which controls the entire state machine.

FIGURE 26: (a) PWM switching pulse with constant load. (b) Duty cycle change with the variation of load.

4. Prototype Model of Controller

We have developed a prototype model of DC-DC buck converter. The buck converter is designed with $L = 8 \text{ mH}$; $C = 100 \text{ }\mu\text{F}$; and load $R = 20 \text{ ohms}$. The duty cycle of the PWM signal with constant load is 50% as shown in Figure 26(a). We have tested our prototype model with resistive load only. By changing the load, current varies which changes the voltage. For constant voltage, the duty cycle of the PWM switching pulse will change accordingly. We have tested the controller performance by decreasing the load; gradually the current requirement increases. From the V-I characteristics curve of SOFC model, a decrease in the output voltage with an increase in current density is shown. So, for a constant output voltage, the duty cycle will increase gradually which is shown in Figure 26(b).

Voltage sensing is done by simple voltage dividing circuit which will be V_{dc} . This V_{dc} is subtracted from V_{dcref} using an op-amp subtractor circuit. This error signal $e(t) = V_{dcref} - V_{dc}$ is fed to the FPGA based PI + PWM controller which is synthesized in XC3S500E development board. It is given to ADC (analog-to-digital conversion) module of XC3S500E board. LTC1407A-1 ADC converter IC has been used in this board which gives 1-bit digital output represented in 2's complement binary value. It has a precision of 14 bits. Maximum sampling rate which can be achieved is approximately 1.5 MHz. Using PI modules, the error $e(t)$ is minimised and PWM output is generated with its reference and output is taken from I/O pin F8 of XC3S500E board.

Using optocoupler (HCPL817), PWM signal is interfaced with the DC-DC buck converter. The optocoupler provides isolation between the FPGA board and the power circuit (see Figure 25).

5. Conclusions

This paper proposes a comprehensive state space model for fuel cell power system that comprises fuel cell, DC-DC buck converter and load. The proposed model for the fuel cell system is validated through extensive simulation using MATLAB/SIMULINK. PI in conjunction with PWM controller scheme is proposed for DC-DC converter that guarantees

a stable and desired output voltage and this control scheme is implemented using FPGA that simplifies circuits and adds flexibility. The controller facilitates computing the pulse width and switches the MOSFET so that desired output voltage is obtained. Controller for fuel cell power system is prototyped using XC3S500E development board containing a SPARTAN 3E Xilinx FPGA. The obtained results validate the proposed model and indicate expected performance.

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