Hindawi Publishing Corporation
ISRN Electronics
Volume 2013, Article ID 376869, 8 pages
http://dx.doi.org/10.1155/2013/376869

Research Article

A High-Efficient Multi-Output Mixed Dynamic/Static Single-Bit Adder Cell

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Received 30 April 2013; Accepted 29 July 2013

Academic Editors: H. J. De Los Santos, M. Hopkinson, and H. Kim

Dynamic logic is a well-known logic style which is widely used in digital electronics. A mixed dynamic/static full adder cell is presented in this paper with the aim of reaching high efficiency. The midoutputs are obtained from a Multi-output dynamic module. Then, a multiplexer generates final outputs in the static part. Several conventional and state-of-the-art dynamic adders are also surveyed and compared in the paper. All circuits are simulated by HSPICE with 32 nm CNFET technology. The proposed design is the fastest dynamic adder cell. In addition, it has approximately 5% higher efficiency in terms of PDP than the second most high-performance cell, which is DDCVS.

1. Introduction

In today's VLSI circuit designs, the increasing demand for high-speed and low-power structures can be addressed at different design levels including design methodology and fabrication technology. From the technological view, many fundamental drawbacks of metal-oxide semiconductor (MOS) technology such as short-channel effects, high leakage power dissipation, large parametric variations, and reduced gate control make numerous challenges and difficulties for the near future generation of integrated circuits (ICs) [1]. In order to overcome the mentioned problems, some nanoscale devices such as single-electron transistor (SET) [2], quantum-dot cellular automata (QCA) [3], and carbon nanotube field effect transistor (CNFET) [4] have recently been presented in the literature to be employed in nanoscale digital electronics.

According to the Moor's law, miniaturization and optimization of transistors to the nanoranges are the most dominant obstacles of silicon-based technology. Hence, downsizing of the conventional silicon-based devices will reach its limit at the gate length of 5 nm around the year 2020 [5]. CNFET, which is one of the most promising devices among the emerging nanotechnologies, turned out to be an alternative technology to implement switches with miniaturized dimensions.

Based on comprehensive investigations on the characteristics of CNFETs, they have high superior properties such as close structural and behavioral similarities to the current CMOS devices, reusability of fabrication process, and excellent current handling capabilities with high thermal conductivity [6]. As the threshold voltage of the CNFET is proportional to the inverse of the diameter of CNT (D_{CNT}) [4], different threshold voltages can be achieved by changing the diameter of CNFETs. The relationship is shown in (1)

$$V_{\mathrm{th}} = \frac{\sqrt{3}}{3} \times \frac{aV_{\pi}}{eD_{\mathrm{CNT}}}, \tag{1}$$

where parameter a ($\approx$ 0.249 nm) is the carbon-to-carbon atom distance, V_{π} ($\approx$ 3.033 eV) is the carbon π-π bond energy in the tight bonding model, e is the unit electron charge, and D_{CNT} is the diameter of CNT. The diameter of CNT can be

calculated by the following equation [4], where n and m are chirality of CNT,

$$D_{\mathrm{CNT}} = \frac{a\sqrt{3}}{3} \times \sqrt{n^2 + m^2 + nm}. \quad (2)$$

On the other hand, depending on the application, design methodology is also very important. The utilized logic style directly influences the terms of efficiency. Delay, power consumption, and area are the main efficiency factors [7]. However, other design parameters such as robustness, driving power, and rail-to-rail operation should be definitely considered, especially when the circuit is supposed to be employed in low-voltage applications.

Design methodologies can be generally categorized as static and dynamic logics. Static logic is robust and easy to design. In spite of having high switching activity, dynamic logic has some attractive features. They are usually faster than their static counterparts. They need fewer transistors which results in less surface area. In addition, the voltage levels are generally-full swing, and they do not have any static power dissipation due to the elimination of short-circuit currents which flow in static circuits when a direct path is formed from power supply to the ground [8, 9]. However, clock distribution interconnections result in increased power in dynamic circuits [10].

Full Adder is known as a fundamental arithmetic block which is widely used in microprocessors, digital signal processors (DSPs), video and image processing units, and micro/nanoelectronic systems. It is also a basic component for all arithmetic blocks [7]. It plays an important role in the whole system efficiency, since it lies in the critical path of the system. In this paper, a novel highly efficient CNFET-based single-bit adder cell is proposed for dynamic logic. The whole cell is a Multi-Output mixed dynamic/static structure. Several dynamic full adders are also selected for comparison and a comprehensive survey of the previous works. There is also a comparison between CNFET and MOSFET technologies for the proposed design.

The rest of this paper is organized as follows. Section 2 reviews the previously presented dynamic full adders. Section 3 exhibits the proposed design. Simulation results and comparisons are presented in Section 4. CNFET and MOSFET technologies are compared for the proposed structure in Section 5. Finally, Section 6 concludes the paper.

2. Literature Review on Previously Presented Dynamic Adders

In this section, several conventional and state-of-the-art dynamic full adder cells are reviewed in detail. All adders are simulated with CNFET technology in order to make a fair technology-independent comparison and also to conduct a survey of future technology impacts on the existing logic styles. Diameters of CNTs are adjusted to 1.4877 nm for all transistors except the ones passing a non-full-swing signal. Further explanations are provided for each design. The number of nanotubes under the gate terminal (#CNTs) is also reported within the figures inside the parentheses.

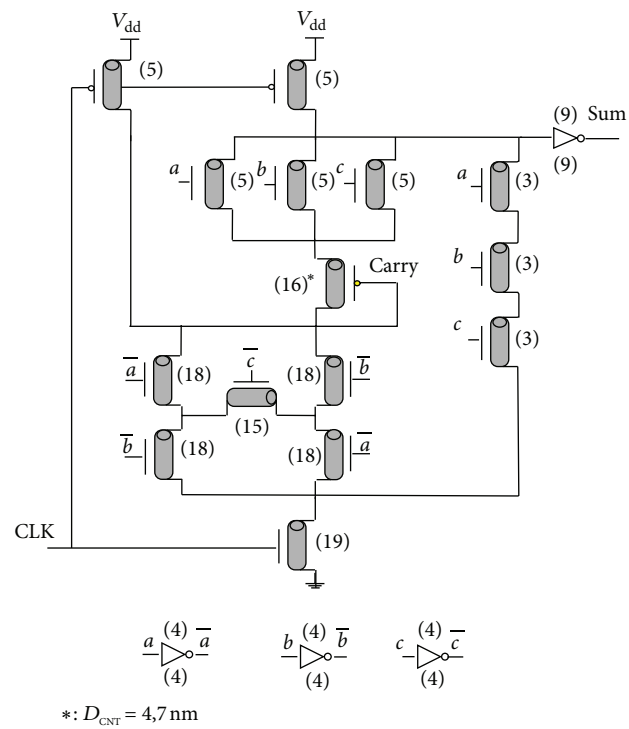

Figure 1: Multi-output bridge [11].

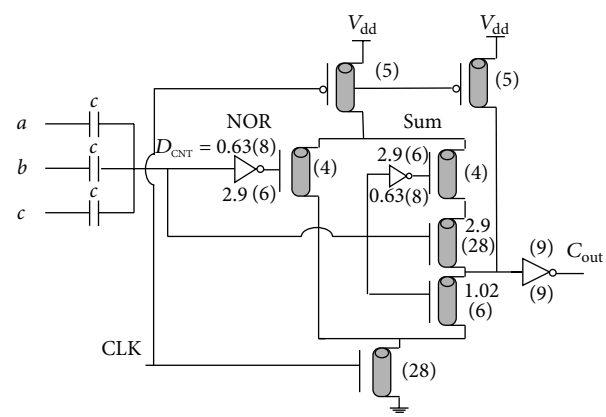

Figure 2: Multi-output CAP [12].

A bridge style Multi-Output dynamic full adder cell has been presented in [11] (Figure 1). It has 23 transistors and utilizes a bridge circuit to produce the output carry. Both outputs (C_{out} and Sum) are generated within a single pull-down network, where a p-type transistor is used. This transistor has to be sized in a way that shows minimum resistivity in order to correct its improper placement. Therefore, D_{CNT} is increased to 4.77 nm with the aim of reducing threshold voltage as well as the equivalent impedance. Any load capacitor on the output node C_{out} has to be discharged in order to link the node $\overline{\mathrm{Sum}}$ to the ground. It results in slow operation, especially in presence of high-load capacitors.

Another Multi-Output structure has been proposed in [12] (Figure 2). A capacitor network averages input variables

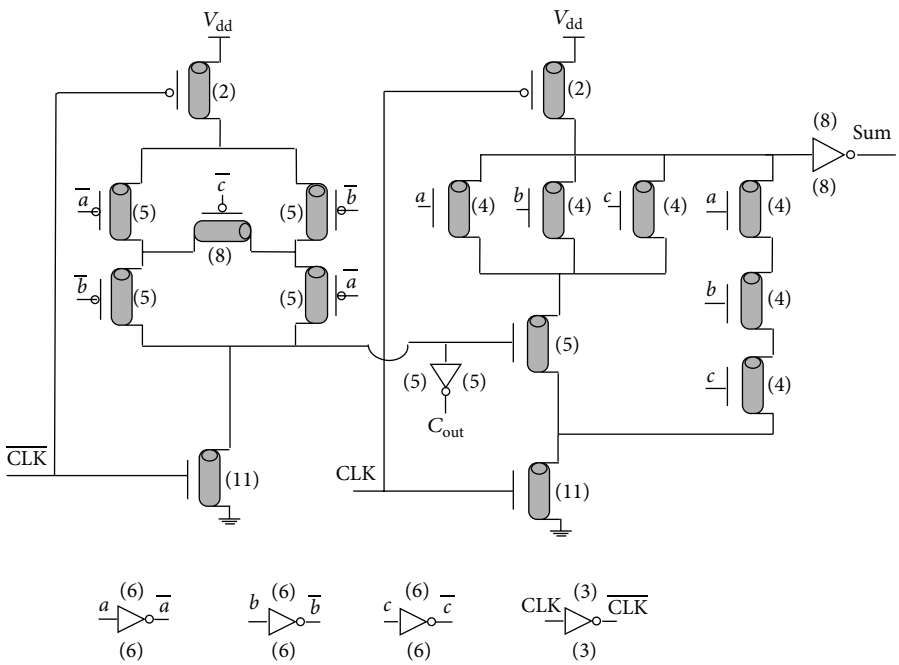

Figure 3: Zipper [11].

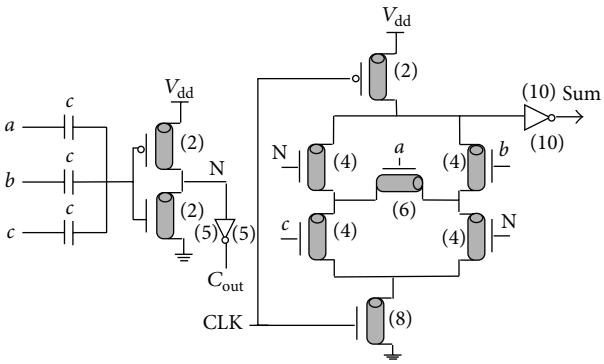

Figure 4: Majority-based [13].

out. The output carry is equal to the majority function of the input signals. Voltage transfer characteristic (VTC) curves of the intermediate inverters are shifted in a way that NAND and NOR functions are obtained. Although it has few transistors (13 transistors + 3 capacitors), it works inefficiently. This design is highly dependent on diameters to be adjusted precisely. Therefore, it is highly sensitive to process and voltage variations. Furthermore, the capacitor network generates incomplete voltage levels, which results in reduced noise margin and considerable leakage power dissipation in the following inverters.

Zipper or NP domino logic style has been employed in [11] to form a dynamic full adder cell (Figure 3). The p-block is a bridge circuit which generates the output carry. The Sum output is generated from the output carry in the second module by an n-block. The blocks do not enter the evaluation phase at the same time, because the second module is driven by the negated clock. The whole cell has 26 transistors including the inverters which are necessary to create complementary inputs. It operates efficiently and produces rail-to-rail signals. However, distribution of $\overline{\text{Clock}}$ also brings about extra power consumption in zipper circuits.

In [13], a dynamic adder cell has been proposed on the basis of majority functions (Figure 4). The first one is implemented with three capacitors. A bridge-style circuit implements the second majority function to generate the Sum. The entire cell has 13 transistors and 3 capacitors. Although it works very fast, the initial voltage division between capacitors leads to incomplete voltage levels, which results in reduced noise margin. Besides, it causes high leakage power dissipation in the following inverter, whose transistors are not turned off completely.

A dynamic differential cascode voltage switch (DDCVS) full adder has been presented in [14] (Figure 5). Two separate circuits generate the outputs Sum and C_{out} simultaneously. The inverted outputs are also produced within the circuits. It has 40 transistors, which is higher than the transistor count of the other cells. The final inverters increase the driving power and lead to high-speed operation. Weak p-type feedback transistors are used in the original circuit to enhance signal integrity. However, they slow down the switching activity by adding more capacitance to the internal nodes. They are eliminated in this paper to increase speed and reduce transistor count.

Finally, a hybrid static-dynamic adder cell has been proposed in [15] (Figure 6). An exclusive-nor (XNOR) function is implemented in the dynamic part in a non-full-swing manner. Multiplexers are utilized in the static portion to generate output signals. Instead of transmission-gates, pass-transistors are used to implement multiplexers with the aim

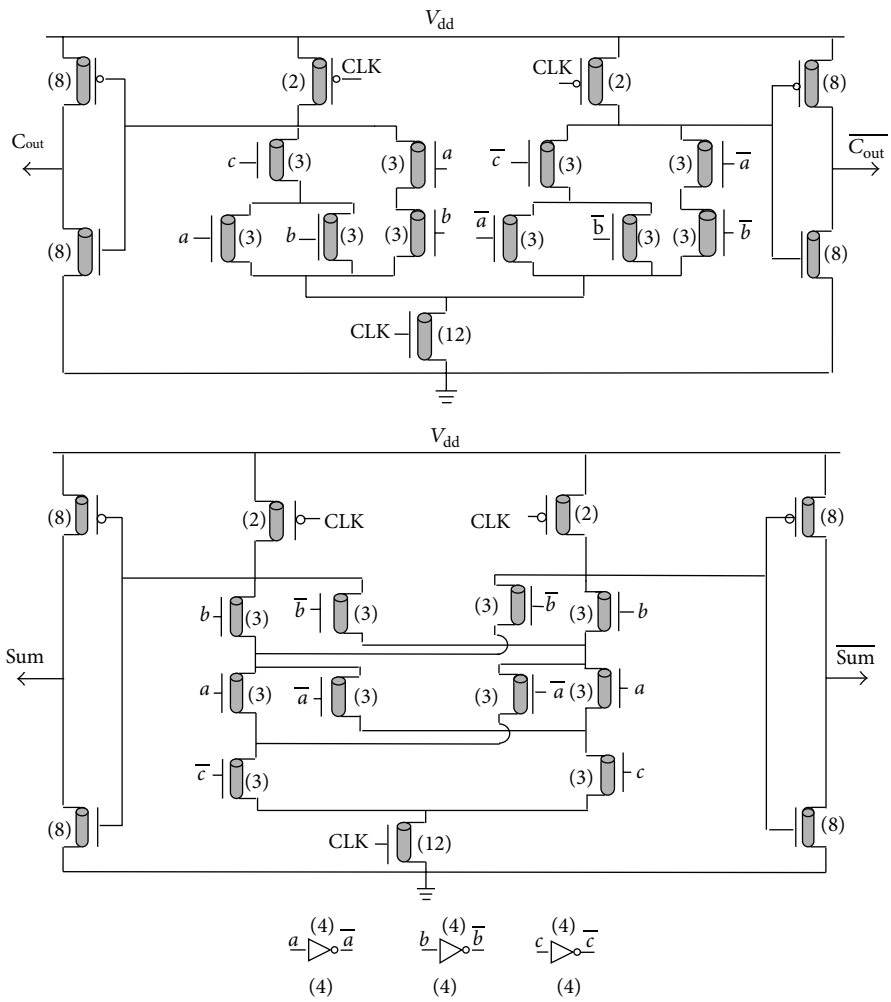

Figure 5: DDCVS [14].

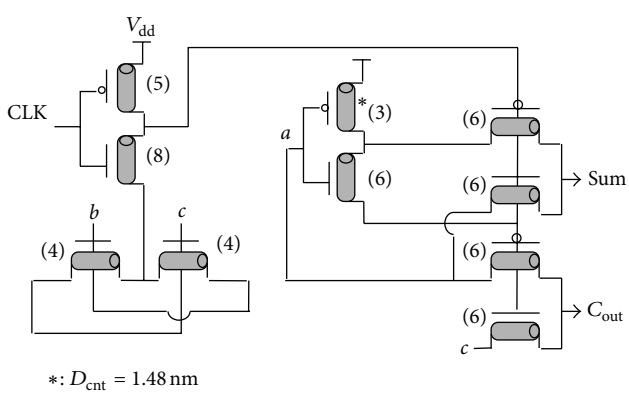

Figure 6: SD-10T [15].

of reducing the number of transistors. Even though it has very few transistors (10 transistors), it suffers from non-full-swing internal and output nodes. Reduced noise margin, low driving capability, and slow operation are the payoffs for reaching a low transistor-count design. Diameters of CNTs are increased to 3.132 nm for the transistors which do not pass the proper voltage level. However, it still does not operate in a full-swing manner when high load capacitors are applied to the output nodes.

3. The Proposed Multi-Output Mixed Dynamic/Static Full Adder

The proposed full adder (Figure 7) is a mixed dynamic/static structure. It operates on the basis of (3). In the first stage, $\overline{b+c}$, $\overline{bc}$, and $\overline{b \oplus c}$ functions are generated by a Multi-Output dynamic structure, which causes the number of transistors to be reduced. It shares the part generating $\overline{b+c}$ in order to diminish transistor count. A couple of transistors in series are added to produce $\overline{(b+c)(bc)} = \overline{bc}$. Another two transistors, which are parallel, are also added to create $\overline{(b+c)(\overline{b}+\overline{c})} = \overline{b \oplus c}$. The charge sharing problem of dynamic circuits is mostly solved by the Multi-Output approach, because almost

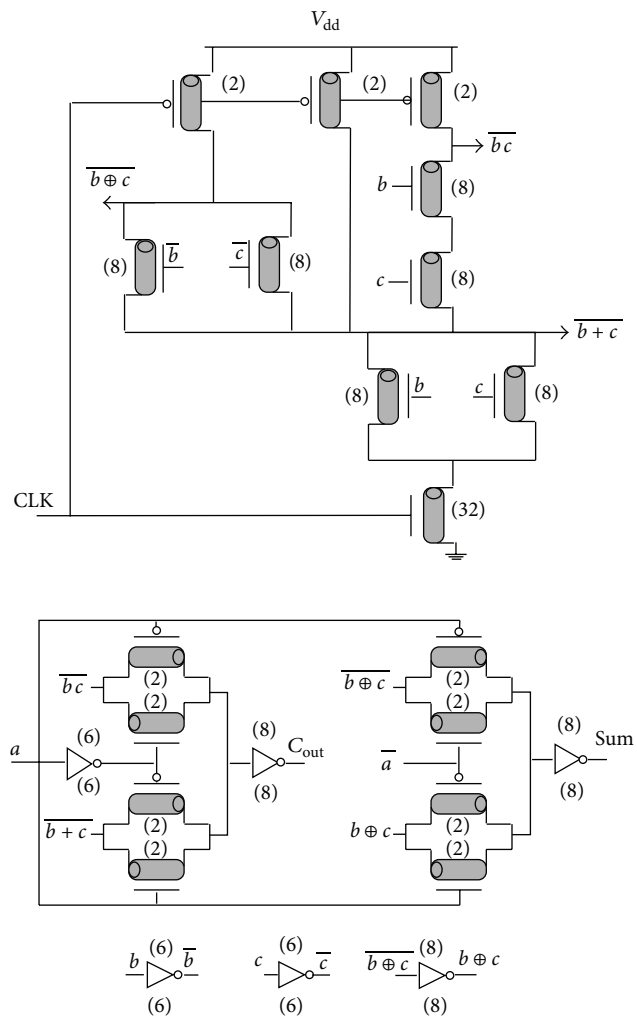

Figure 7: The proposed Multi-output mixed dynamic/static full adder.

all nodes within the pull-down network are charged at the precharge phase as follows:

$$\text{Sum} = \overline{\overline{a}\left(\overline{b \oplus c}\right) + a\left(b \oplus c\right)},$$
$$C_{\text{out}} = \overline{\overline{a}\left(\overline{bc}\right) + a\left(\overline{b+c}\right)}. \tag{3}$$

Two multiplexers are utilized in the second stage to generate the final outputs (Sum and C_{out}). The first operand (A) is chosen as the selector of the multiplexers. It selects between $\overline{bc}$ and $\overline{b+c}$ to generate $\overline{C_{\text{out}}}$. It also makes a simultaneous selection between $\overline{b \oplus c}$ and $b \oplus c$ to achieve $\overline{\text{Sum}}$ in the second multiplexer. Transmission-gates are employed to implement the final multiplexers in order to reach a robust structure. Thus, it will be applicable for low-voltage applications. An inverter negates the exclusive-nor (XNOR), provided from the first stage, to achieve the exclusive-or (XOR) function.

In the proposed design, the clock (CLK) signal is only applied to the first stage of the circuit. The outputs of this stage are connected to a limited number of nodes. Hence, the high number of fan-outs does not cause any voltage drops to the output signals of the first stage, although they are not connected to the power supply in the evaluation phase. The second stage, which generates the final outputs, is a static structure. It benefits from the high driving capability. The proposed design is a mixed dynamic/static structure, and hence it benefits from the best of the two worlds. The entire circuit has 30 transistors. Diameters of all CNTs are 1.4877 nm. A single-threshold circuit shows higher reliability and robustness in the presence of device parameter variations. Eventually, rail-to-rail operation is achieved for both internal and output nodes which are important factors especially in low voltages. The waveforms of input and output signals are illustrated in Figure 8, when input and output buffers are used.

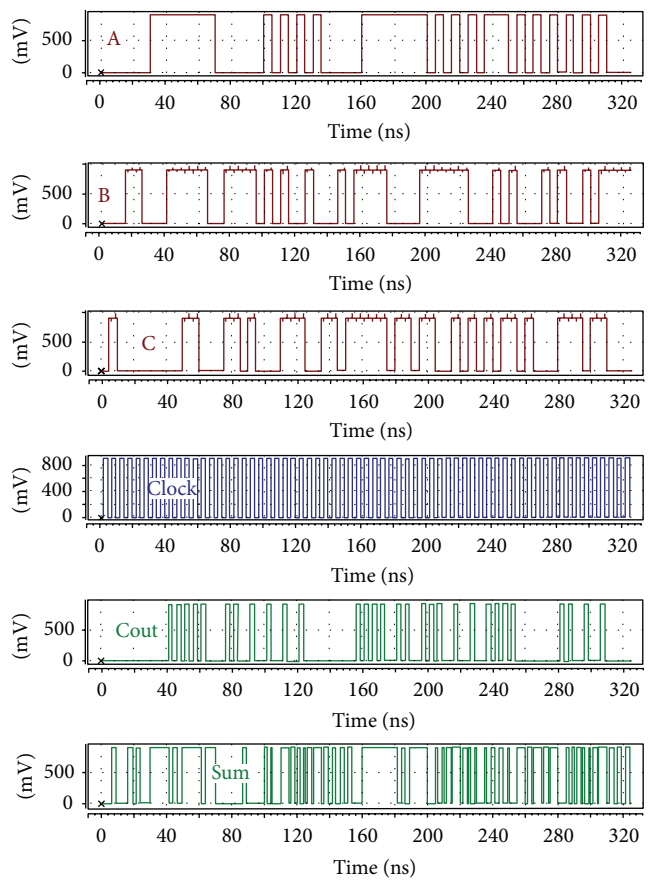

Figure 8: Waveforms of input and output signals.

4. Simulation Results and Comparisons

The proposed design and all the six previously presented dynamic structures, which were mentioned in Section 2, are simulated by using Synopsys HSPICE 2008 and 32 nm CNFET Compact SPICE Model [16]. Simulations are performed in 0.9 V power supply at room temperature after performing transistor sizing with the aim of reaching the lowest power-delay product (PDP). Input buffers and 2 fF

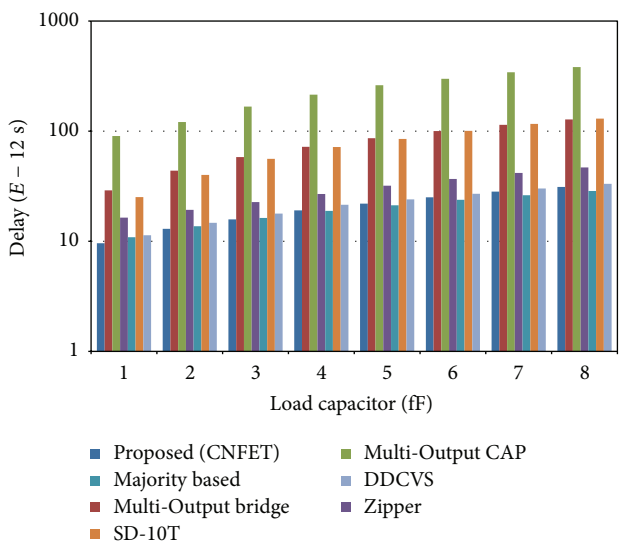

Figure 9: Delay versus load capacitors.

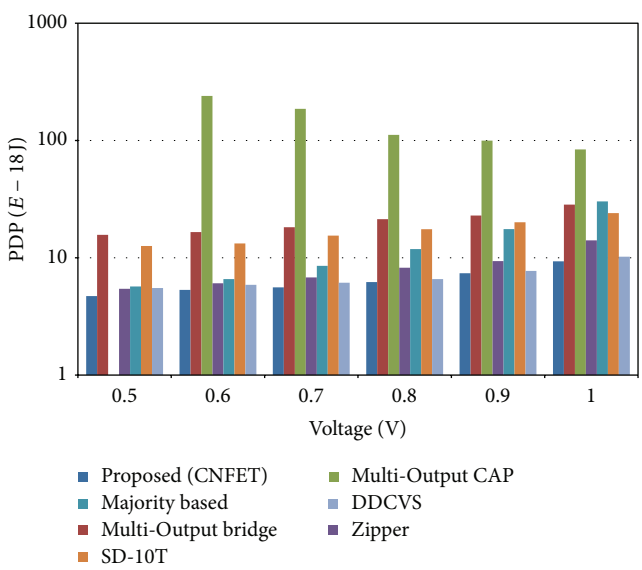

Figure 10: PDP versus voltage variations.

load capacitors are utilized to provide a realistic test-bed. The complete input pattern (Figure 8) is fed to the circuits with clock frequency of 200 MHz. It reveals the maximum delay by checking 56 different transitions of input variables. The simulation results, shown in Table 1, demonstrate the superiority of the proposed design in terms of PDP.

Toexaminedriving capability, simulations are repeated while applying different load capacitors ranged from 1 fF to 8 fF. All circuits are also simulated in a vast range of power supply voltages (1 V down to 0.5 V). The Multi-Output CAP circuit fails to operate at 0.5 V power supply. In addition, to test the immunity to temperature variations, simulations are repeated in different ambient temperatures, ranged from 0°C up to 80°C. The results of these three experiments are shown in Figures 9, 10, and 11, respectively. The proposed design

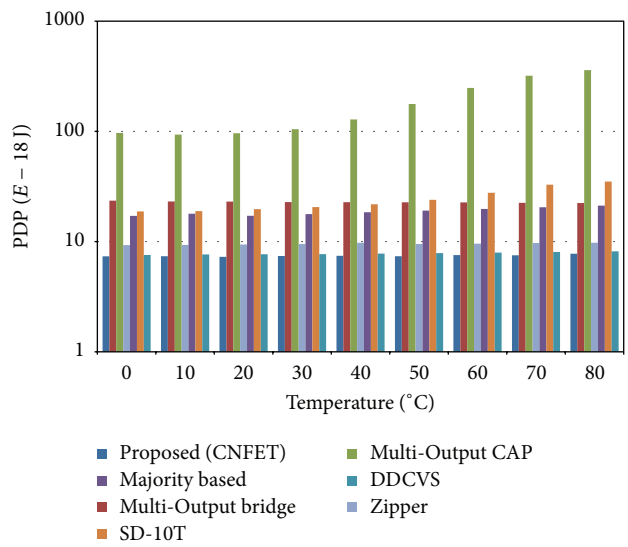

Figure 11: PDP versus ambient temperature variations.

Table 1: Simulation results at 0.9 V power supply and 200 MHz clock frequency.

Design	Delay (psec)	Power (μW)	PDP (aJ)
Proposed	12.980	0.56878	7.3827
Multi-output Bridge	43.767	0.52364	22.918
Multi-output CAP	121.02	0.82386	99.706
Zipper	19.289	0.48637	9.7060
Majority-based	13.695	1.28330	17.574
SD-10T	40.052	0.50209	20.109
DDCVS	14.724	0.52492	7.7289

surpasses other structures in charging and discharging high-load capacitors. It also operates reliably in spite of voltage and temperature variations.

Finally, to evaluate the functionality and performance of the adder cells in high-operative frequency, all circuits are tested at 2 GHz clock frequency. The simulation results are depicted in Table 2. It can be inferred from the results that the proposed design properly works in high frequencies. It is almost as efficient as the DDCVS structure, while it has 10 fewer transistors.

5. CNFET versus MOSFET

CNFET is considered as a promising candidate for future nanoscale transistor devices, which will be applicable in nanoelectronics applications. The growing trend is towards fabricating CNFETs due to serious problems of current silicon-based transistors in nanoscale regime. In addition, CNFETs are highly advantageous in terms of efficiency. In order to evaluate the potential benefits of this new technology, performance estimation for replacing MOSFETs by CNFETs

Table 2: Simulation results at 0.9 V power supply and 2 GHz clock frequency.

Design	Delay (psec)	Power (μW)	PDP (aJ)
Proposed	15.337	5.7311	87.897
Multi-output Bridge	43.961	5.2829	232.24
Multi-output CAP	130.18	7.2148	939.23
Zipper	19.705	4.9108	96.766
Majority-based	15.126	6.5500	99.078
SD-10T	36.835	4.2811	157.69
DDCVS	16.007	5.1890	83.061

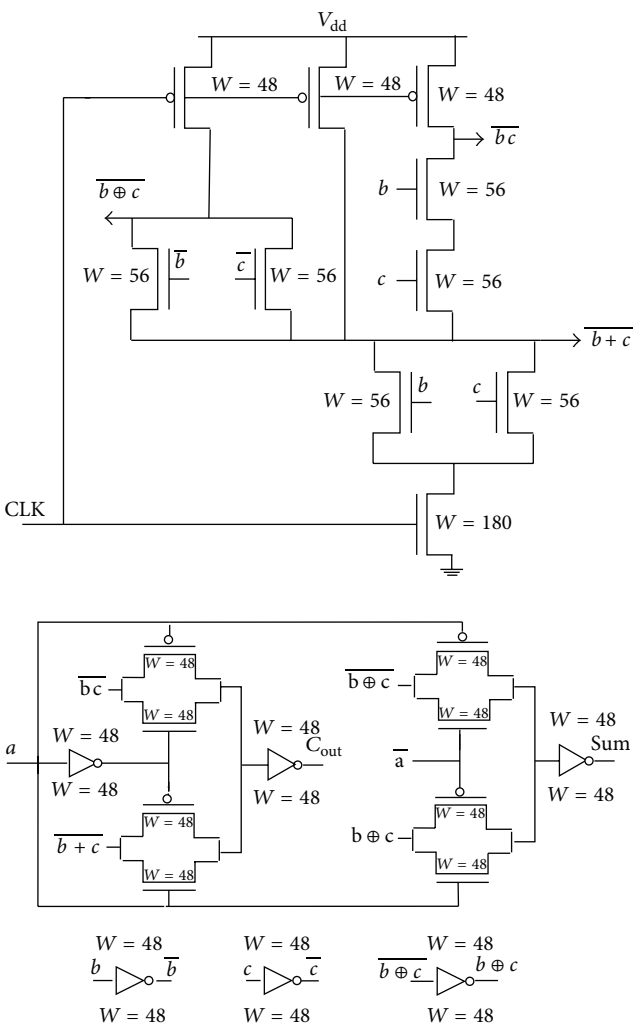

Figure 12: The proposed design (MOSFET technology).

is made at transistor level for the proposed structure. It is also simulated with 32 nm feature size (MOS technology) at 0.9 V power supply. Transistors are sized appropriately to minimize the PDP metric using the algorithm presented in [17] (Figure 12). The same test-bed described in Section 4 is also applied here. Simulation results are shown in Table 3. As it was expected, the CNFET-based circuit operates far more efficiently. It operates about 82% faster, and it consumes 2.974 μW less power, which results in 88% lower PDP.

Table 3: Simulation results for the proposed design (CNFET versus MOSFET technologies).

Design	Delay (psec)	Power (μW)	PDP (aJ)
CNFET	12.980	5.6878	7.3827
MOSFET	72.924	8.6618	63.166

6. Conclusion

A new Multi-Output mixed dynamic/static full adder cell has been proposed in this paper. Several simulations have been carried out to investigate efficiency in different aspects. Simulation results demonstrated the superiority of the given structure in terms of speed and PDP. It charges and discharges high-load capacitors rapidly with sufficient driving power. It also operates reliably and efficiently in high frequencies and in a vast range of voltage and temperature variations. Eventually, terms of efficiency have been compared between MOSFET and CNFET technologies. The latter brings higher performance.

Several conventional and state-of-the-art dynamic full adders have been also reviewed. All of them were simulated with the CNFET technology. Based on our investigations, DDCVS has the best performance. The zipper structure is also very efficient. Both designs generate rail-to-rail signals which are very important in low voltages in terms of noise tolerance and circuit robustness. The majority-based full adder is the fastest one. However, it consumes considerable power which is not desirable for low-power applications. Other full adder cells are not entirely suitable for low-voltage applications due to their reduced noise margins, inefficiency, and inadequate driving power.

References

[1] S. Lin, Y.-B. Kim, and F. Lombardi, "A novel CNTFET-based ternary logic gate design," in *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS '09)*, pp. 435–438, Cancun, Mexico, August 2009.

[2] A. K. A. El-Seoud, M. El-Banna, and M. A. Hakim, "On modelling and characterization of single electron transistor," *International Journal of Electronics*, vol. 94, no. 6, pp. 573–585, 2007.

[3] K. Navi, R. Farazkish, S. Sayedsalehi, and M. Rahimi Azghadi, "A new quantum-dot cellular automata full-adder," *Microelectronics Journal*, vol. 41, no. 12, pp. 820–826, 2010.

[4] M. Moradi, R. Faghih Mirzaee, M. H. Moaiyeri, and K. Navi, "An applicable high-efficient CNTFET-based full adder cell for practical environments," in *Proceedings of the 16th CSI International Symposium on Computer Architecture and Digital Systems (CADS '12)*, pp. 7–12, May 2012.

[5] H. Iwai, "CMOS technology after reaching the scale limit," in *Proceedings of the International Workshop on Junction Technology (IWJT '08)*, pp. 1–2, Shanghai, China, May 2008.

[6] H. Hashempour and F. Lombardi, "Circuit-level modeling and detection of metallic carbon nanotube defects in carbon

nanotube FETs," in *Proceedings of the Design, Automation and Test in Europe Conference and Exhibition*, pp. 841–846, April 2007.

[7] K. Navi, R. F. Mirzaee, M. H. Moaiyeri, B. M. Nezhad, O. Hashemipour, and K. Shams, "Ultra high speed full adders," *Electronics Express*, vol. 5, no. 18, pp. 744–749, 2008.

[8] A. Marshall and S. Natarajan, *SOI Design: Analog, Memory and Digital Techniques*, Springer, 2002.

[9] D. Soudris, C. Piguet, and C. Goutis, *Designing CMOS Circuits for Low Power*, Kluwer Academic Publishers, 2002.

[10] F. H. A. Asgari and M. Sachdev, "A low-power reduced swing global clocking methodology," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 12, no. 5, pp. 538–545, 2004.

[11] R. Faghih Mirzaee, M. H. Moaiyeri, and K. Navi, "High speed NP-CMOS and multi-output dynamic full adder cells," *International Journal of Electrical and Electronics Engineering*, vol. 4, no. 4, pp. 304–310, 2010.

[12] M. Bagherizadeh and M. Eshghi, "Two novel low-power and high-speed dynamic carbon nanotube full-adder cells," *Nanoscale Research Letters*, vol. 6, article 519, pp. 1–7, 2011.

[13] S. Wairya, G. Singh, V. Vishant, R. K. Nagaria, and S. Tiwari, "Performance analysis of high speed hybrid CMOS full adder circuits for low voltage VLSI design," *VLSI Design*, vol. 2012, Article ID 173079, 18 pages, 2012.

[14] L. Heller, W. Griffin, J. Davis, and N. Thoma, "Cascode voltage switch logic: a differential CMOS logic family," in *Proceedings of IEEE International Solid-State Circuits Conference*, pp. 16–17, 1984.

[15] M. H. Ghadiry, M. S. Nadi, and M. Sheilkhpour, "Static-dynamic full adder cell based on a new logic approach," *Australian Journal of Basic and Applied Sciences*, vol. 5, no. 8, pp. 221–223, 2011.

[16] J. Deng, *Device modeling and circuit performance evaluation for nanoscale devices: silicon technology beyond 45nm node and carbon nanotube field effect transistors [Ph.D. thesis]*, Stanford University, 2007.

[17] C.-H. Chang, J. Gu, and M. Zhang, "A review of 0.18-μm full adder performances for tree structured arithmetic circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 13, no. 6, pp. 686–694, 2005.