Research Article

Selection of Design Parameters to Reduce the Zero-Sequence Circulating Current Flow in Parallel Operation of DC Linked Multiple Shunt APF Units

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Capacity enhancement and operational flexibility are two of the important limitations of the centralized shunt APF (APF_{sh}) unit. These limitations can be conquered by the operation of multiple APF units in parallel and connected back to back by a common DC link capacitor. In that case, a circulating current (CC) flows within the APF_{sh} units. This CC flow becomes out of control when the APF_{sh} units operate in hysteresis based current controlled mode. One of the difficulties of this CC flow control or reduction is the variable switching frequency of the APF_{sh} units. In this paper, the model for CC flow is derived by the switching dynamics study of the APF_{sh} units. It is found that the selection of design parameters plays an important role in the amount of CC flow. Detailed simulation, analysis, and real-time performance show how the selection of design parameters affects the CC flow and the reduction of CC flow can also be achieved at an acceptable level by the proper selection of design parameters.

1. Introduction

The power quality, at all time, is a matter of concern where a number of nonlinear, harmonics producing, and sophisticated loads are connected in an electrical distribution network. In that case, for power quality (PQ) improvement, shunt active power filters (APF_{sh}) are finding greater applications as interfacing and compensating devices in the distributed network. The power rating and switching frequency of the APF_{sh} converters are determined by the magnitude of harmonic currents and required filter bandwidth. In high power applications, the filtering task cannot be performed for the whole spectrum of harmonics by using a single converter due to the limitations on switching frequency and power rating of the semiconductor devices. Therefore, compensating the reactive harmonic components to improve the power quality of the distributed network as well as to avoid the large capacity centralised APF_{sh} , parallel operation of multiple low power APF_{sh} units is increasing. Different controlling mechanisms and topologies are available in handling the difficulties of parallel operation of APF_{sh} either in active

load sharing or distributed mode. Although the harmonic current compensation is the primary function of parallel APF, it can also be used as a compensator for voltage harmonics. A detailed technical review on parallel operation of APF_{sh} for current and voltage harmonic compensation in a distributed generation (DG) network has been done in [1, 2] where the pros and cons of the different control methods have been discussed. For these cases, there is no physical/electrical link between the APF_{sh} units. Another kind of configuration is also available where the system components and cost are reduced by maintaining a common DC link back-to-back connection between the APF_{sh} units [3]. But it then raises the control complexity by introducing the zero-sequence circulating current (ZSCC) flow within the APF_{sh} units which can overload the inverters of the APF units and thus increases the power losses. Other problems associated with the ZSCC flow is that it can reduce the ampacity (capacity of carrying current) of the cable, it can increase the DC link voltage, and it is harmful for the DG system like DFIG application [4–8].

The control methods for the reduction of ZSCC discussed in the literature are mainly for PWM based control system.

FIGURE 1: (a) Single line diagram of a 3ph 2 units APF_{sh} and (b) VSI switching with common DC link presenting $i_{cc} = \text{ZSCC flow}$.

In most of the cases, the methods are discussed for the parallel operation of inverter or rectifier [6–10]. Very few of the articles show the ZSCC reduction for the parallel operation of APF_{sh} units [11]. None of these discuss the ZSCC flow issues and control method for the parallel operation of converter/APF_{sh} based on hysteresis control. Therefore, an attempt has been made here to discuss the issues related to hysteresis control.

2. Working Principle

According to the working principle of an APF_{sh} unit in parallel to the load to compensate the reactive and harmonic current, there are two possible modes of operation: capacitive mode (where the current flows from the capacitor) and inductive mode (the current flows towards the capacitor). When multiple APF units work in a current sharing mode, there could be four possible modes of operation: (i) capacitive-capacitive, (ii) inductive-inductive, (iii) capacitive-inductive, and (iv) inductive-capacitive. As an example, Figure 1(a) shows a single line diagram of a 3-phase system, where i_{cc} represents the circulating current flow between the APF units. In the case of a 3-phase system, shown in Figure 1(b), this circulating current flow exists as a zero-sequence harmonics in the zero-sequence current flow when a circulating loop is created within the APF_{sh} units and hence it is termed zero-sequence circulating current (ZSCC) flow. In general these harmonics are $(3 + n * 6)$ order, where $n = 0, 1, 2, \dots$

3. Model for ZSCC Flow

For simplicity, derivation of ZSCC flow has been carried out on a per phase basis. Figure 2 shows the possible mode of

operation between the APF units (1 phase), where sh- i and sh- c represent the corresponding inductive and capacitive mode, respectively. If there is a difference in any of the parameters, such as switching frequency, current sharing, interfacing inductor, and hysteresis band (in case of hysteresis current controller), then the APF_{sh} units can operate in inductive-capacitive or capacitive-inductive mode. In these cases, ZSCC will flow and these are reflected in Figures 2(f) and 2(h).

From Figures 2(a) and 2(b), during the capacitive mode, the current flow can be obtained as

$$\frac{di_{sh-c}}{dt} = \frac{v_{sh-c} - v_{pcc}}{L_{sh1} \parallel L_{sh2}}, \quad (1)$$

while $v_{sh-c1} = \delta_1 v_{dc} = v_{sh-c2} = (1 - \delta_2) v_{dc} = v_{sh-c}$; here δ is the duty cycle; that is, the AC voltages of the APF_{sh} units are equal.

Similarly, Figures 2(c) and 2(d) show that when both the APF units work in inductive mode during its switching cycle, the resulting current flows can be found as

$$\frac{di_{sh-i}}{dt} = -\frac{v_{sh-i} + v_{pcc}}{L_{sh1} \parallel L_{sh2}}, \quad (2)$$

while $v_{sh-i1} = (1 - \delta_1) v_{dc} = v_{sh-i2} = \delta_2 v_{dc} = v_{sh-i}$.

From Figures 2(e) and 2(f), the circulating current flow in capacitive-inductive mode can be obtained as

$$\frac{di_{cc-c}}{dt} = \frac{v_{cc-c}}{L_{sh1} + L_{sh2}} = \frac{v_{sh-c1} - v_{sh-i2}}{L_{sh1} + L_{sh2}} = \frac{(\delta_1 - \delta_2) v_{dc}}{L_{sh1} + L_{sh2}}, \quad (3)$$

while $v_{sh-c1} > v_{sh-i2}$.

FIGURE 2: Possible mode of operation between two APF units to calculate circulating current.

Similarly, the circulating current flow for inductive-capacitive mode is

$$\frac{di_{cc-i}}{dt} = \frac{v_{cc-i}}{L_{sh1} + L_{sh2}} = \frac{v_{sh-i1} - v_{sh-c2}}{L_{sh1} + L_{sh2}} = -\frac{(\delta_1 - \delta_2)v_{dc}}{L_{sh1} + L_{sh2}}, \quad (4)$$

while $v_{sh-i1} > v_{sh-c2}$.

Therefore, in general, the equation for the ZSCC flow can be written as

$$\frac{di_{cc}}{dt} = \frac{\delta_{cc}v_{dc}}{L_{sh1} + L_{sh2}}, \quad (5)$$

where $\delta_{cc} = \delta_1 - \delta_2$ for capacitive mode and $\delta_{cc} = \delta_2 - \delta_1$ for inductive mode.

FIGURE 3: Continued.

FIGURE 3: Performance of APF_{sh} for the cases A1–A5 and the corresponding CC flow.

The possible maximum value for CC flow ($I_{cc-max} < V_{dc}/(L_{sh1} + L_{sh2})$) in one leg can be obtained as

$$I_{cc-max} = \frac{(S_{11ON} \sim S_{12ON}) \cdot V_{dc}}{(L_{sha1} + L_{sha2})} = \frac{\Delta t \cdot V_{dc}}{(L_{sha1} + L_{sha2})}, \quad (6)$$

where S , S_{11ON} , and S_{12ON} are the switch and switching time, as shown in Figure 1, respectively. The possible value of Δt can be obtained as $\Delta t = k \cdot T_{sw}$. Here, $k = 0, \dots, 1$ and T_{sw} is the time period.

For 3-phase system, the ZSCC can be found as

$$ZSCC = i_{sh1-zs} \sim i_{sh2-zs}, \quad (7)$$

where i_{sh1-zs} and i_{sh2-zs} are the zero-sequence components of the APF_{sh} units.

This is also confirmed in [11] for APF_{sh} topology analysis based on a parallel interleaved inverter. It is also similar to the rectifier analysis in [6]. In most of the research articles, derivation or ZSCC cancellation has been carried out for two inverters or APF_{sh} units [7–11]. Moreover, the control methods discussed in the literature are mainly for PWM based control system. None of them discuss the CC flow issues for the parallel operation of APFs based on hysteresis control. Therefore, an attempt has been made here to discuss the issues related to hysteresis control.

4. Control Issues for the ZSCC Flow

There are mainly two ways to eliminate or reduce the ZSCC flow: (i) breaking the route of CC flow by introducing physical

FIGURE 4: Continued.

FIGURE 4: Performance of APF_{sh} for the cases B1–B5 and the corresponding CC flow.

devices such as an isolation transformer or common mode inductor or (ii) by proper control methods. From the derivation of ZSCC flow it is found that the CC value depends on the duty cycle (δ) or switching frequency (f_{sw}), DC link voltage (V_{dc}), and the interfacing inductor (L_{sh}) of the APF units. Therefore, before selecting the control method for multiple APF_{sh} units with a common Dc link, some design consideration should be made to reduce the CC flow. The design options that can be implemented to reduce the CC flow are as follows.

- (i) Decrease the V_{dc} . According to the design criteria of single/3-phase APF_{sh} system there is a minimum value of V_{dc} that has to be maintained to compensate the reactive and harmonic current.
- (ii) As the $\delta = \tau/T = \tau f_{sw}$, reducing the f_{sw} and decreasing the difference between the f_{sw} or δ will reduce CC flow.
- (iii) Reduced f_{sw} will further increase the L_{sh} (in the case of hysteresis current control) and it will then in turn reduce the circulating current flow. But increased L_{sh} will reduce the VAR rating of APF_{sh}.

It is also clear from the derivation that the CC flow does not directly depend on the compensating current rating of the APF_{sh} units. Therefore, once the current or VAR rating of APF_{sh} is fixed, the design components (f_{sw} and L_{sh}) should be chosen in such a way so that the L_{sh} is possibly high and the f_{sw} difference between the APF_{sh} units is as low as possible. In that case, introducing the common mode inductor in the APF_{sh} units can be a better choice. Implementation of a CC

FIGURE 5: CC flow for the cases C and D.

FIGURE 6: ZSCC comparison between the cases (a) A3, A4, and A5 and cases (b) A6, A7, and A8.

control method in the APF_{sh} control strategy will further reduce the CC flow. But it will then increase the control complexity.

5. Selection of Control Method for APF_{sh} Units

With the control issues of the CC flow in mind, selection of a control strategy for the APF_{sh} units should be made. Different control strategies for parallel operation of multiple APF units were reviewed [1, 2]. In general, control can be based on active current sharing where the compensating power/current can be divided equally or up to the compensating capacity of the APF units. Another prominent control is droop control where information exchange between the APF units is required.

For simplicity, a current sharing (power splitting) method based on hysteresis current control has been chosen for the remainder of the analysis. The control of switches mainly depends on the control method for the APF units. In the case of the current sharing method, the switching can be determined by current sharing (equally distributed) or a capacity limitation technique. As an example, if I_{sh} , I_{sh-ref} , $I_{APFsh-rated}$, and I_{sw-ref} are the Rms values of APF compensating current, reference compensating current, rated current, and the switching reference current for ON/OFF condition, then

$$I_{sh} \leq I_{sw-ref} \text{ for the current sharing technique where } I_{sw-ref} = I_{sh-ref}/N \text{ and}$$

$$I_{sh} \leq I_{APFsh-rated} \text{ for the capacity limitation technique.}$$

FIGURE 7: FFT analysis of the ZSCC for the cases (a) A6, (b) A7, and (c) A8.

6. Simulation Study

In-depth information on parallel operation of multiple APF_{sh} based on hysteresis current controller is not available yet, especially in the case of ZSCC flow. Therefore, in the present work, the objective is to reduce the ZSCC flow based on the design parameter selection. Two units of APF_{sh} have been modelled here to operate in power sharing mode. In terms of sharing the following proportions have been chosen:

- (A) $I_{APFsh1} = I_{APFsh2} = 0.5 * I_{lqh-max}$ and $I_{lqh-max} = 100$ A; each APF_{sh} compensates half of the load reactive and harmonic components,
- (B) $I_{APFsh1} = 0.75 * I_{lqh-max}$; $I_{APFsh2} = 0.25 * I_{lqh-max}$ and $I_{lqh-max} = 100$ A,
- (C) $I_{APFsh1} = 0.6 * I_{lqh-max}$; $I_{APFsh2} = 0.4 * I_{lqh-max}$; and $I_{lqh-max} = 100$ A,
- (D) $I_{APFsh1} = 0.6 * I_{lqh-max}$; $I_{APFsh2} = 0.4 * I_{lqh-max}$; and $I_{lqh-max} = 200$ A.

In the case of a hysteresis current control based APF_{sh} , according to the selection of design parameters for APF_{sh} , described in [12–14] and the control issues of CC flow, the CC flow can be reduced by the proper selection of the design components including f_{sw} , L_{sh} , h , and V_{dc} . As the V_{dc} is fixed, variation of other components has been made here to analyze the reduction of CC flow. Results and discussion are given below.

TABLE 1: A: $I_{APFsh1} = I_{APFsh2} = 0.5 * I_{lqh-max}$ and $I_{lqh-max} = 100$ A.

Frequency (kHz)	Cases	L_{sh1}/L_{sh2} (mH)	$h1/h2$ (A)	THD@ I_{pcc} (%)
$f_{sw1} = 17.3$	A1	0.625/0.625	5/5	2.57
$f_{sw2} = 17.3$	A2	1.25/1.25	2.5/2.5	2.02
	A3	1.25/0.625	2.5/5	1.74
$f_{sw1} = 17.3$	A4	1.25/1.25	2.5/3.75	1.67
$f_{sw2} = 11.6$	A5	1.25/1.875	2.5/2.5	2.35
	A6	1.67/0.625	2.5/5	2.88
$f_{sw1} = 13.0$	A7	1.67/1.25	2.5/3.75	2.82
$f_{sw2} = 11.6$	A8	1.67/1.875	2.5/2.5	3.76

Table 1 shows the parameters that have been considered for the proportion (A), as mentioned above. Corresponding results have been given in Figure 3 and discussed below.

Figure 3 shows the performance study of the two APF_{sh} units in power sharing mode for the cases A1a–A5a where each of the units compensates half of the load reactive and harmonic components. APF_{sh1} starts working at the beginning, whereas APF_{sh2} starts at 0.5 sec. As there is no ZSCC that occurs before 0.5 sec, therefore the ZSCC waveforms for the corresponding simulations have been shown in A1b–A5b from 0.55 sec to 0.75 sec. For the cases A1–A3, the switching frequency of both units was equal and the variations have been made for L_{sh} and h . Cases A1 and A2 show that the possible CC flow can be zero when $L_{sh1} = L_{sh2}$ and $h1 = h2$; that

FIGURE 8: Real-time simulation structure in SIL configuration with hardware synchronization mode.

TABLE 2: B: $I_{APF_{sh1}} = 0.75 * I_{lqh-max}$; $I_{APF_{sh2}} = 0.25 * I_{lqh-max}$; and $I_{lqh-max} = 100$ A.

Frequency (kHz)	Cases	L_{sh1}/L_{sh2} (mH)	$H1/h2$ (A)	THD@ I_{pcc} (%)
$f_{sw1} = 17.3$	B1	0.835/2.5	3.75/1.25	1.74
$f_{sw2} = 17.3$	B2	0.418/1.25	7.5/2.5	1.81
	B3	0.835/1.25	3.75/2.5	2.25
$f_{sw1} = 17.3$	B4	0.835/1.87	3.75/2.5	2.25
$f_{sw2} = 11.6$	B5	0.835/3.74	3.75/1.25	2.33

is, both the APF_{sh} units are identical. Although the rating and f_{sw} of each unit are the same, ZSCC can flow as shown in case A3. This happens due to the difference in design parameters L_{sh} and h . Cases A4, and A5 show the results for different f_{sw} , L_{sh} , and h . For both the cases, ZSCC flows. In a comparison with A3, A4 and A5, A5 shows better results in the reduction of ZSCC flow. It is due to the higher values of L_{sh} and lower values of h , though the parameter f_{sw} is different.

Table 2 shows the parameters that have been considered for the proportion (B). Corresponding results have been given in Figure 4 and discussed below.

Figure 4 shows that, for all the cases, ZSCC flows. Even though the f_{sw} values are different, the reduced ZSCC flow occurs in the case of B5 where the values for L_{sh} are high and h are low compared to other cases. The worst case occurs for B2 where L_{sh} is low and h is high.

Tables 3 and 4 show the parameters for the cases C and D where the sharing proportion is different than that for A and B. For both the cases, values of L_{sh} are kept low, whereas the values for h are high. In both cases, f_{sw} are equal. And

TABLE 3: C: $I_{APF_{sh1}} = 0.6 * I_{lqh-max}$; $I_{APF_{sh2}} = 0.4 * I_{lqh-max}$; and $I_{lqh-max} = 100$ A.

Frequency (kHz)	Cases	L_{sh1}/L_{sh2} (mH)	$H1/h2$ (A)	THD@ I_{pcc} (%)
$f_{sw1} = 17.3$	C1	0.625/0.625	5/5	2.65
$f_{sw2} = 17.3$				

TABLE 4: D: $I_{APF_{sh1}} = 0.6 * I_{lqh-max}$; $I_{APF_{sh2}} = 0.4 * I_{lqh-max}$; and $I_{lqh-max} = 200$ A.

Frequency (kHz)	Cases	L_{sh1}/L_{sh2} (mH)	$H1/h2$ (A)	THD@ I_{pcc} (%)
$f_{sw1} = 17.3$	D1	0.625/0.625	5/5	2.12
$f_{sw2} = 17.3$				

the same components have been chosen for D where the compensating current is two times higher than that of case C.

Figure 5 shows the performances for the cases C and D in terms of ZSCC flow. In both cases, ZSCC flow is the same even though for case D, APF_{sh} units are compensating higher current than that of C. These results indicate that the ZSCC flow does not depend on the amount of compensating current. These ZSCC flows are higher than that of A and B and this is due to the lower values of L_{sh} .

Finally, a comparison has been made for the ZSCC between the A3–A5 and A6–A8 cases for one cycle, as shown in Figure 6. For A3, f_{sw} is the same for both of the APF_{sh} units, whereas for A4 and A5 it is different. But the values of L_{sh} are comparatively higher for A5. Therefore, within A3 to A5,

FIGURE 9: Performance of APF_{sh} units for the cases (a) A6, (b) A7, and (c) A8.

the ZSCC flow is comparatively lower in the case of A5, as shown in Figure 6(a).

For the cases A6–A8, the switching frequency (f_{sw1}) of APF_{sh1} is reduced and therefore the value of L_{sh} increases, as shown in Table 1. At the same time, the switching frequency difference between the APF_{sh} units is also reduced. The performance of the APF_{sh} units in terms of ZSCC flow for these cases is reflected in Figure 6(b). This shows that ZSCC flow can further be reduced by reducing the f_{sw} (to increase the value of L_{sh}) and the difference between the f_{sw} of the APF_{sh} units. The reduction of zero-sequence harmonics content for the cases A6–A8 is also shown in Figure 7, where it shows that the magnitude of zero-sequence harmonics components in the compensating current is reduced gradually for the cases from A6 to A8. This also confirms the outcome as shown in Figure 6.

But it also has to be kept in mind that increasing L_{sh} could increase the THD at the PCC, as given in Table 1. Therefore, in terms of design criteria for the selection of APF_{sh} units to place in multiple units with common DC link system, one should consider the higher values of L_{sh} and lower the difference between f_{sw} of the APF_{sh} units with care about THD.

7. Real-Time Performance Study

With the advancement of technology, real-time performance of any system can be observed using a real-time simulator. Instead of developing the complete actual system at full

capacity, the controller/system can either be modelled in software or can be built in hardware or can be a combination of both. In real-time simulation, the accuracy of the computations depends upon the precise dynamic representation of the system and the processing time to produce the results [15].

An electrical power system including 2 units of APF_{sh} has been modelled in MATLAB using RT-LAB (real-time simulation) tools to observe the performance in the real-time environment. The system is then tested in SIL (Software-in-Loop; both the controller and the plant are simulated in real-time in the same simulator) with the hardware synchronization mode (data communication is in real-time through the ADC/DAC) which is similar to hardware-in-loop (HIL) test. Figure 8 shows the real-time simulation structure in a SIL configuration used to develop the real-time environment by OPAL-RT. With the combination of MATLAB SPS (Sim Power System) from MATHWORKS and the RT-LAB toolbox from OPAL-RT, the real-time model of the power system and controller is developed for the real-time simulator.

Figure 9 shows the results for the cases A6, A7, and A8, where both the APF_{sh} units are compensating harmonic current in a power sharing mode. The waveform of the utility current (i_s) contains fewer harmonics for A7 compared to A6 and A8. This happens because of the moderate value of L_{sh} and h for A7 compared to that of A6 (L_{sh} is too low) and A8 (L_{sh} is too high). Therefore, the THD value is also reduced.

For the case of A8, although the THD increases, ZSCC is reduced. Figures 10(a), 10(c), and 10(e) show the ZSCC flow for these (A6–A8) cases and it clearly depicts the gradual

(a)

(b)

(c)

(d)

(e)

(f)

FIGURE 10: ZSCC flow for the cases (a) A6, (c) A7, and (e) A8; the zoom-in for one cycle (b) A6, (d) A7, and (f) A8.

reduction of ZSCC from A6 to A8. It is also clear from the zoom-in for one cycle study in Figures 10(b), 10(d), and 10(f) that a considerable amount of ZSCC can be reduced by proper selection of design parameters for the APF_{sh} units to operate in load sharing mode. Thus, it validates the simulation, analysis of the performance, and ZSCC flow study.

8. Conclusion

Capacity enhancement and operation flexibility are two of the important limitations of the centralized APF_{sh} unit when placed in a DG integrated network, especially in the low voltage distribution level where the compensating current

could be high. Therefore multiple APF_{sh} units can operate in parallel. This can be controlled in an active load sharing mode (intercommunication is required) or in droop control mode. The most important part is the common DC link between the APF units. Therefore, a circulating current could flow. In the case of a hysteresis current controller based multiple APF_{sh} units in load sharing mode, this CC control is not yet achieved. One of the difficulties of this CC flow control or reduction is the variable switching frequency of the APF_{sh} units. By proper selection of design parameters, this CC flow can be reduced in an acceptable level.

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