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Research Article

Design of a Single-Electron Memory Operating at Room Temperature

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Single-electronic transistors (SETs) are considered as the attractive component for the next generation of transistors due to their ultrasmall size and low power consumption. Because SETs with single island cannot work at high temperature normally, more researchers begin to carry out research on the SETs with N-dimension multi-islands. In this paper, we introduce a new architecture of single-electron memory; ideally the memory should operate in combination of SETs with a nanowire of two-dimensional regular array of multiple tunnel junctions (MTJs). This structure is analyzed and studied with Monte Carlo simulator, SIMON. The Coulomb blockade effect and thermionic effect play an important role in carrier conduction in the system at room temperature. Nanowire MTJs are used as an electrometer to sense the memory-node charge. The well-defined parameter in tunnel junction circuits helps to obtain the charging of single electrons in these circuits at room temperature.

1. Introduction

Single-electron devices (SEDs), which consist of at least one small conductive dot, are based on the so-called Coulomb blockade. If an electron tries to enter a small isolated region, the electrostatic energy of the region would increase; thus the electron cannot enter if the charging energy $e^2/2C$ is larger than the thermal energy k_BT, where C is the island capacitance, T is the temperature, e is the elementary charge, and k_B is the Boltzmann constant. Their great advantages are their small size than being more highly integrated and low power consumption. Since the operating temperature of an SET is determined by the geometrical size of the island that should be as small as a few nanometers to operate at higher temperature, it presents a challenge to the modern nanofabrication technology. One of the most promising applications of single electronics is the single-electron memory [1] in digital electronics, where information "bits" are defined by one, or at most a few, electrons, has found great interest. The single-electron charging and quantum confinement effects into the quantum dot also lead to stored electrons. Operating cell with a precise number of electrons is by controlling the magnitude of the writing voltage. The criteria that a good single-electron memory cell must fulfill are the operation temperature, the bit error, power consumption, and the same time short read and write cycles. Robustness against random background charge is a prerequisite, and the SET device must be manufacturable with today's technology.

However, the principal problem is that the operation of a single-electron transistor at room temperature requires extremely small island capacities of about 1 aF and thus structure widths around 1 nm. Such MTJ systems in a single-electron transistor (SET) are used for practical purposes, and recently, much effort has been focused on devices with more tunnel junctions between conducting islands of very small dimensions in order to observe a Coulomb blockade effect at room temperature and, if possible, up to high temperature. The effects of dot-size fluctuation can be overcome by using one array or more of nanodots and then the target $E_C \gg k_BT$ to get room temperature operation.

An MTJ memory in GaAs was used as the basis of the first intentionally designed single-electron memory cell, operated at 4.2 K by Matsumoto et al. [2]. A room temperature MTJ single-electron memory has been fabricated using an atomic force microscope by Nakazato et al. [3]. Nakazato et al. [4] have realized an alternative device consisting of a multiple

tunnel junction in silicon-on-insulator (SOI) material that precisely controls a small number of stored electrons on a memory node. Another important phenomenon regarding single-electron memory is that it should have a highly sensitive in the current of an SET electrometer in order to detect the small charges of stored electrons.

2. Cell Uses Two MTJs Nanowires and SET

2.1. Multi-Islands Nanowires. The dynamics of the system are governed by the following equation which gives the tunneling rate of an electron in a tunnel junction by using the "orthodox theory" [5] of single-electron tunneling:

$$\Gamma_{i\to j} = \frac{1}{e^2 R_T} \frac{\Delta F_{ij}}{1 - \exp\left(\Delta F_{ij}/k_B T\right)}, \tag{1}$$

where $\Delta F_{ij} = \Delta F_i - \Delta F_j = -eV_D$ is the difference between the free energy of the initial and final states, where V_D is the source voltage and R_T is the tunneling resistance of the junction. The tunnel resistance R_T of device as a function [6] of the material parameters: E_F (Fermi energy), Φ (height barrier), dimensions d (junction length), r (island radius), the effective mass of electron m, and h (Planck's constant) is as follows:

$$R_T = \left(\frac{h^3}{64\pi^2 me^2} \frac{(E_F + \Phi)^2}{E_F^2} \frac{1}{\Phi}\right) \times \left(\frac{2\pi}{hr}\sqrt{2m\Phi} \frac{\exp\left(4\pi d\sqrt{2m\Phi}/h\right)}{1 - \left\{1 - [r/(r+d)]^2\right\}^{1/2}}\right). \tag{2}$$

The second bracket contains the geometrical factor. The distance d should be smaller than 1 nm in order to get

$$R_H \approx 26\,\text{k}\Omega < R_T < 10^{10}\,\Omega. \tag{3}$$

The tunnel resistance has been plotted with the following hypothesis in Figure 1.

We have chosen only one digit values: $r = 3$ nm, $E_F = 4$ eV, and $\Phi = 3.5$ eV; no precise values have been chosen, and therefore the main value of the physical parameters which will be used needs to be justified. A schematic circuit of MTJs nanowire is illustrated in Figure 2. Two tunnel junction arrays are formed by N metallic islands on the insulator, as metal spheres in a homogeneous insulator, and $N + 1$ tunnel junctions connected in series with equal junction capacitances C_T. The source is connected to the ground. This will reduce the error to the order $1/MN$, where M and N are the number of junctions in parallel and in series, respectively. We developed and previously simulated the device structure using SIMON [7, 8].

The oxide layer separating the two MTJs is shown in Figure 2 by a capacitor C_{ox}. Such as approximate expression of the capacity of oxide:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_r S_{dot}}{d}. \tag{4}$$

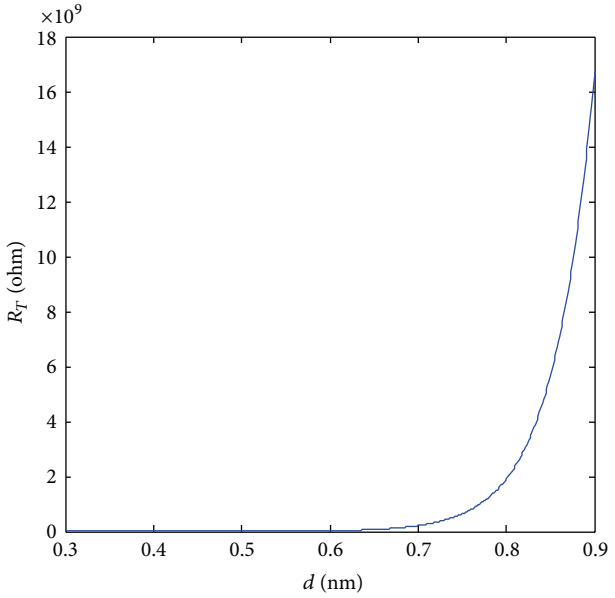

Figure 1: Characteristics of tunnel resistance as function of the junction length d.

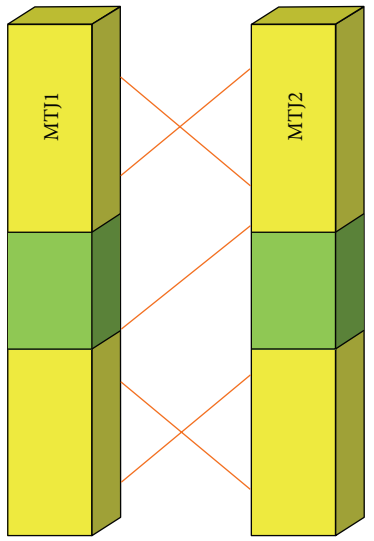

Figure 2: Nanowire with double MTJs arrays separated by an oxide layer represented by an oxide.

Figure 3 shows the drain source $I_{ds} - V_{ds}$ characteristics of a device for low and high temperatures. The effects of memory center are clearly observed with staircase fluctuations when an electron passes through the MTJs nanowire, and the large number of islands center gives an extra energy band to overcome the temperature problem of one single island of SET and also the polarization bias is increased then a single SET. The tunneling occurs through the system according to (1), and the effective capacitance C_{eff} of quantum dot centre is given by

$$C_{eff} = C_i + C_{ox}, \tag{5}$$

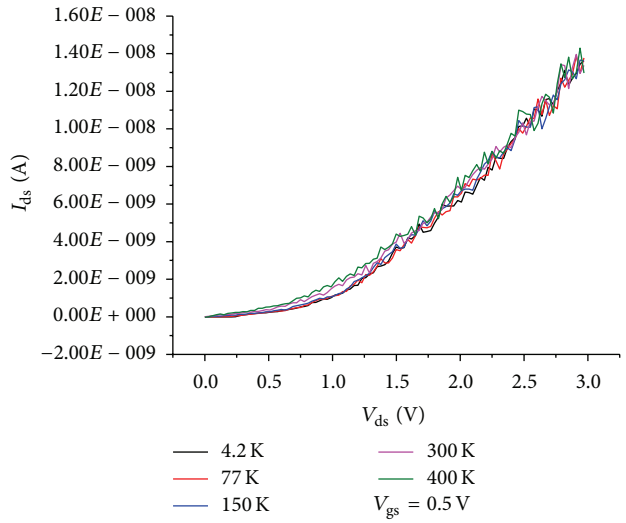

Figure 3: Current through MTJs nanowires as temperature functions, with $C_T = 2.10^{-19}$ F, $C_{ox} = 2.10^{-19}$ F, and $R_T = 4.10^{07}$ Ohm. Trap center is observed.

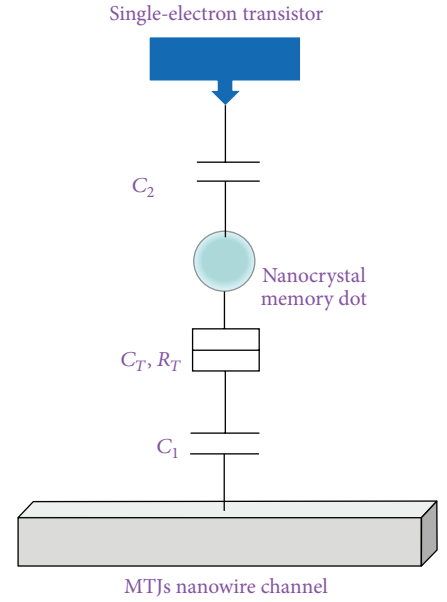

Figure 4: Schematic circuit of the basic single-electron memory cell.

where

$$C_i = \sqrt{C_{ox}^2 + 2C_T C_{ox}} - C_{ox}. \quad (6)$$

2.2. Quantum Dot Memory Description. Because the capacitances are connected in series, the total capacitance of the island inside the MTJs nanowire system is decreased, with an increase in the charging energy and so an increase in the temperature operation. The potential generated at the island by a single electron on the island is then given by

$$V_{dot} = -\frac{e}{C_{eff}}. \quad (7)$$

The effective capacitance may be used to obtain the charging energy for a single electron:

$$E_{ch} = \frac{e^2}{2C_{eff}}. \quad (8)$$

In our case $C_{eff} = 0.316$ aF, C_{eff} is lower than the total capacitance attached to an island $2C_T + C_{ox} = 0.6$ aF, and $E_{ch} = 0.25$ eV $= 10k_BT$ (0.025 eV at 300 K). This proves that the charging energy is much higher than the thermal energy at 300 K and therefore we can say that increasing the number of tunnel junctions and the MTJ networks can overcome the effect of low capacity and temperature operation. Blocking zone is more important when the number of junctions decreases. The charging energy of the island creates an energy barrier which blocks the entrance of electrons into the MTJ so that multistable states of different numbers of electrons can be formed. The MTJ is also important in suppressing cotunneling effects, that is, electron tunneling simultaneously across more than one junction. The blocking region is more important when the number of junctions increases. For a current in the order of nanoamperes, the tunnel resistances must be lowered to 10^8 Ω. Phase locking in nonuniform array of MTJ gives values of life time equal to 385 cycles for 11 junctions arrays and life time of 15900 cycles for 185 tunnel junctions.

3. The Single-Electron Memory Array

3.1. Principle. We now consider a single-electron memory circuit, with the principal parts of basic circuit schematic shown in Figure 4, which consists of an MTJs nanowire cell coupled with a simple single-electron transistor. This idea is based on the electron-trap memory cells proposed in [9, 10]. The charged state and the uncharged state, the excess of a precise number of electrons stored on the memory dot, can be used to represent binary information "1" and "0" and are depending on the circuit parameters used to control the charging of the memory node. SET, capacitively coupled via a capacitor C_c, is used to control the charging of the memory node (write and erase operations). The write operation is sensed in the current of the MTJs nanowire (read the information). The current through the SET will be sensitive to the number of electrons in memory node.

Each MTJ array has 6 tunnel junctions coupled to an oxide layer. The resistance of each one of these junctions is 4.10^7 Ω and the capacitance is 2.10^{-19} F. The SET parameters are defined by $R_D = R_S = 4.10^6$ Ω and $C_D = C_S = C_g = C_c = C = 2.10^{-18}$ F, where C is the capacitive effect of the substrate. By applying a positive voltage V_{ds} or V_{gs}, if the energy can provide the Coulomb blockade energy, an electron or a small number of electrons is transported from the ground to island. When the writing voltage increases, the number of electrons on the memory node can be changed. The energy of the Coulomb blockade in the array of single-electron memory cells makes it possible to enable and disable certain single electron.

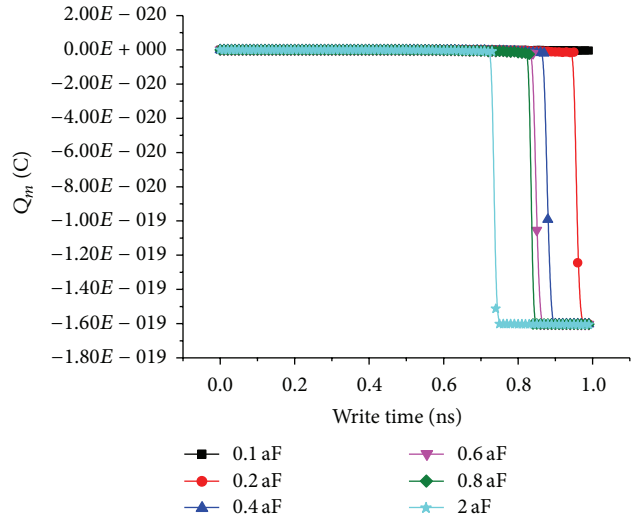

FIGURE 5: On the time evolution of the charge in the dot of memory as function of V_{ds} bias.

3.2. Storage in the Node Memory. The simulated operation of the memory cell is shown in Figure 5. So the first electron will enter the array only when it becomes energetically favorable. This occurs at some critical value Q_c of the induced charge, defined by [11]

$$Q_c = \frac{eC_{MTJ}}{C_\Sigma}\left(\frac{1+\Delta}{2}\right). \quad (9)$$

C_Σ is the total capacitance connected to the memory node and can be expressed as $C_\Sigma = C_{MTJ} + C_S + C_G$.

The parameter $\Delta = (1 - 1/N)(C_\Sigma/C_{MTJ} - 1)$, where N is the number of islands in the MTJ nanowire. The passage of electrons through the nanowire is blocked when the modulus of the charge Q on one side of this device is less than the critical charge Q_c.

Here, τ, the time required to charge up the memory node, can be approximated with the previous data as

$$\tau = 2NR_{MTJ\_Nw}C_{MTJ\_Nw}. \quad (10)$$

The probability for a bit error has to be below 10^{-20}; then we get $t > 46\tau$; therefore one must wait about 0.46 ns for a tunnel event to occur. This approximation is very close to the result given by SIMON shown in Figure 5.

The coupling oxide is in a direct relationship with the memory effect as well as the write time. The source drain actuates the potential of the memory node through the capacitive coupling term to overcome the charging energy due to the nanocrystal memory node self-capacitance. The potential on the central nanocrystal node memory is reduced from (7) to 0.44 V.

3.3. Detection of Stored Charge. Initially, the voltage V_{ds} is zero and there are no excess electrons at the memory node. After 0.4 ns, V_{ds} reaches the value of 0.2 V; at this time an electron is transported from the ground and stored with Coulomb blockade effect. This causes the positive current pulse in Figure 6. After that, the value of V_g becomes 0.3 V again a second electron can be memories because it surmount the potential barrier imposed by the tunnel junctions. MTJs nanowire is used as a sense transistor to detect the memory-node voltage. Each trapped electron represents a peak of current in the nanowire tunnel junctions arrays. When the write voltage returns to the initial state, the electron reaches the nanocrystal memory node and a negative current peak is detected in the nanowire system and proves the discharge of memory node. The maximal charge stored per nanocrystal is around 8 electrons. This value is obtained with a source-drain bias voltage of 10 V with a minimum writing time of 1 nanosecond.

With a nanowire of tunnel junctions we can obtain a higher Coulomb gap as well as in averaging out the background charge fluctuations. For these devices, the threshold shift cannot always be measured from the initial uncharged state because of the difficulty in removing the electrons from the nanocrystal memory node. We found that the threshold voltage shifted continuously with charging voltage. At a given charging voltage, the threshold shift increased with charging time as seen in Figure 7.

3.4. Temperature Effect. There is a critical temperature T_c above which the electrons can be stored in the node. The memory-node storage depends both on the voltage applied to the gate/source drain and on the temperature. Figure 8 proved that the thermionic effect plays a very important role in the memory effect of the structure. The writing of the logic "1" starts at $T_c = 256$ K. The fluctuation of charges begins when T is near the critical temperature, and for temperatures below T_c, no memory effect is observed.

As the oxide thickness decreases, the tunnel current density increases. The reduction of the barrier due to high temperature promotes the passage of electrons by Tunnel Fowler-Nordheim tunneling in the case of thick oxide (>10 nm) [12]. The reduction of the barrier leads to a decrease

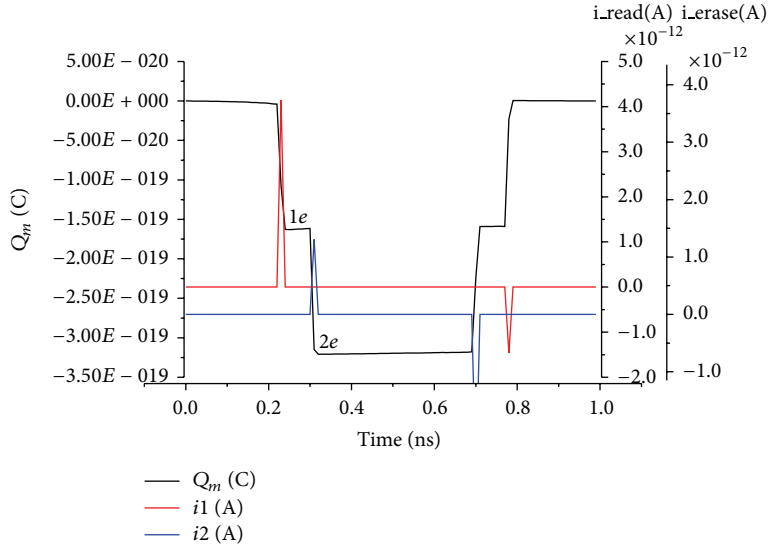

Figure 6: MTJs nanowire detection of state "1" and state "0."

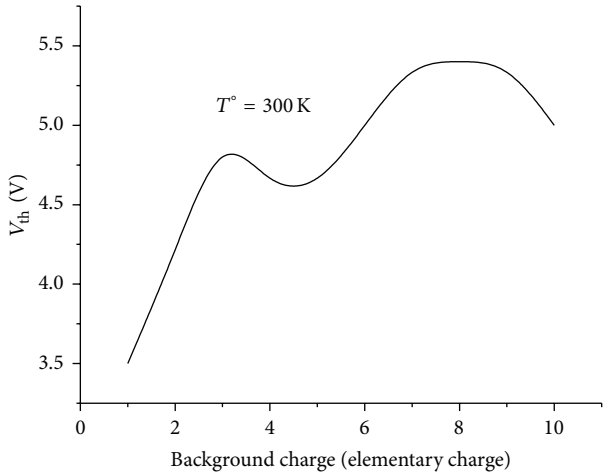

Figure 7: Background charge effect on the threshold voltage.

in the effective length of the potential barrier that must cross the particle and thus to an increase in the probability of transition. If the magnitude of the write pulse function is less than $C_\Sigma V_C/C_g$, then no electrons are written to the memory. During a positive write pulse, the voltage across the MTJs nanowire greater than V_C causes change to the state of the memory. During a negative write pulse, the stored electrons are removed from the memory node via the nanowire.

3.5. Retention of Cell. Moreover, we suggest that the conduction process responsible for the injection of electrons through the tunnel oxide is direct tunneling at low voltages and Folder-Nordheim tunneling at higher voltages. The charging kinetics can be expressed as [13] a simple expression for the retention time of the cell, as a function of the Coulomb blockade voltage V_c in the MTJs nanowire:

$$t_{1/2} \approx \frac{R_{\mathrm{MTJ}}C}{eV_c} k_B T \exp\left(\frac{eV_c}{2k_B T}\right), \tag{11}$$

where $t_{1/2}$ is the time taken to lose half of the stored charge and

$$V_c = \frac{e}{2C_{\mathrm{dot}}}. \tag{12}$$

According to the results shown in the curve in Figure 9, the retention time is depending on the nanocrystal memory center. When we use a large nanocrystal, the retention time increases; the structure containing nanocrystal of 10 nm, that is, 84% of the initial injected charges, is still stored after about 10^4 seconds, whereas the structure containing 5 nm nanocrystal lost less than 84% of its charge in 500 seconds.

4. Conclusion

In this work, the operation of a new design of memory cell has been described and checked by the Monte Carlo simulator SIMON. The MTJs nanowire is a good detector of

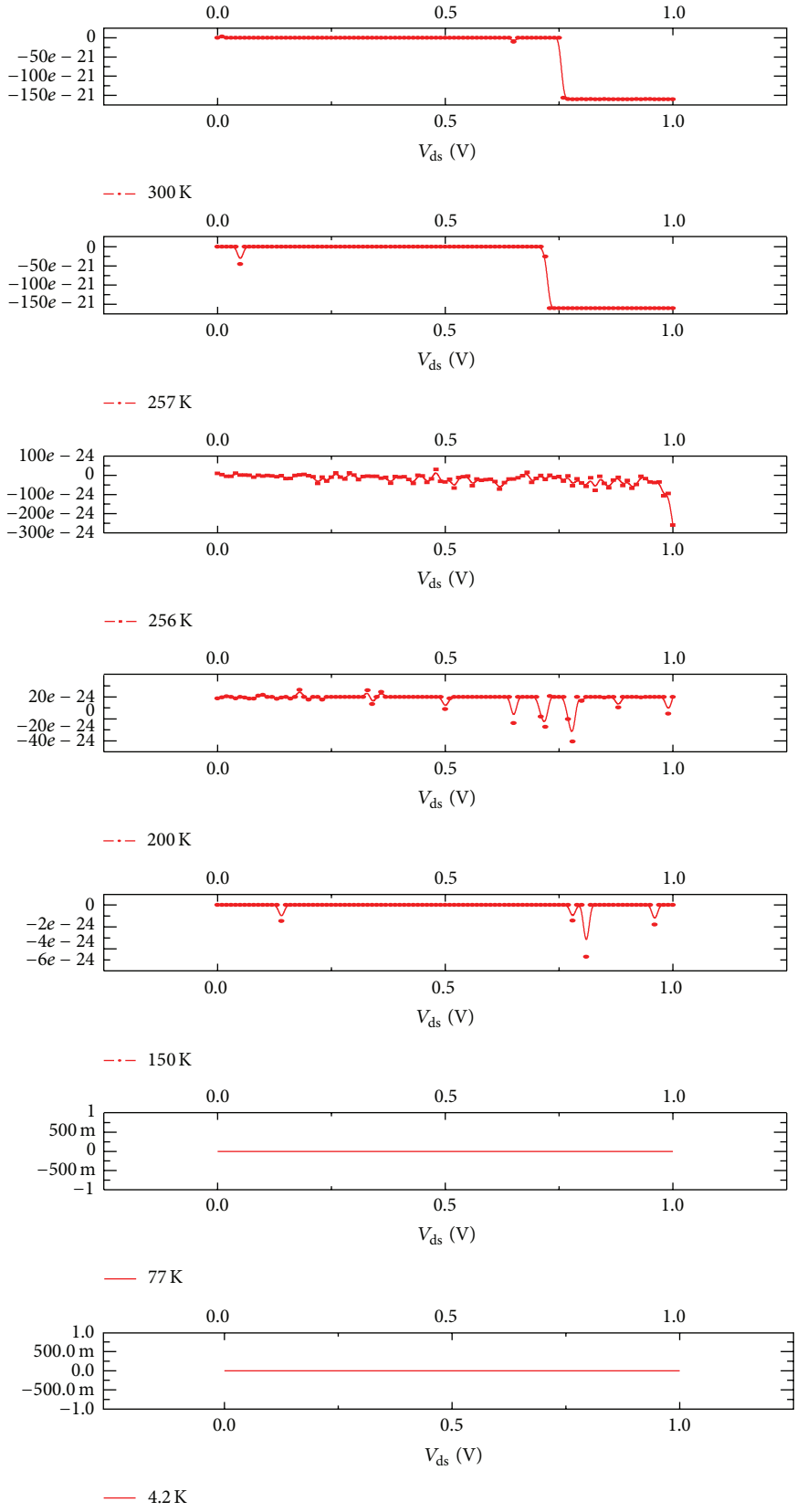

Figure 8: Evolution of the charge in the dot of memory as a function of temperature.

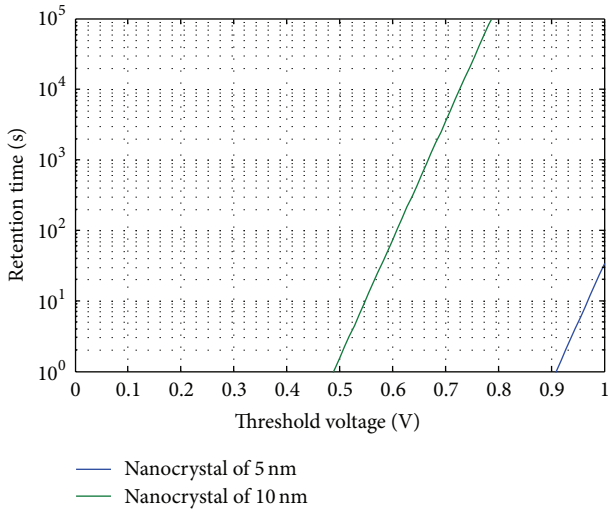

Figure 9: Evolution of the charge in the dot of memory as a function of threshold voltage and of the nanocrystal diameter.

single charge in a memory centre. Simulation demonstrated a long retention time for large nanocrystal memory node; the designed structures operate as nonvolatile memory devices. The gap of single-electron transistor and MTJs nanowire give to the memory a large temperature operation and a high write voltage.

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