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Microcontroller Based Less Switches Topology and Digital Gating Technique for Single-Phase Five-Level Inverter

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The multilevel inverter is the idea of connecting such distributed DC energy sources (solar and fuel cells in addition to rectified output of wind turbines) to a power grid. Multilevel pulse width modulation (PWM) inverters have gained importance in high performance power applications without requiring high ratings on individual devices. The elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage DC sources to perform the power conversion by synthesizing a staircase voltage waveform. In the present paper we introduce a power circuit for single-phase five-level inverter which contains a very lower number of switches and the technique for the generation of required signals to control the operation of the inverter switches. The presented technique is implemented via microcontroller ATmega16. The simulation and practical results are presented.

1. Introduction

Multilevel inverter has become an effective and practical solution for reducing switching losses in high power voltage source inverter (VSI) applications [1, 2]. By synthesizing the AC output voltage from several levels of DC voltages, a staircase or multilevel output waveform is produced. For a conventional VSI, the maximum voltage level output is determined by the voltage blocking capability of each device. In many cases, the power device blocking capability could not reach the required DC link voltage, hence limiting their application. Ingenious methods such as device series connection to increase the blocking capacity may result in very complicated and unreliable circuits [2].

By using a multilevel structure, the stress on each device can be reduced in proportional to the number of levels; thus the inverter can handle higher voltages [3]. It may be possible in certain application to avoid expensive and bulky stepup transformers.

Another significant advantage of a multilevel output waveform is that several voltage levels lead to a better and more sinusoidal voltage waveform. As a result, a lower total harmonic distortion (THD) is obtained. In another perspective, the harmonic in the output waveform can be reduced without increasing switching frequency or decreasing the inverter power output [4]. As the number of voltage levels reaches infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints. In motor application, high dV/dt in power supply generates high stress on motor windings and requires additional motor insulation. Furthermore, high dV/dt of semiconductor devices increases the electromagnetic interference (EMI), common mode voltage, and possibility of failure on motor. With several levels in output waveform constructed by multilevel inverter, the switching dV/dt stresses are reduced [3]. With these known advantages, multilevel VSI has become a popular alternative to the conventional VSI. There are various works carried out in this area, but there appears to be limited publications on the analytical method to calculate the harmonics spectra of the output voltage. The multilevel inverter is the idea of

connecting such distributed DC energy sources (solar and fuel cells in addition to rectified output of wind turbines) to a power grid. Multilevel pulse width modulation (PWM) inverters have gained importance in high performance power applications without requiring high ratings on individual devices, as static VAR compensators, drives, and active power filters. A multilevel inverter divides the DC rail directly or indirectly, so that the output of the leg can be more than two discrete levels. As both amplitude modulation and pulse width modulation are used in this, the quality of the output waveform gets improved with low distortion. The advantages of multilevel inverter are good power quality, low switching losses, reduced output dV/dt, and high voltage capability [5, 6].

Increasing the number of voltage levels in the inverter increases the power rating. The three main topologies of multilevel inverters are the Diode-clamped inverter, flying capacitor inverter, and the cascaded H-bridge inverter [1, 2, 7].

When we are talking about the numbers of power switches to form the multilevel inverter, we found that, for example, in case of five-level diode clamped inverter each leg requires 8 power switches, 12 diodes, and 4 capacitors for sharing the DC link, in general $(m-1)$ switches, $(m-1)(m-2)$ diodes, and $(m-1)$ capacitors for sharing the DC link). In case of capacitor clamped five-level inverter, it requires 8 switches, 6 capacitors, and 4 capacitors for sharing the DC link (in general $(m-1)$ switches and $(m-1)*(m-2)/2$ capacitors in addition to $(m-1)$ capacitors for sharing the DC link). So it is simple to note the power circuit complication in addition to the complexity of the generation of the signals to control the operation of the switches [8].

In the present paper we introduce a power circuit for single-phase five-level inverter which contains a very low number of switches and the technique for the generation of required signals to control the operation of the inverter switches. The presented technique is implemented via microcontroller. The simulation and practical results are presented.

Table 1: Diode-clamped five-level inverter voltage levels and their switching states [2].

Output V_{ao}	Switch state							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$
$V_5 = V_{dc}/2$	1	1	1	1	0	0	0	0
$V_4 = V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3 = 0$	0	0	1	1	1	1	0	0
$V_2 = -V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1 = -V_{dc}/2$	0	0	0	0	1	1	1	1

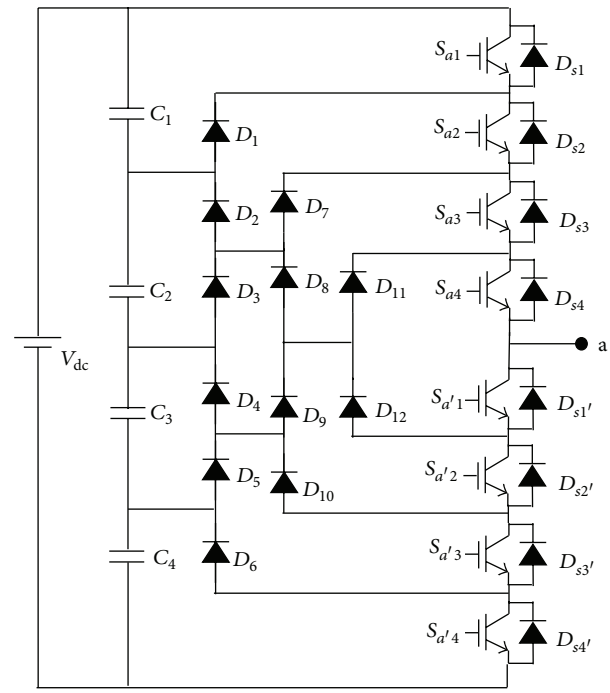

Figure 1: Diode-clamped one-leg Five-level inverter circuit.

2. Classical Multilevel Power Circuit Topology and Operation

It is a fact, until today, multilevel topologies are the best alternative to implement low-frequency based inverters with low output voltage distortion. The most common multilevel topologies are as follows.

2.1. Diode-Clamped Multilevel Inverter (DCMLI). The circuit of DCMI is shown in Figure 1 for five-level inverter. A total of eight switches and twelve diodes of equal voltage rating are used. In this circuit not only the main switches are clamped by the clamping diodes, the clamping diodes are clamped mutually by other clamping diodes. Thus the need for large RC network to deal with voltage sharing problem among series connected diode is removed. In general, a single m-level inverter phase leg requires $(m-1)$ storage capacitors, $2(m-1)$ switches, and $(m-1)(m-2)$ diodes.

For five-level case, the output voltage levels and their corresponding switching states are listed in Table 1. For simplicity the operation can be decomposed into two level switching cells, in cell (a), switches S_{a2}, S_{a3}, and S_{a4} are always on, while switches S_{a1} and $S_{a'4}$ work alternately to give the output voltage V_{ao} of V_{dc} and $3V_{dc}/4$, respectively. Similarly, in cell (b), switches S_{a3}, S_{a4}, and $S_{a'1}$ are always on, while switches S_{a2} and $S_{a'2}$ work alternately to give the output voltage V_{ao} of $3V_{dc}/4$ and $V_{dc}/2$, respectively. In cell (c), switches S_{a4}, $S_{a'1}$, and $S_{a'2}$ are always on, while switches S_{a3} and $S_{a'3}$ work alternately to give the output voltage V_{ao} of $V_{dc}/2$ and $V_{dc}/4$, respectively. Finally, in cell (d), switches $S_{a'1}$, $S_{a'2}$, and $S_{a'3}$ are always on, while switches S_{a4} and $S_{a'4}$ work alternately to give the output voltage V_{ao} of $V_{dc}/4$ and 0, respectively [9–11].

2.2. Capacitor Clamped Multilevel Inverter (CCMLI). A similar topology to the DCMLI topology is the capacitor clamped (CC), or flying capacitor, multilevel inverter topology, which can be seen in Figure 2. Instead of using clamping diodes it uses capacitors to hold the voltages to the desired values. The number of capacitors required is $(m-1)*(m-2)/2$ in addition

Table 2: Switching states for capacitor clamped five-level inverter.

Output voltage	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
$-V_{dc}/4$	1	0	0	0	1	1	1	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1

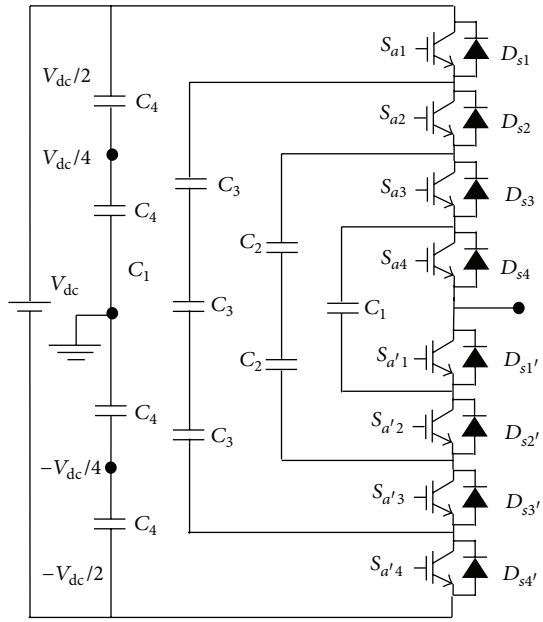

Figure 2: Circuit diagram of one leg of capacitor clamped five-level inverter.

to $(m-1)$ number of capacitors on a shared DC bus, where m is the level number of the inverter. Instead of clamping diodes, one or more (depending on position and level of the inverter) capacitors are used to create the output voltages. They are connected to the midpoints of two switch pairs on the same position on each side of the a midpoint between the switches [12].

The big difference is the use of clamping capacitors instead of clamping diodes, and since capacitors do not block reverse voltages, the number of switching combinations increases [10]. Several switching states will be able to generate the same voltage level, giving the topology redundant switching states. The sum of a certain output voltage is generated by the DC bus voltage $\pm V_{dc}2$ and one or more of the clamping capacitors voltages added together.

Table 2 illustrates the switching of operation of capacitor clamped five-level inverter [13].

2.3. Multilevel Inverter Using Cascaded Inverters (CMLI). This type of multilevel inverter uses cascaded of H-bridge inverters (single-phase full bridge) with separate DC sources. The general function of this multilevel inverter is the same

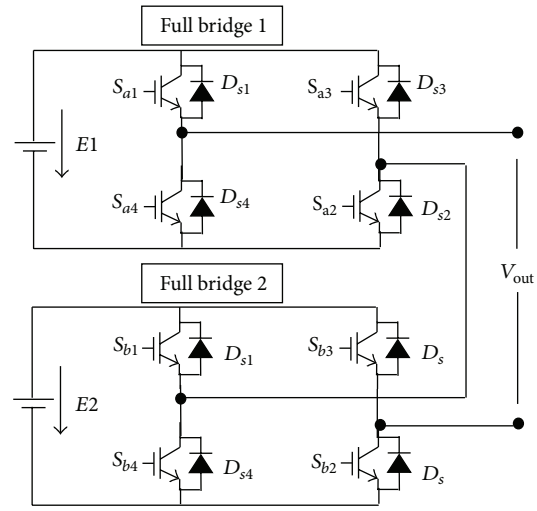

Figure 3: Circuit diagram of cascade multilevel inverter.

as that of the other two previous inverters. The multilevel inverter using cascaded inverter with SDCSs synthesizes a desired voltage from several independent sources of DC voltages, which may be obtained from either batteries, fuel cells, or solar cells. This configuration recently becomes very popular in AC power supply and adjustable speed drive applications. This new inverter can avoid extra clamping diodes or voltage balancing capacitors. A single-phase m-level configuration of such an inverter is shown in Figure 3 [14–16].

Each bridge is associated with a single-phase full-bridge inverter. The ac terminal voltages of different level inverters is connected in series. By different combinations of the four switches, $S_1 - S_4$, each inverter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$, and zero. The ac output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. Note that the number of output phase voltage levels is defined in different ways from those of two previous inverters. In this topology, the number of output phase voltage levels is defined by $m = 2s + 1$, where s is the number of DC sources. The number of switches required is $2(m - 1)$. The advantage of this type is circuit layout. Modulated circuit layout and packaging are possible because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitors [9, 13, 17].

Finally we presented a comparison between the three types of multilevel inverters as summarized in Table 3.

3. Low Switches Number Five-Level Inverter (LSFLI)

It is clear from the upper presented types of inverters and referring to Table 3 that the number of the components used is high; for example, the circuit of single-phase bridge diode-clamped five-level inverter requires 16 switches, 24 clamping

Table 3: Comparison of power components required for one leg.

Inverter Configuration	Diode Clamped	Capacitor clamped	Cascade inverter
Main switching devices	$2(m-1)$	$2(m-1)$	$2(m-1)$
Main diodes	$2(m-1)$	$2(m-1)$	$2(m-1)$
Clamping diodes	$(m-1)(m-2)$	0	0
DC bus capacitors	$(m-1)$	$(m-1)$	$(m-1)/2$
Clamping capacitors	0	$(m-1)(m-2)/2$	0

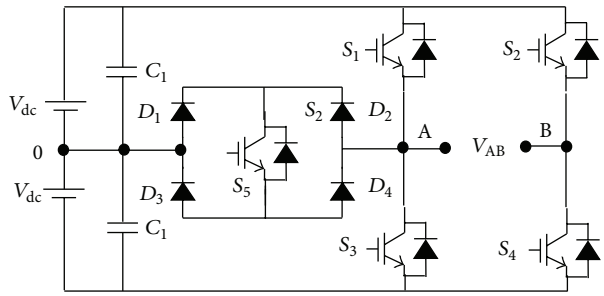

Figure 4: Circuit diagram of low number of switches five-level inverter.

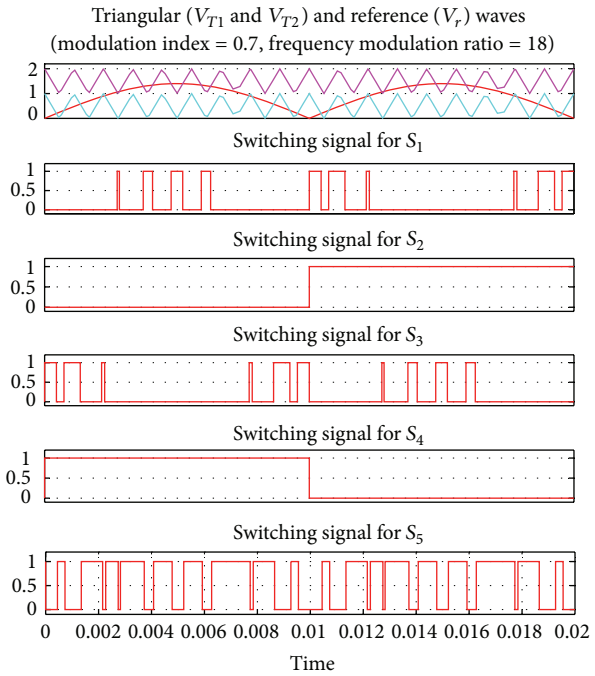

Figure 5: Principle of gating signals generation for the inverter switches (FMR = 18, MI = 0.7).

diodes which rise the cost and the complexity of the control circuit.

In the presented five-level inverter topology it requires only five switches and four diodes of the same rating as shown in Figure 4. The operation of the circuit is as follows.

During the positive half cycle of the reference output voltage

(i) S_4 is switched ON (S_2 is OFF);

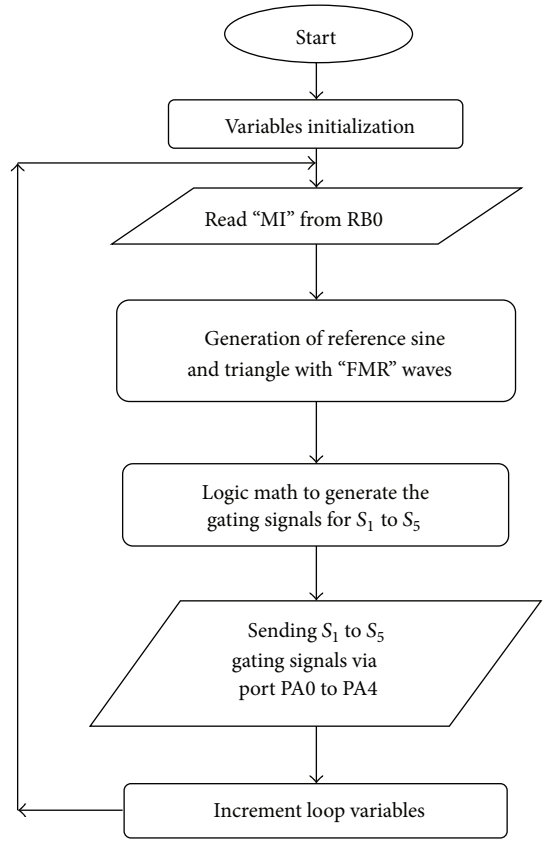

Figure 6: The flowchart of the proposed gating signal generation for five-level inverter.

(ii) if the PWM signal is applied on the gate of switch S_1 (during which case switch S_3 is OFF), there are two cases: when switch S_1 is turned ON, S_5 is OFF (which means both S_3 and S_5 are off, and of course S_4 is ON), so the output voltage (V_{AB}) is ($+2V_{dc}$); the other case is when S_1 is OFF, S_5 is ON (which means that S_3 is OFF and S_5 is ON, and of course S_4 is ON), in such case the point A of the output voltage is connected to the midpoint of the DC source which gives an output voltage $(V_{AB}) = (0 - (-V_{dc})) = +V_{dc}$;

(iii) if the PWM signal is applied on the gate of switch S_3 (during which case switch S_1 is OFF), there are two cases: when switch S_3 is turned OFF, S_5 is ON (which means S_1 is OFF, S_3 is OFF, S_4 is ON, and S_5 is ON), so the output voltage $(V_{AB}) = (0-(-V_{dc})) = +V_{dc}$; the other case when S_3 is ON, S_5 is OFF (which means

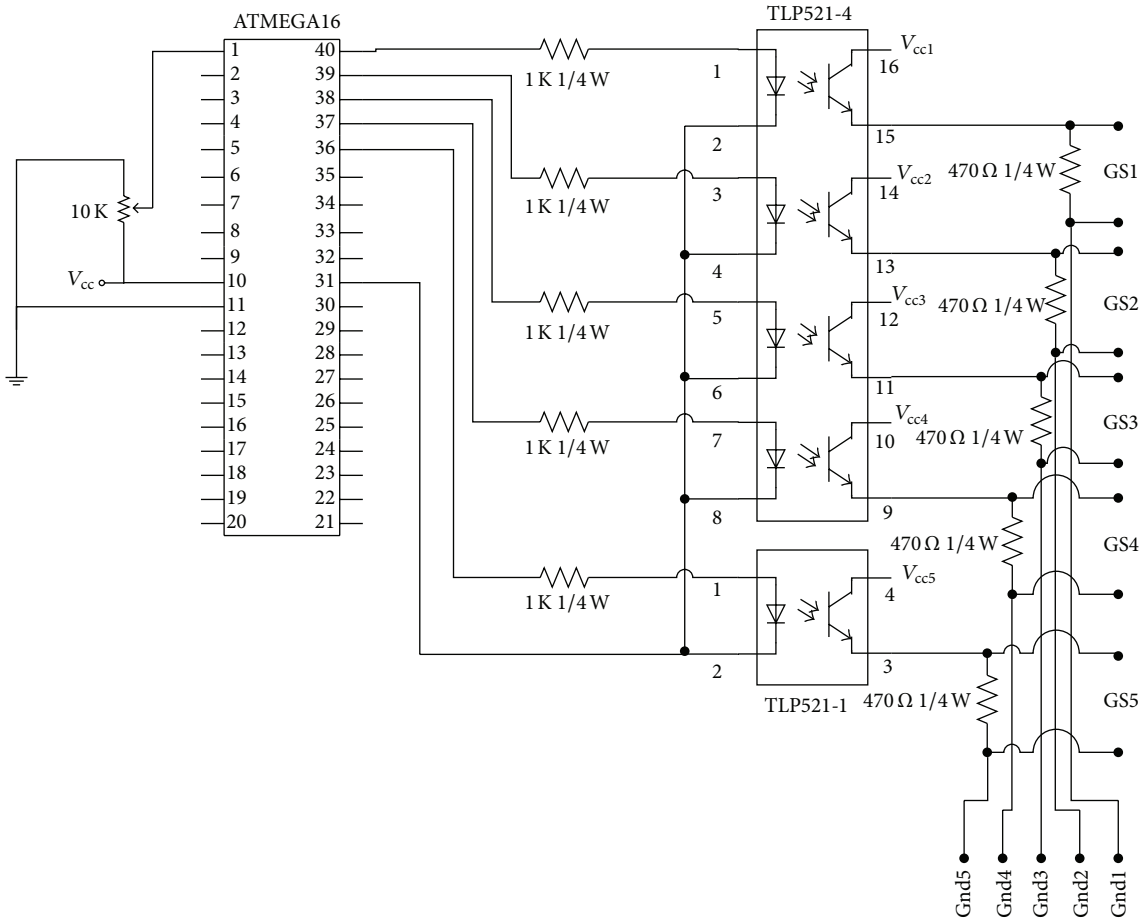

Figure 7: Proposed hardware circuit layout of single-phase five-level inverter.

that S_1 is OFF, S_3 is ON, S_4 is ON, and S_5 is OFF), in such case the load is short circuited by the lower part of the bridge and the output voltage (V_{AB}) = 0;

(iv) summary of this period: when S_1 is turned ON and OFF, the output voltage varies between $+2V_{dc}$ and $+V_{dc}$, respectively. When S_3 is turned OFF and ON, the output voltage varies between $+V_{dc}$ and 0.

During the negative half cycle of the reference output voltage

(i) S_2 is switched ON (S_4 is OFF);

(ii) if the PWM signal is applied on the gate of switch S_3 (during which case switch S_1 is OFF), there are two cases: when switch S_3 is turned ON, S_5 is OFF (which means both S_1 and S_5 are off, and of course S_2 is ON), so the output voltage (V_{AB}) is ($-2V_{dc}$); the other case is when S_3 is OFF, S_5 is ON (which means that S_3 is OFF and S_5 is ON, and of course S_2 is ON), in such case the point A of the output voltage is connected to the midpoint of the DC source which gives an output voltage (V_{AB}) = (0 − (+V_{dc})) = $-V_{dc}$;

(iii) if the PWM signal is applied on the gate of switch S_1 (during which case switch S_3 is OFF), there are two cases: when switch S_1 is turned OFF, S_5 is ON (which means S_3 is OFF, S_1 is OFF, S_2 is ON, and S_5 is ON), so the output voltage (V_{AB}) = (0 − (+V_{dc})) = $-V_{dc}$; the other case is when S_1 is ON, S_5 is OFF (which means that S_1 is ON, S_3 is OFF, S_2 is ON, and S_5 is OFF), in such case the load is short circuited by the upper part of the bridge and the output voltage (V_{AB}) = 0;

(iv) summary of this period: when S_1 is turned ON and OFF, the output voltage varies between $+2V_{dc}$ and $+V_{dc}$, respectively. When S_3 is turned OFF and ON, the output voltage varies between $+V_{dc}$ and 0;

(v) summary of this period: when S_3 is turned ON and OFF, the output voltage varies between $-2V_{dc}$ and $-V_{dc}$, respectively. When S_1 is turned OFF and ON, the output voltage varies between $-V_{dc}$ and 0.

Table 4 summarized the switching states of the low switches five level inverter.

Then the advantages of the presented five-level circuit are the following.

(1) Reduction in the number of components when the initial cost reduces.

(2) Controlling becomes easier.

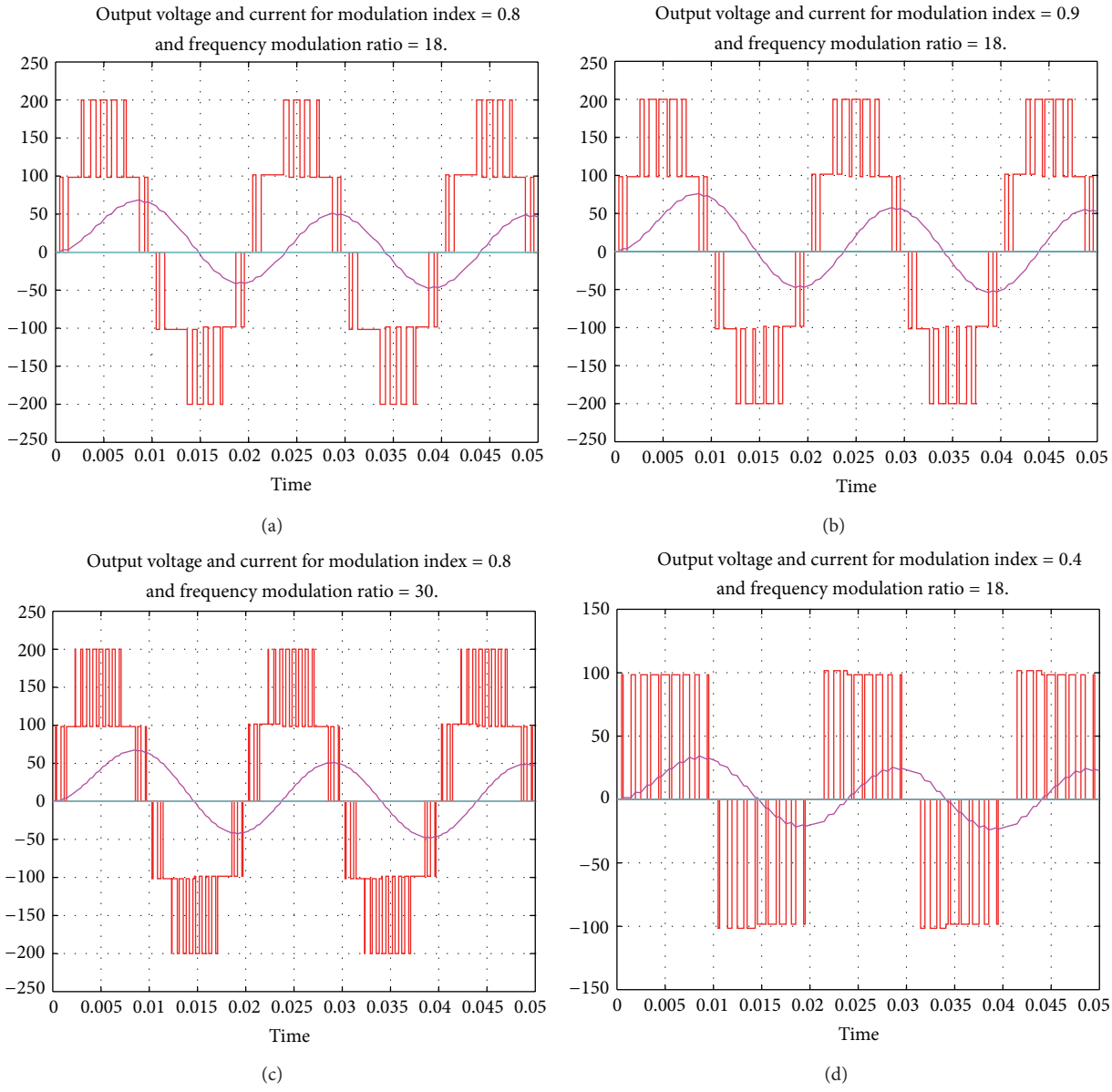

Figure 8: The simulation results using MATLAB.

(3) Losses become less due to the elimination of the harmonics.

(4) Apt structure for industrial applications.

(5) Overall weight reduces because of the usage of less number of components.

4. Gating Pulses Generation

If we suppose that the reference (wanted) sine wave output voltage of frequency of F_R of peak value of A_R and the modulation (carrier) signal have a frequency of Fc whose peak value of Ac, then the modulation index (MI) is A_R/Ac, and the frequency modulation ration (FMR) is Fc/F_R. In order to generate the required gating pulses, the basic idea depending on a sinusoidal reference signal of frequency F_R is first rectified and compared with the carrier triangular signals. There are two triangular signals; the first one (V_{T1}) varies from two

Table 4: The switching state and output voltage of low number of switches five-level inverter.

Switches state					Output voltage (V_{AB})
S_1	S_2	S_3	S_4	S_5	
1	0	0	1	0	$+2V_{dc}$
0	0	0	1	1	$+V_{dc}$
0/1	0/1	1/0	1/0	0/0	0
0	1	0	0	1	$-V_{dc}$
0	1	1	0	0	$-2V_{dc}$

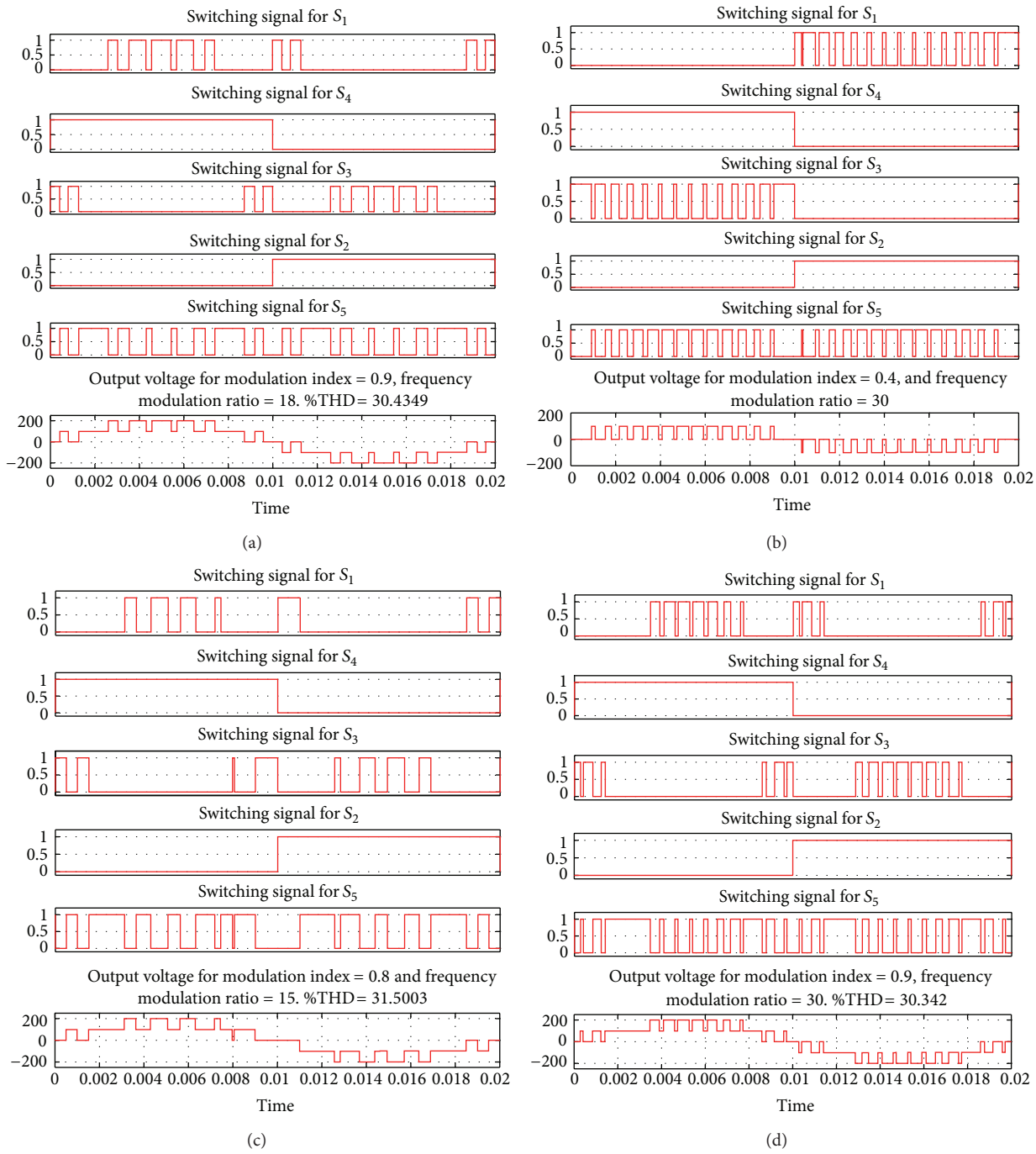

FIGURE 9: The simulation results using Visual Basic.

peaks of zero and 0.5 Vm, while the second one (V_{T2}) is of the same phase shift with the first signal but has an offset of 0.5 V.

During the positive half cycle of the reference signal (V_R), the crossing of the reference signal with (V_{T1}) generates the gating signals for the switch S_3, and the crossing of the reference signal with (V_{T2}) generates the gating signals for the switch S_1. S_4 is ON during this period, and S_5 is the inversion of ($S_1 + S_3$).

During the negative half cycle of the reference signal, the crossing of the reference signal with (V_{T1}) generates the gating signals for the switch S_1, and the crossing of the reference signal with (V_{T2}) generates the gating signals for the switch S_3. S_2 is ON during this period, and S_5 is the inversion of ($S_1 + S_3$).

The algorithm depends on the principle that the value of the reference sine voltage between two sampling periods (the sampling period equal to reference time/FMR) can be transformed in a pulse signal whose average value is the same as that of the reference voltage during the same period. Figure 5 shows the principle of the gating signals generation in addition to the output voltage.

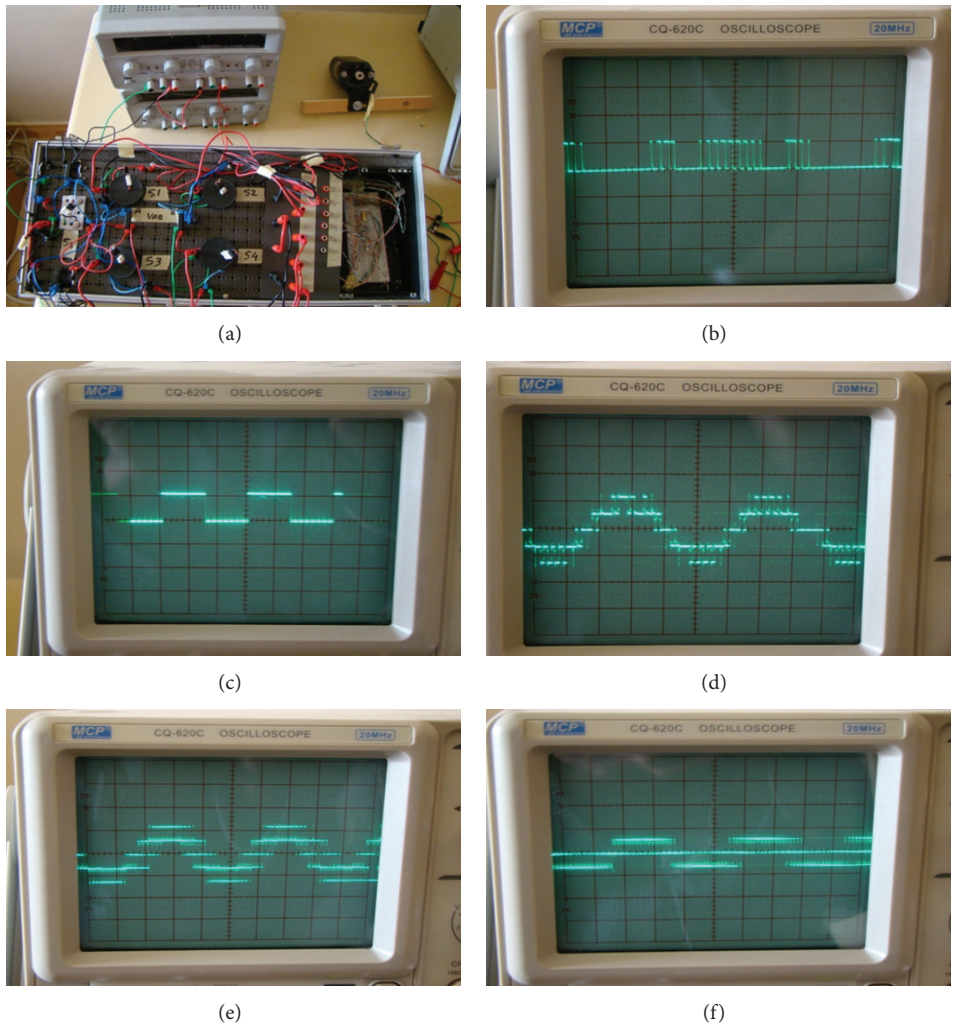

FIGURE 10: Experimental results: (a) implemented prototype setup, (b) and (c) gating for S_1 and S_4 signals, respectively, (d) output voltage for MI = 0.8 and FMR = 18, (e) output voltage for MI = 0.8 and FMR = 30, and (f) output voltage for MI = 0.4 and FMR = 18.

5. Hardware Implementation

The generation of the necessary gating signals for S_1 to S_5 is done using the mentioned algorithm by means of a microcontroller; the hardware consists of the following parts.

(1) ATMEGA16 in which the algorithm is implemented.

(2) TLP521-4 photocoupler for isolation and driving circuit.

(3) MOSFET IRF540.

(4) 1N-4007 Diode.

The variation of the nodulation index can be varied externally by means of a variable DC input, while the generation of sine and triangular waveforms and their comparison, logic operation, and other required signals is realized inside the microcontroller. Once the switches signals are output from the microcontroller, the signals are applied to the MOSFET gates via isolation and driving circuit. Figure 6 shows software flowchart, and the algorithm is implemented in the microcontroller using flow code V_4 programming. Figure 7 demonstrates the hardware circuit diagram.

6. Simulation and Practical Results

The system presented in this paper (Figure 7) is firstly simulation using two well-known programming languages (MATLAB and Visual Basic). Figure 8 shows the results of four cases of simulation using MATLAB while Figure 9 shows the results of four cases using Visual Basic program.

The proposed hardware of the inverter is implemented practically and tested for many cases; some of them are presented in Figure 10 in which cases the modulation index, (MI) and its value are varied by means of external variable dc voltage, and the frequency modulation ratio (FMR) is varied;

Table 5: The values of THD against the FMR.

FMR	15	18	30	40	60	80	100
% THD	31.0	30.5	30.5	27	26	25	18

it is noted that when the modulation index is equal or below 0.5, then the inverter works in three-level mode while the inverter works in five-level mode if the modulation index more than 0.5. In addition to the output voltage the values of total harmonic distortion are also presented for some cases as listed in Table 5 for MI = 0.9.

7. Conclusions

Multilevel inverter PWM offers more degree of freedom and advantages over the traditional two-level PWM inverter. The traditional five-level bridge inverter requires 16 power switches with their gating signal circuit in addition to the 12 power diodes, while the inverter power circuit presented in this paper requires only five switches and four power diodes.

The algorithm for the generation of the gating signal for the power switches is implemented by microcontroller Atmega16, and the driving circuits are also designed.

The presented inverter is implemented practically, the experimental results given are very closed to the simulation results, and they are very reasonable.

As presented in Table 5 the percentage of THD is the range of the results presented by other well-known techniques (such as level shifting PWM). It is also important to point out that as the FMR increases, the THD decreases, and of course the switching losses are the limit.

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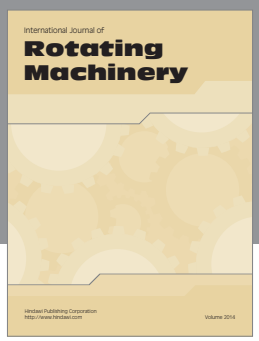

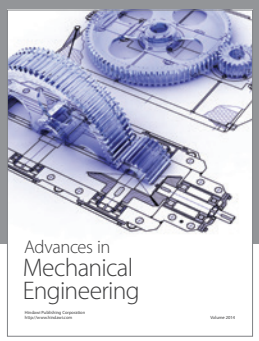

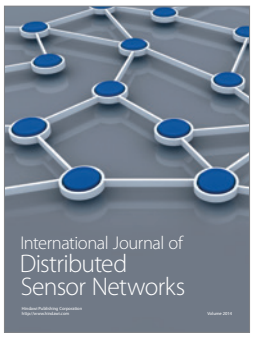

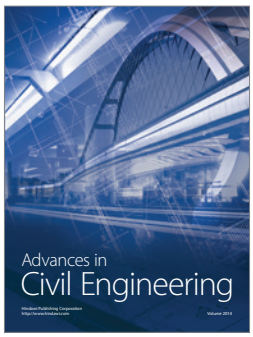

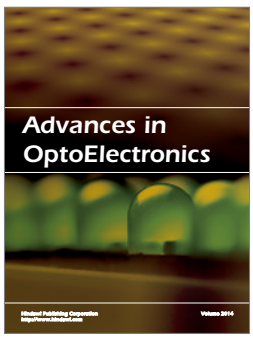

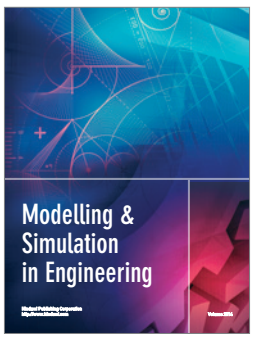

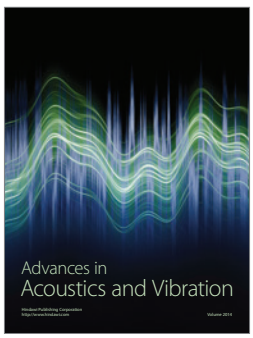

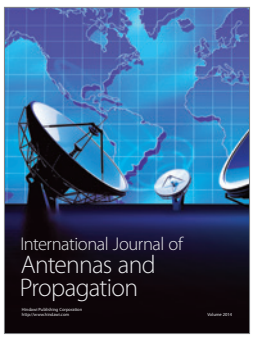

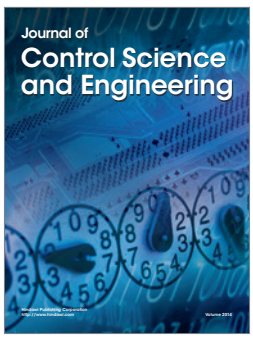

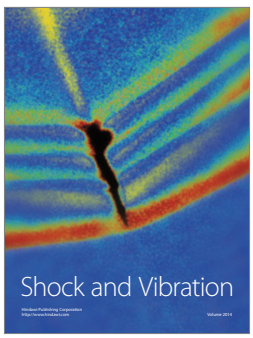

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