Research Article

High-Frequency and Low-Power Output Stages Based on FGMOS Flipped Voltage Follower

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Two new high-performance output stages are proposed. These output stages are basically designed by using a flipped voltage follower (FVF). The proposed low-power and low-voltage output stages have utilized the advantages of the FGMOS technology. They are characterized by low-power dissipation, reduced power supply requirement, and larger bandwidth. By using FGMOS-based FVF in place of conventional FVF, the linearity of the output stages has been highly improved. The small-signal analysis of FGMOS-based FVF is done to show the bandwidth enhancement of conventional FVF. The circuits are simulated to demonstrate the effectiveness using SPICE, in TSMC 0.25-micron CMOS device models. The simulation results show that the power supply requirement of the proposed output stages is highly reduced and bandwidths are extremely higher than the conventional circuits.

1. Introduction

The challenge of designing of high performance low-voltage and low-power analog circuits is increasing due to the scaling down of CMOS technology and the increasing demand for portable electronic equipments [1]. The speed of conventional analog integrated circuits is degrading on reducing the supply voltage for a given technology. To fulfill these requirements, the researchers are focusing on the development of new integrated circuits that have low voltage supply requirement, without any degradation in the performance.

One of the basic building blocks in analog signal processing circuits is voltage buffer, which is used to drive low-impedance loads (Figure 1(a)). The flipped voltage follower (FVF) [2] is a low-voltage operating buffer that can be used in different circuits in place of conventional voltage buffer very efficiently. A FVF circuit is shown in Figure 1(b).

A FVF cell has found increasing applications in areas where a voltage buffer is required. These applications include operational amplifier, current mirror, output stages, and arithmetic circuits and act as a basic building block in various analog circuits [2–7]. The advantages of FVF include low supply voltage requirement, almost unity gain, and high current-sinking capabilities [2].

Ramirez-Angulo et al. [3] have introduced an FVF which is based on FGMOS level shifter stage, shown in Figure 2. Due to its high swing and low voltage operation, the FGMOS-based FVF can be preferred over conventional FVF in many high-swing, low-power, and wideband analog integrated circuits.

Applications for communication systems require low power, low voltage, and high frequency output stages. The supply voltage and the power dissipation of output stage can be reduced by using floating gate technology. There are several attractive features of FGMOS such as it can incorporate tuneable mechanisms and work below the operational limits of supply voltage levels for a particular technology, without affecting the other characteristics of the system, and thus power dissipation is also lesser than the minimum power required for a MOS circuit of the same technology [8–13].

Usually buffers require an extra circuitry to achieve large bandwidth, which often increases power consumption. In this work, the FVF with floating gate level shifter [3] is used to replace the conventional FVF in different output stages, which have been investigated by Centurelli et al. in [14]. We have achieved high bandwidth of output stages, without

FIGURE 1: (a) Voltage follower and (b) flipped voltage follower.

FIGURE 2: FVF using floating gate level shifter [3].

affecting the gain of the system, and moreover the power consumption is highly reduced.

This paper is organized as follows. Section 2 covers the large signal analysis and small signal analysis of conventional FVF with a floating gate level shifter. Section 3 presents the proposed output stages based on FGMOS FVF. On the basis of simulation results, the performances of designed circuits are compared in Section 4. Finally, the conclusion is given in Section 5.

2. FVF with Floating Gate Level Shifter

2.1. Large Signal Analysis. The symbolic representation of two-input floating gate transistor, whose threshold voltage can be controlled by the values of capacitors, and its equivalent circuit are shown in Figures 3(a) and 3(b), respectively.

The input signal (V_1) and bias (V_2) are applied at gate G1 and G2, respectively. The drain current (I_D) of the FGMOS operating in ohmic region is given by [8, 9]

$$I_D = \beta \left[\left\{ \left(\frac{C_1}{C_{\text{Total}}} V_1 + \frac{C_2}{C_{\text{Total}}} V_2 + \frac{C_{\text{GD}}}{C_{\text{Total}}} V_{\text{DS}} \right) - V_T \right\} - \frac{V_{\text{DS}}}{2} \right] V_{\text{DS}}, \quad (1)$$

where β is the transconductance parameter, C_1 and C_2 are the capacitances associated with G1 and G2, $C_{\text{Total}} = C_1 + C_2 + C_{\text{GS}} + C_{\text{GD}} + C_{\text{GB}}$ is the total floating-gate (FG) capacitance, and V_T stands for the threshold voltage. The above equation can be simplified as

$$I_D = \beta \left(\frac{C_1}{C_{\text{Total}}} \right) \left[(V_1 - V_{T,\text{eff}}) V_{\text{DS}} - \frac{C_{\text{Total}}}{2C_1} V_{\text{DS}}^2 \right], \quad (2)$$

where effective threshold voltage ($V_{T,\text{eff}}$) is given by [8]

$$V_{T,\text{eff}} = V_T + \frac{C_2}{C_1} (V_T - V_2). \quad (3)$$

From (3), it is obvious that the reduction in $V_{T,\text{eff}}$ can be done by selecting $V_2 > V_T$ and $C_2 > C_1$. Hence, $V_{T,\text{eff}}$ is controllable and it depends on the values of C_1 and C_2 . The proposed output stage circuits utilize this property of the FGMOS transistor.

The control gates (G1 and G2) develop a floating gate voltage V_{FG} as a weighted sum of inputs voltages V_i , via a capacitive voltage divider. V_{FG} is given by [8]

$$V_{\text{FG}} = \left\{ \sum_{i=1}^N \left(\frac{C_i}{C_{\text{Total}}} \right) V_i + \left(\frac{C_{\text{GS}}}{C_{\text{Total}}} \right) V_S + \left(\frac{C_{\text{GD}}}{C_{\text{Total}}} \right) V_D + \left(\frac{C_{\text{GB}}}{C_{\text{Total}}} \right) V_B + \frac{Q_{\text{FG}}}{C_{\text{Total}}} \right\}, \quad (4)$$

FIGURE 3: (a) Schematic symbol of 2-input FGMOS transistor and (b) equivalent circuit of FGMOS transistor.

where V_X is the voltage at X terminal, C_{GS} , C_{GD} , and C_{GB} are the parasitic capacitances, C_i is capacitance at input terminal, C_{Total} is the total capacitance seen by floating gate and Q_{FG} refers to the amount of charge that has been trapped in floating gate during fabrication. Using (4) to find the floating gate voltage of FGMOS-based FVF (Figure 2) and an approximation given in [8], we obtain

$$V_{FG} \approx \left(\frac{C_1}{C_1 + C_2} \right) V_{D1} + \left(\frac{C_2}{C_1 + C_2} \right) V_{GND}, \quad (5)$$

or

$$V_{FG} = \left(\frac{C_1}{C_1 + C_2} \right) V_{D1}. \quad (6)$$

Hence, the voltage at drain terminal of M1 is

$$V_{D1} = \left(\frac{C_1 + C_2}{C_1} \right) V_{FG} = \left(1 + \frac{C_2}{C_1} \right) V_{FG}. \quad (7)$$

It is obvious from (7) that V_{D1} is level shifted by (C_2/C_1) .

2.2. Small Signal Analysis. The small signal model of FGMOS-based FVF is shown in Figure 4. The FGMOS-based FVF is analyzed to obtain the transfer function.

In the analysis, r_{o1} and r_{o2} are the resistances due to channel length modulation effect, C_{gs1} and C_{gs2} are the gate to source capacitances, and g_{m1} and g_{m2} are the transconductances of transistors M1 and M2, respectively. C_1 and C_2 are the capacitances associated with two different inputs of floating gate transistor M2, respectively, and R_b is the output impedance of the current source I_b .

On applying KCL at nodes (a), (b), and (c) in Figure 4, the obtained equations are

$$\begin{aligned} V_{out} \left(sC_{gs1} + g_{m1} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} \right) - V_{in} (g_{m1} + sC_{gs1}) \\ - \frac{V_{d1}}{r_{o1}} + g_{m2} \left(\frac{C_1}{C_2} \right) V_{d1} = 0, \end{aligned} \quad (8)$$

FIGURE 4: Small-signal equivalent model of FVF with floating gate level shifter.

$$V_{d1} \left(\frac{1}{R_b} + \frac{1}{r_{o1}} + sC_1 \right) - \frac{V_o}{r_{o1}} + g_{m1} (V_{in} - V_o) - sC_1 V_{g2} = 0, \quad (9)$$

$$V_{g2} (sC_T) = V_{d1} (sC_1), \quad (10)$$

where $C_T = C_1 + C_2 + C_{gs2}$.

Substituting the value of V_{g2} from (10) in (9), it gives

$$\begin{aligned} V_{d1} \left(\frac{1}{R_b} + \frac{1}{r_{o1}} + sC_1 \left(1 - \frac{C_1}{C_T} \right) \right) = V_o \left(\frac{1 + g_{m1}r_{o1}}{r_{o1}} \right) \\ - g_{m1}V_{in}. \end{aligned} \quad (11)$$

And, thus,

$$V_{d1} = \left(\frac{R_b C_T \{ V_o (1 + g_{m1}r_{o1}) - g_{m1}r_{o1}V_{in} \}}{C_T (r_{o1} + R_b) + sC_1 (C_T - C_1) r_{o1} R_b} \right). \quad (12)$$

FIGURE 5: Output stage based on FVF [15].

FIGURE 7: The proposed output stage based on floating gate FVF.

FIGURE 6: Class AB output stage based on FVF [14].

FIGURE 8: The proposed class AB output stage based on floating gate FVF.

Replacing V_{d1} by using (12) in (8), the transfer function is given by

$$A_V(s) = (r_{o1}r_{o2}(sC_{gs1} + g_{m1})X + g_{m1}r_{o1}r_{o2}R_b(g_{m2}r_{o1}C_1 - C_T)) \times (r_{o1}r_{o2}(sC_{gs1} + g_{m1})X + X(r_{o1} + r_{o2}) + g_{m1}r_{o1}r_{o2}R_b(g_{m2}r_{o1}C_1 - C_T) + r_{o2}R_b(g_{m2}r_{o1}C_1 - C_T))^{-1}, \quad (13)$$

where $X = C_T(r_{o1} + R_b) + sC_1r_{o1}R_b(C_T - C_1)$.

Assuming $r_{o1} = r_{o2} = r_o$, $C_1 = C_2 = C$, and $C_{gs1} = C_{gs2} = C_{gs}$, (13) transforms into

$$A_V(s) = \frac{a_2s^2 + a_1s + a_0}{a_2s^2 + (a_1 + \Delta a_1)s + (a_0 + \Delta a_0)}, \quad (14)$$

where

$$\begin{aligned} a_2 &= C_{gs}C(C_{gs} + C)r_o^3R_b, \\ a_1 &= r_o^2\{g_{m1}r_oR_bC(C_{gs} + C) + C_{gs}(r_o + R_b)(C_{gs} + 2C)\}, \\ \Delta a_1 &= 2CR_b(C_{gs} + C), \\ a_0 &= g_{m1}r_o^3(C_{gs} + 2C) + g_{m1}g_{m2}r_o^3R_bC, \\ \Delta a_0 &= \{g_{m2}r_o^2R_bC + r_oR_b(C_{gs} + 2C) + 2r_o^2(C_{gs} + 2C)\}. \end{aligned} \quad (15)$$

By definition, at $\omega = \omega_o$, $|A_V|^2 = 1/2$ [16], and thus

$$\frac{1}{2} = \frac{(a_0 - a_2\omega^2)^2 + (a_1\omega)^2}{((a_0 + \Delta a_0) - a_2\omega^2)^2 + ((a_1 + \Delta a_1)\omega)^2}. \quad (16)$$

The -3 dB frequency is

$$\omega_o = \frac{1}{a_2} \sqrt{\Delta a_1^2 + 2a_1\Delta a_1 + 2a_0a_2 - a_1^2 - 2a_2\Delta a_0}. \quad (17)$$

TABLE 1: Circuit parameters of simple FVF and FGMOS-based FVF.

Parameters	Values
Aspect ratio of M1	(10/0.25) μm
Aspect ratio of M2	(10/1) μm
Bias current I_{bias}	500 μA
FGMOS capacitors $C_1 = C_2$	175 fF
FGMOS resistors $R_1 = R_2$	10 G Ω

FIGURE 9: DC responses of simple and floating-gate-based FVF.

FIGURE 10: Frequency responses of simple and floating-gate-based FVF.

(Since the expression of the lower 3-dB frequency is too large, the symbols are used to represent it.) By placing the values of symbols, it can be easily observed that the lower 3-dB frequency of floating gate FVF is much greater than that of simple FVF [7].

To enhance the speed and reduce the power supply requirement, the wideband FGMOS-based FVF is used in conventional buffers [14] and is explained in the next section.

TABLE 2: Circuit parameters of conventional FVF-based output stage and proposed FVF-based output stage.

Parameters	Values
Aspect ratio of M1 and M2	(13/0.25) μm
Aspect ratio of M3	(100/0.5) μm
Aspect ratio of M4 and M5	(50/0.5) μm
Bias voltage $V_{\text{bias},p} = V_{\text{bias},n}$	0.3 V
Bias voltage V_b	0.2 V
FGMOS capacitors $C_1 = C_2$	175 fF
FGMOS resistors $R_1 = R_2$	10 G Ω

TABLE 3: Circuit parameters of conventional and proposed class AB FVF buffer.

Parameters	Values
Aspect ratio of M1 and M2	(2/0.25) μm
Aspect ratio of M3 and M4	(3/0.25) μm
Aspect ratio of M5 and M6	(15/0.25) μm
Aspect ratio of M7	(1/0.25) μm
Bias voltage V_{bias}	1 V
Bias voltage V_b	0.2 V
FGMOS capacitors $C_1 = C_2$	175 fF
FGMOS resistors $R_1 = R_2$	10 G Ω

3. Proposed High-Frequency and Low-Power Output Stages

In many analog circuits, it is required to drive the impedance by a voltage buffer like that in operational amplifiers. For low-power circuits, low-power voltage buffers are used as output stages. The FVF has overcome the drawbacks of conventional voltage buffers. It has low-power dissipation, large output signal swing, low settling time, and almost unity gain [2]. Moreover, class AB biasing can be employed to reduce power consumption without affecting the ability to drive large capacitive loads [14]. Figure 5 shows an output stage based on conventional FVF [15]. But a FVF will not work properly in class AB. Centurelli et al. [14] have developed an output stage which was based on FVF operating in class AB (Figure 6).

In this paper, we have introduced two output stages which are based on FVF with FGMOS level shifter. The proposed output stages are shown in Figures 7 and 8.

The output stage shown in Figure 8 operates in class AB. It is shown in Section 2.2 that a FVF with a floating gate level shifter has larger bandwidth in comparison to the conventional FVF. This motivates us to replace MOS transistor M2 by a two-input FGMOS transistor. Moreover, the proposed circuits have high linearity, low power consumption, and power supply requirement.

The effects and advantages of replacing conventional transistor by floating gate transistor can be easily observed through the simulation results.

TABLE 4: Simulation results of designed conventional and proposed circuits.

Simulated circuit	Power supply (V)	Output impedance (Ω)	Voltage gain	Power dissipation (mW)
Simple FVF	3.0	54.34	0.91	1.5
Conv. FGMOS-based FVF	1.0	65.09	0.95	0.5
Conv. FVF-based output stage	3.0	52.82	0.89	1.18
Prop. FVF-based output stage	0.8	51.45	0.91	0.0062
Conv. class AB FVF buffer	3.0	196.91	0.93	1.22
Prop. class AB FVF buffer	1.8	106.71	0.99	0.071

FIGURE 11: DC responses of conventional (shown by solid line) and proposed FVF-based output stage.

FIGURE 12: DC responses of conventional and proposed class AB FVF buffer.

4. Simulation Results

The designed circuits are simulated using PSPICE in TSMC 0.25 μm CMOS technology. The FGMOS circuits have been simulated by using the model given by EdgarSánchez-Sinencio [9].

In this work, the performance of a simple FVF and floating-gate-based FVF is compared. The circuit parameters of simple FVF and FGMOS-based FVF are given in Table 1.

It is obvious from the DC response (shown in Figure 9) that, by using floating gate transistor in place of MOS transistor, the linearity and gain of the system have been improved.

Figure 10 shows the frequency responses of these two circuits. The bandwidth is extended from 1.17 GHz to 4.78 GHz.

The paper has presented two new buffers that can be used as output stage in many analog and mixed-signal circuits. The circuit parameters of FVF-based output buffer and class AB output buffers are given in Tables 2 and 3, respectively.

The DC responses of the proposed and conventional buffer circuits are shown in Figures 11 and 12. The use of FGMOS technology has improved the linearity of the buffers to a large extent and power consumption is reduced. The frequency responses of the conventional and proposed buffers are shown in Figures 13 and 14.

FIGURE 13: Frequency responses of conventional and proposed FVF-based output stage.

FIGURE 14: Frequency responses of conventional and proposed class AB buffers.

The level shifting in output signal can be easily observed in the proposed circuits. The bandwidth has been largely enhanced by using floating-gate-based FVF. The comparative results are given in Table 4.

5. Conclusion

In this paper, two new low-power low-voltage and wideband output stages based on FVF with floating gate level shifter have been proposed. The use of floating gate technology provides the advantages of low-power consumption and low-power supply requirement. Moreover it gives a significant improvement in the bandwidth of the systems and the ability of the buffers to drive heavy capacitive loads by decreasing the output impedance. The simulation results have shown that the proposed buffers display good characteristics when compared with the reported works achieved so far. These improved buffer structures can be useful as output stage in many analog signal processing applications.

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