Research Article

A Novel Reconfigurable MB-OFDM UWB LNA Using Programmable Current Reuse

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This paper presents a design of a reconfigurable low noise amplifier (LNA) for multiband orthogonal frequency division multiplexing (MB-OFDM) ultra wideband (UWB) receivers. The proposed design is divided into three stages; the first one is a common gate (CG) topology to provide the input matching over a wideband. The second stage is a programmable circuit to control the mode of operation. The third stage is a current reuse topology to improve the gain, flatness and consume lower power. The proposed LNA is designed using $0.18\ \mu\text{m}$ CMOS technology. This LNA has been designed to operate in two subbands of MB-OFDM UWB, UWB mode-1 and mode-3, as a single or concurrent mode. The simulation results exhibit the power gain up to 17.35, 18, and 11 dB for mode-1, mode-3, and concurrent mode, respectively. The NF is 3.5, 3.9, and 6.5 and the input return loss is better than -12 , -13.57 , and -11 dB over mode-1, mode-3, and concurrent mode, respectively. This design consumes 4 mW supplied from 1.2 V.

1. Introduction

Ultra wideband (UWB) has many advantages over narrowband technology such as high data rate, low power, low complexity, and low cost technology. When The US Federal Communication Commission (FCC) recognized the potential advantages of UWB, it issued a report that allows UWB use for commercial communication systems in 2002, and its applications can operate in the unlicensed spectrum of 3.1–10.6 GHz [1]. UWB supports carrierless baseband signals such as impulse-radio IR-UWB, and it supports wideband with carrier such as multiband orthogonal frequency division multiplexing MB-OFDM UWB [2]. In MB-OFDM UWB systems, the spectrum from 3.1 to 10.6 GHz is divided into 14 subbands of 528 MHz as shown in Figure 1, which supports data rates from 53 to 480 Mbps [3, 4].

In order to roam across different subbands, devices that support multinet applications are required. There is a strong motivation on using single chip supports multiband and multiapplications, due to it provides wireless access for users anywhere and anytime. In such reconfigurable devices, the design of low noise amplifier (LNA) is a critical issue

because its has effects in the overall system and requirements as high gain, low noise figure (NF), and lower power consumption, with good input and output matching over each band of interest.

Recently, there are some schemes proposed to the multistandard LNAs like parallel, concurrent, wideband, and reconfigurable LNA. The first approach is the parallel architecture that employs multiple architectures for each band of interest [5]. However, this approach requires large area, different design for each band, and more time. The concurrent and wideband approaches provide multiband simultaneously [6] by providing the input matching, but this approaches pass the large interference the matching network; therefore, increasing the linearity is required [7, 8]. Recently, the reconfigurable approach presents to discrete band and/or concurrent bands [7] to solve the tradeoff between area, power, and cost. Many approaches present a continuous tuning like [8, 9]; it is good for narrowband applications, but it is not applicable for widebands.

This paper proposed a new reconfigurable MB-OFDM LNA for UWB systems. The proposed LNA reconfigured over dual widebands and it works as a discrete band or concurrent

FIGURE 1: Frequency spectrum of MB-OFDM UWB system.

FIGURE 2: Current reuse architecture.

based on the programmable part. This design based on CG topology to provide the input matching over wideband [10, 11], current reuse technique shown in Figure 2 used to provide high and flat gain, and low power consumption [12–14], and programmable circuit to select the band of operation. This paper is organized as follows, the demonstration of the proposed circuit, defect and solution of current reuse technique will be presented in Section 2. Section 3 discusses the simulation results of the proposed LNA. Finally, the conclusion is presented in Section 4.

2. Circuit Design of the Proposed Reconfigurable MB-OFDM UWB LNA

The proposed LNA was designed by a standard $0.18\mu\text{m}$ CMOS process. Figure 3(a) shows the schematic of the LNA. This circuit consists of three stages distinguished by three different blocks in Figure 3(a). The first one, input matching stage in block-1 in Figure 3(a), the CG topology used to control the input matching over wideband [11, 15] where the input impedance at L_S resonated with the gate-to-source parasitic capacitance of C_{gs1} of M_1 is $Z_{in} = 1/g_{m1}$, where g_{m1} is the transconductance of transistor M_1 . Therefore, the matching bandwidth can be calculated by

$$f_{BW} = \frac{1}{2\pi C_{gs1} (1/g_{m1})} = \frac{g_{m1}}{2\pi C_{gs1}} \quad (1)$$

TABLE 1: Look-up table of programmable circuit.

M_{S1}	M_{S2}	BW (GHz)	f_0 (GHz)	Mode
0	0	—	—	—
0	1	0.528	3.432	Single
1	0	0.528	4.488	Single
1	1	≈ 1.4	3.96	Concurrent

hence, by controlling g_{m1} the input impedance can be matched to 50Ω at resonance.

Second stage is the programmable switches in block-2 in Figure 3(a), actually this stage is proposed to achieve two main tasks. The first task is used to select the branch that will provide the desired band, consequently, the selected band depends on Table 1, where f_0 is the center frequency of the selected mode. The other task is used to solve current reuse defect, without using this stage the control of this circuit can be made by transistor M_{2a} and M_{2b} , but when one of them is OFF, n_1 and n_2 nodes will be shorted, thereby the overall circuit performance will be effected.

To solve this problem the programmable circuit is proposed, when transistor M_{S2} is OFF as shown in Figure 3(b) n_1 and n_2 nodes will be disconnected.

Finally, the current reuse stage in block-3 in Figure 3(a), is used to achieve high and flat gain, and lower power consumption. This architecture was simplified in Figure 2 and it consists of series inductor L_1 and shunt capacitor C_1 connected to DC cascode transistors M_1 and M_2 . C_1 is used to resonate with gate-to-source parasitic capacitance of M_2 , C_{gs2} , while L_1 is selected large in the desired bandwidth to provide high impedance path to block RF signal. Furthermore, when the capacitance C_o is selected large, the transistors M_1 and M_2 act as two common source (CS) cascaded stage at high frequency [12–14].

3. Simulation Results

Design of the proposed reconfigurable MB-OFDM UWB LNA was carried out using Spectre simulator from Cadence Design Suite. The proposed circuit consumes 3.32 mA from 1.2 V supply when it works in single mode, but when it works in concurrent mode it consumes 3.39 mA. The simulation results for S-parameters and NF are illustrated in Figure 4 and Figure 5.

Figure 4(a) shows the simulated input return loss S_{11} for different frequency bands based on Table 1. As noticed,

FIGURE 3: Circuit design of the proposed reconfigurable MB-OFDM UWB LNA: (a) schematic of proposed reconfigurable MB-OFDM UWB LNA and (b) operation of the proposed LNA when M_{S1} ON and M_{S2} OFF.

S_{11} is less than -12 , -13.57 , and -11 dB for UWB mode-1 with center frequency 3.432 GHz, UWB mode-3 with center frequency 4.488 GHz, and concurrent mode with center frequency 3.96 GHz, respectively. These results depict the input matching network of the proposed LNA under -10 dB, the reason behind this due to CG topology and selection of appropriate value of L_s to resonate with C_{gs1} , so the proposed design has a good input matching.

Figure 4(b) presents the reverse isolation S_{12} between output and input ports over bands of interest, where it is less than -50.5 , -44.2 , and -52 dB for mode-1, mode-3, and concurrent mode, respectively. Also the better isolation comes from CG topology, where the input isolated from the output of this topology.

Figure 4(c) illustrates the voltage gain S_{21} of the proposed LNA. As depicted, the proposed LNA achieves 17.35, 18, and 11 dB for mode-1, mode-3, and concurrent mode, respectively. The high gain of this LNA is due to current reuse, where the overall transconductance of this design is $g_m = g_{m1}g_{m2}$. However, the gain of concurrent mode is lower than single mode, due to the parallel resistance of branches (output resistance of M_{2a} , r_{o2a} series with output resistance of M_{S1} , and r_{oS1} are parallel with output resistance of M_{2b} , r_{o2b} series with output resistance of M_{S2} , and r_{oS2}). Figure 4(d) shows the output return loss S_{22} of the reconfigurable LNA where it is under -14.9 , -9.6 , and -14.2 dB for all modes.

The good output matching was achieved due to the selection of appropriate values for output matching network (M_2 , L_{g2} , L_{d2} , L_{out} , C_{out} , and C_o). The simulated NF versus bands of interest is shown in Figure 5. As noticed, NF of the proposed LNA achieves 3.49–3.53, 3.9–3.93, and 6.29–6.8 dB for mode-1, mode-3, and concurrent mode, respectively. The high NF of concurrent mode is due to the number of transistors that are used in this mode.

The performance of the proposed LNA and a comparison with existing architectures are summarized in Table 2. As shown in this table, the proposed LNA provides discrete tuning and concurrent, while the existing techniques either provide discrete, concurrent, or continuous tuning. The voltage gain S_{21} for the proposed architecture is lower than [8, 9, 16], because they use the cascode and cascade topologies for that they consume higher power when compared with the proposed reconfigurable LNA.

4. Conclusion

A reconfigurable LNA for MB-OFDM UWB receivers is proposed. This LNA works in three modes of operation based on programmable current reuse technique. The detailed operation of the proposed reconfigurable LNA including input matching topology (CG), programmable switches circuit, high gain and low power technique (current reuse),

FIGURE 4: S-Parameter results of reconfigurable LNA over multibands: (a) input reflection coefficient S_{11} , (b) reverse isolation S_{12} , (c) voltage gain S_{21} , and (d) output reflection coefficient S_{22} .

TABLE 2: The performance of the proposed LNA and comparison with existing architecture.

	Tech. CMOS	BW (GHz)	V_{dd} (V)	S_{11} (dB)	S_{22} (dB)	S_{21} (dB)	NF (dB)	Power (mW)	Topology
[7]	0.13	2.8, 3.3, 4.6	1.2	< -18	—	14.2–16	1.7–3.7	6.4	S*
		2.05, 5.65		< -8.6	—	14.9	4–4.8		C**
		4.3–10.8		—	—	3–15.6	4–5.3		UWB
[8]	0.13	1.9–2.4	1.2	< -13	—	14–10	3.2–3.7	17	Con***
[9]	0.13	3.4–3.6	1.2	< -18	< -15.3	20.9–21.3	< 1.8	16	S
		4.2–4.8	1.2	< -15	< -14.5	19.2–20.7	< 2.3		
[15]	0.18	0.9, 1.5, 2.4	1.8	< -10	—	15–19	1.9–4.5	30	C
[16]	0.13	1.8–2.4	1.2	< -12	—	26–28	3.2–3.4	9.6	
This work	0.18	3.168–3.696	1.2	< -12.04	< -14.9	15.8–17.35	3.49–3.53	4	S
		4.224–4.752		< -13.57	< -9.6	16–18	3.9–3.93		S
		3.432–4.488		< -11	< -14.2	10.25–11	6.28–6.8		C

*S: Single mode; **C: Concurrent mode; ***Con: continuous.

FIGURE 5: Noise figure NF.

and the noise performance of this circuit was presented. The proposed LNA operates by 1.2 V supply and consumes 3.32 mA for single mode (UWB mode-1 or mode-3) and 3.39 mA for concurrent mode. Finally, it has been designed by 0.18 μm CMOS process.

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