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Research Article

A Low Power Voltage Controlled Oscillator Design

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The performance of voltage controlled oscillator (VCO) is of great importance for any telecommunication or data transmission network. Here, voltage controlled oscillators (VCOs) using three-transistor NAND gates have been designed. New delay cell with three-transistor NAND gate has been used for designing the ring based VCO circuits. Three-, five-, and seven-stage VCOs have been proposed. Output frequency has been controlled with supply voltage variation from 1.8 V to 2.4 V. Three stage VCO shows output frequency variation in the range of 3.2909 GHz to 4.2280 GHz whereas power consumption varies in the range of 335.4071 μW to 486.1816 μW. Five-stage VCO depicts frequency in the range of 1.9406 GHz to 2.5769 GHz with power consumption variation from 559.0118 μW to 810.3027 μW. Moreover a seven-stage VCO shows frequency variation from 1.3984 GHz to 1.8077 GHz. Power consumption of seven-stage VCO varies from 782.6165 μW to 1134.400 μW. Phase noise results for these VCOs have also been obtained. Power consumption, output frequency, and phase noise results of proposed circuits have been compared with earlier reported circuits, and the proposed circuits show significant improvements.

1. Introduction

Oscillators are the most fundamental blocks in various communication systems. With each generation of communication and microprocessor technology data rates are increasing at a very fast pace. In modern high performance systems phase-locked loops (PLLs) are the commonly used circuit component with wide application in frequency synthesis, clock, and data recovery [1–3]. PLL block contains a phase detector, a charge pump, a loop filter, and voltage controlled oscillator circuit. VCO is the major part of PLL circuit and it affects the system performance in terms of power consumption and noise performance. In modern VCO designs power consumption and high output frequency range have become important performance metrics. Two widely used VCO types are LC tank and CMOS ring based circuits. Combination of capacitor and inductor on integrated circuits consumes large layout area in LC tank based VCO designs [4–6]. CMOS ring based oscillators show advantages due to ease of controlling the output frequency and nonrequirement for on chip inductors [7, 8]. With the beginning of very large scale integration (VLSI) technology CMOS based VCOs are more accepted in PLL systems. These are also easier to integrate and provide wide tuning range. Further, with the rising demand of portable devices like cellular phones, notebooks, and personal communication devices, the need for power saving has also increased many times. Power consumption in very large scale integration (VLSI) systems includes dynamic, static power and leakage power consumption. Total power consumption in any CMOS circuit is given as

$$P_{\text{total}} = \alpha C_L V_{dd}^2 f + I_{\text{sc}} V_{dd} + I_{\text{sub}} V_{dd} + I_{\text{gateleakage}} V_{dd}, \quad (1)$$

α is the switching activity, C_L is the capacitance of the load, f is the clock frequency, and V_{dd} is the supply voltage. I_{sc} is the short circuit current, which flows directly from the power supply to ground terminal when NMOS subnetwork and PMOS subnetwork conduct simultaneously. I_{sub} is the leakage current which results from substrate injection and subthreshold effects. The reverse biased p-n junction current is the static dissipation due to reverse biased diode leakage between the diffusion regions, wells, and substrate. $I_{\text{gateleakage}}$ is the gate leakage current which arises from gate oxide which is mostly dependant on gate oxide thickness. The first two components in (1) represent the dynamic power consumption and the remaining two components show static power consumption. In ring based oscillator design output of last stage is fed back to input of first stage. A VCO block diagram with single ended N-delay inverter stages is shown in Figure 1.

Table 1: Results for NAND delay based VCOs.

Control voltage (V)	Three-stage VCO		Five-stage VCO		Seven-stage VCO	
	Output frequency (GHz)	Power consumption (μW)	Output frequency (GHz)	Power consumption (μW)	Output frequency (GHz)	Power consumption (μW)
1.8	3.2909	335.4071	1.9406	559.0118	1.3984	782.6165
1.9	3.3964	359.4469	2.0288	599.0782	1.4401	838.7095
2.0	3.5444	383.8849	2.0959	639.8081	1.5010	895.7314
2.1	3.7092	408.7571	2.2106	681.2619	1.5954	953.7666
2.2	3.9342	434.0872	2.3065	723.4787	1.6432	1012.900
2.3	4.1088	459.8914	2.3716	766.4857	1.7290	1073.100
2.4	4.2280	486.1816	2.5769	810.3027	1.8077	1134.400

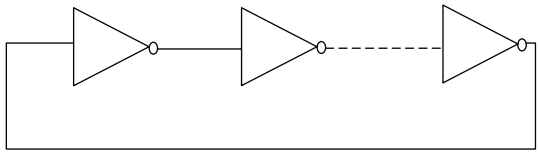


Figure 1: Single ended VCO.

The ring structure must provide a phase shift of 2π and unity voltage gain for oscillation occurrence. Each delay cell should provide a phase shift of π/N, where N is the total number of delay stages. The remaining π phase shift is provided by dc inversion of the inverter delay cells. In single ended oscillator designs the odd numbers of delay stages are required for dc inversion. Frequency of oscillation of VCO designed with N-single ended delay stages is given by $f_o = 1/2Nt_d$, where N is the total number of delay stages and t_d is delay of each stage [9, 10]. Different types of delay cells have been reported in the literature for oscillator design including multiple-feedback loops, dual-delay paths, and single ended delays [11–20]. Delay cells have been implemented by different approaches like inverter stages, latches, cross-coupled cells and so forth. Delay stages are the fundamental building blocks in any VCO design and improved design of these delay cells affects the overall performance of VCO design. In the present work a new delay cell has been designed considering the importance of power consumption and frequency range.

The paper is organized as follows: in Section 2, a three-transistor NAND gate has been discussed. Further, three-, five-, and seven-stage VCOs have been designed with NAND delay cell. In Section 3 results of proposed circuits have been described and compared with the earlier circuits. Finally conclusions have been presented in Section 4.

2. Circuit Description

The output frequency of ring VCO depends on the delay provided by each inverter delay cell. In the proposed designs delay cells based on three-transistor NAND gates are used. Inverter operation has been obtained by three-transistor NAND gate as shown in Figure 2. The circuits have been designed in 0.18 μm CMOS technology with supply voltage of 1.8 V. Supply voltage/control voltage has been varied from 1.8 V to 2.4 V to obtain the different output frequency

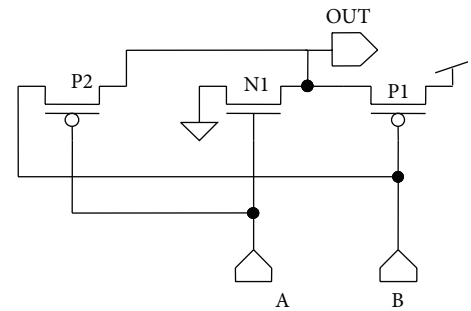


Figure 2: Three-transistor NAND gate.

components. Direct path between V_{dd} and ground has been eliminated in the delay cells, due to which leakage power is reduced and the designs are power efficient.

NAND delay stage is made up of two PMOS transistors and one NMOS transistor. Out of two input terminals of NAND gate, one is connected to logic 1 (i.e., 1.0 V) and feedback signal is applied to the other terminal. This circuits works as inverter without having direct path between V_{dd} and ground with saving in power consumption. The gate lengths of all three transistors have been taken as 0.18 μm. Width (W_n) of NMOS transistor (N1) has been taken as 0.25 μm. Width (W_p) of transistors P1 and P2 has been taken as 1.25 μm. Output frequency has been controlled by varying the supply voltage (V_{dd}) of NAND delay stages. Three- and five-stage VCOs have been shown in Figures 3(a) and 3(b). Seven-stage VCOs have also been designed with the same concept.

The proposed NAND gate has only three transistors so the design is more power efficient and requires less area as compared to conventional four-transistor NAND or NOR gates. The proposed NAND gate design is based on pass transistor logic which has reduced internal capacitance and is suitable for power efficient circuits [15]. In NAND gate design direct connection to V_{dd} is eliminated and there is only one NMOS transistor connected to ground so the design is power efficient as compared to that implemented with conventional gates.

3. Results and Discussions

Simulations have been carried out using SPICE based on TSMC 0.18 μm technology with supply voltage variations from 1.8 V to 2.4 V. Table 1 shows the results of power

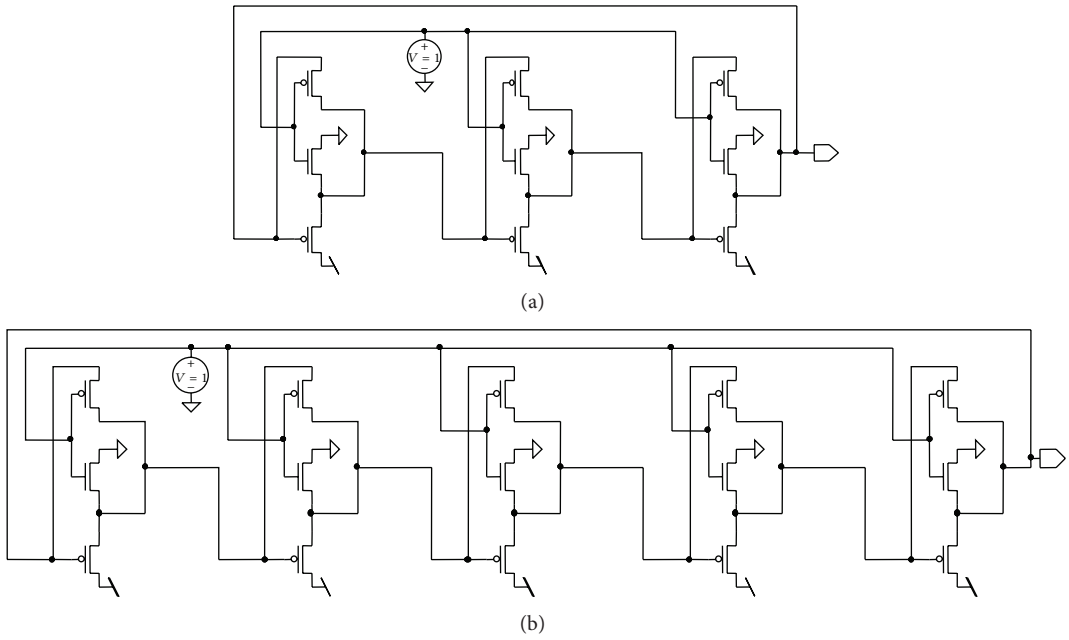


Figure 3: (a) Three-stage VCOs (b) Five-stage VCO.

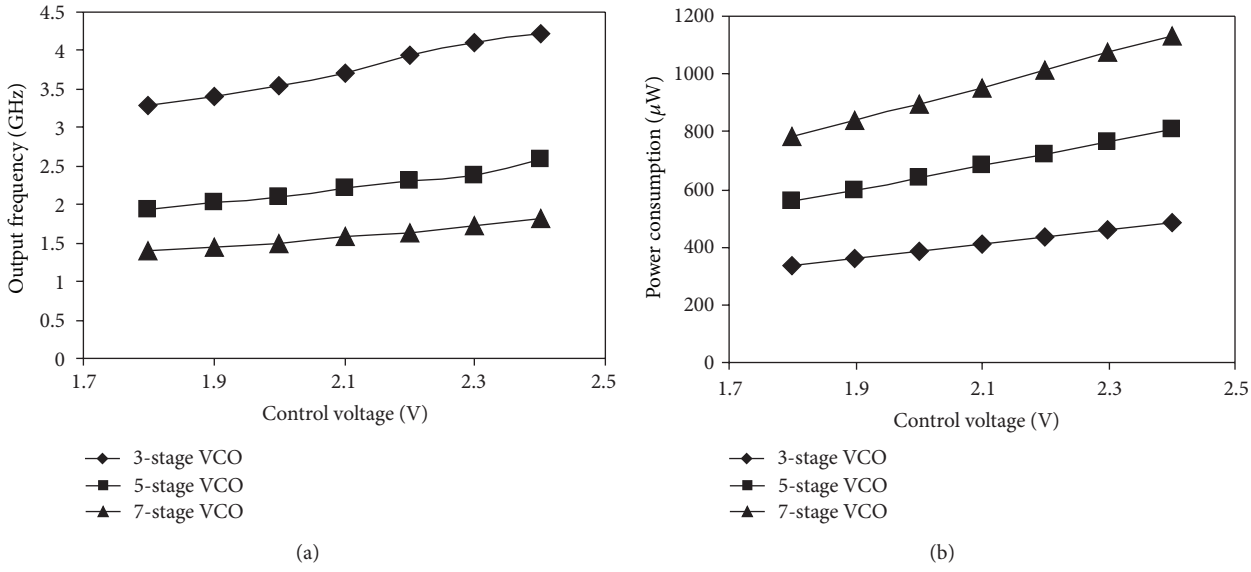


Figure 4: (a) Frequency and (b) power consumption variations of three-, five-, and seven-stage VCOs.

consumption and output frequency for three-, five-, and seven-stage VCOs.

Output frequency of three-stage VCO shows variation from 3.2909 GHz to 4.2280 GHz with power consumption variation from 335.4071 μW to 486.1816 μW. In five-stage ring VCO frequency varies from 1.9406 GHz to 2.5769 GHz with power consumption variation from 559.0118 μW to 810.3027 μW. Finally, in seven-stage ring VCO frequency varies from 1.3984 GHz to 1.8077 GHz with power consumption variation from 782.6165 μW to 1134.400 μW. Figures 4(a) and 4(b) show frequency and power consumption variation for three-, five-, and seven-stage VCOs. Figure 5 shows output waveforms for three-, five-, and seven-stage NAND VCOs at supply voltage of 1.8 V.

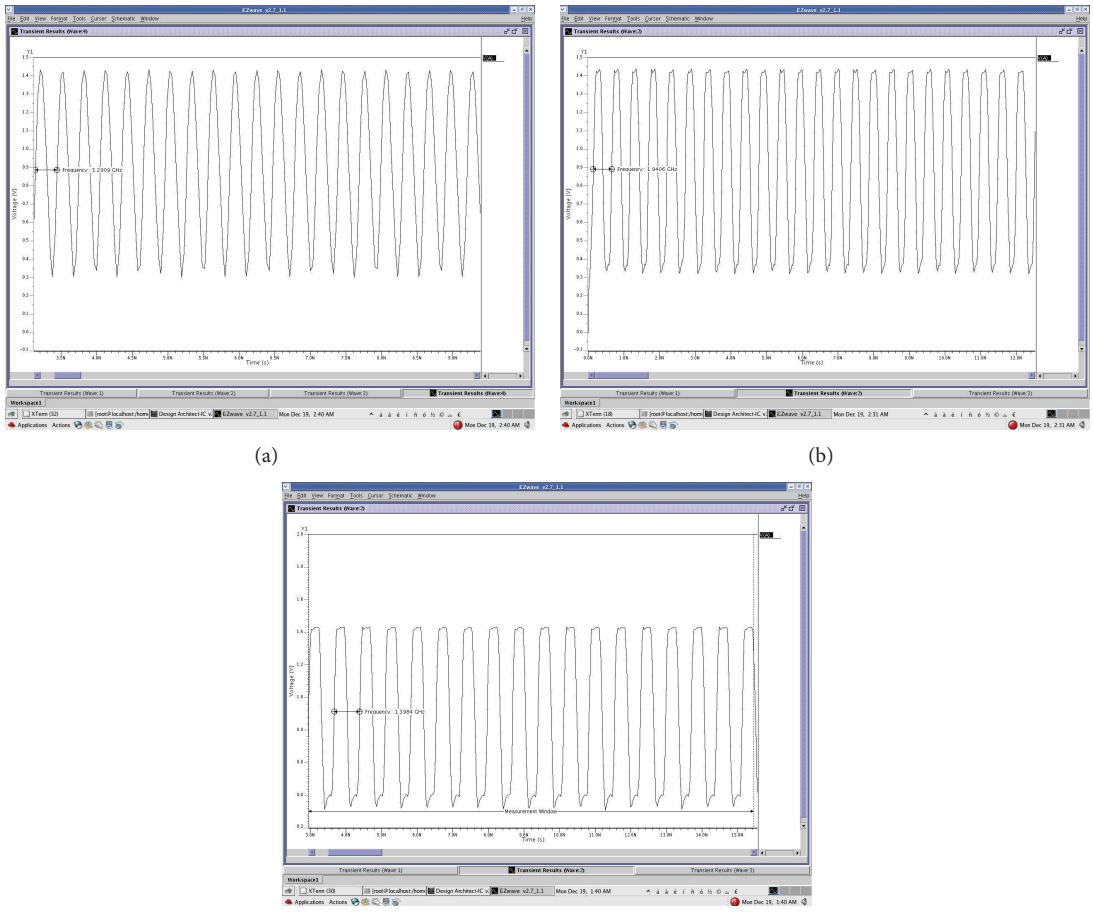
Table 2

VCO circuit	Phase noise (dBc/Hz)	Control voltage
3-stage NAND VCO	−80.9461 at 1 MHz	1.8 V
5-stage NAND VCO	−84.5595 at 1 MHz	1.8 V
7-stage NAND VCO	−86.6507 at 1 MHz	1.8 V

Table 2 shows results of phase noise performance for three-, five-, and seven-stage ring VCOs designed with

Table 3: Comparison of VCO performances.

VCO designs	Operating frequency (GHz)	VDD (V)	Technology (μm)	Power consumption	Phase noise (dBc/Hz)
[4]	2.17–2.73	0.9	0.18	2.7 mW	−122.3at 1 MHz
[8]	0.39–1.41	1.8	0.18	12.5 mW	−80 at 600 KHz
[11]	0.12–1.3	0.5	0.18	0.085 mW	—
[14]	1.57–3.57	1.8	0.090	16.8 mW	−90.01 at 600 kHz
[16]	0.65–1.6	1.8	0.18	39 mW	−108 at 0.2 MHz
Present work 3 stages	3.2909–4.2280	1.8	0.18	335.4071–486.1816 μW	−80.9461 at 1 MHz
Present work 5 stages	1.9406–2.5769	1.8	0.18	559.0118–810.3027 μW	−84.5595 at 1 MHz
Present work 7 stages	1.3984–1.8077	1.8	0.18	782.6165–1134.400 μW	−86.6507 at 1 MHz



(a) (b)

(c)

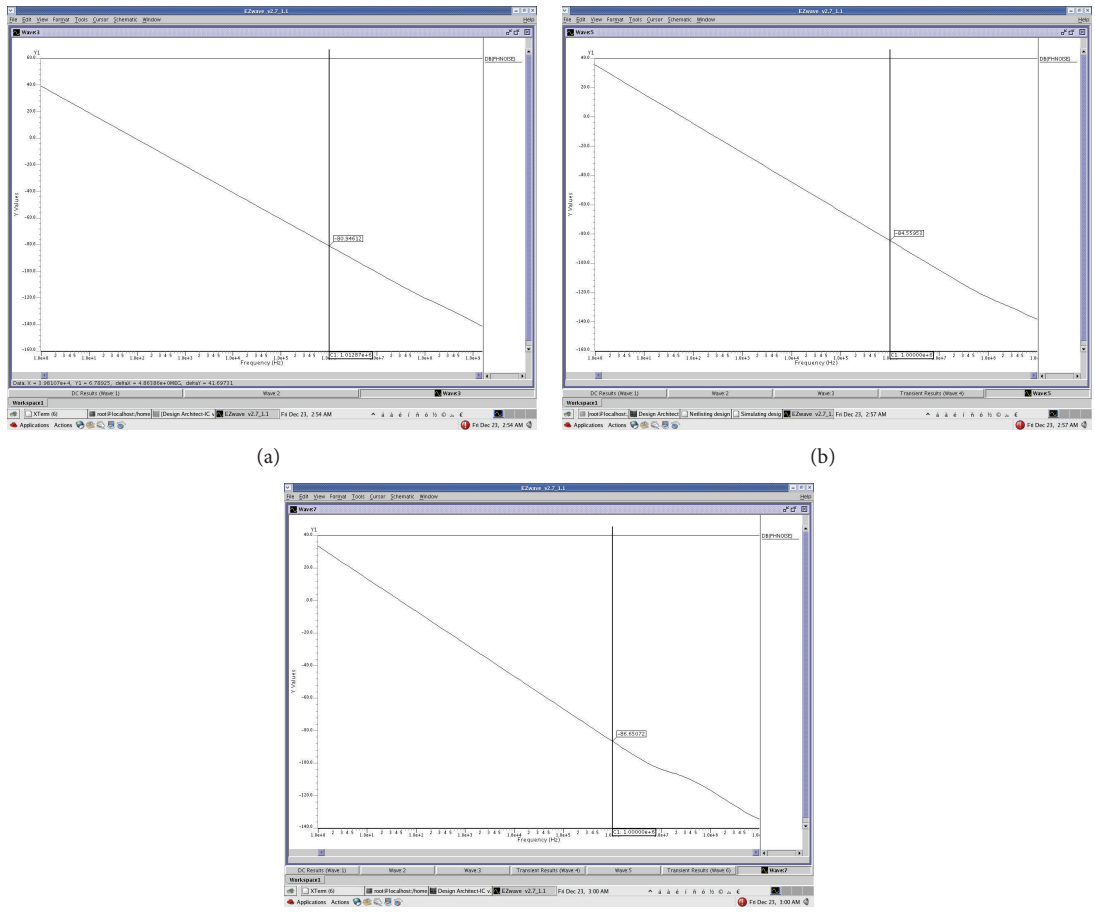
Figure 5: Output waveforms: (a) 3-stage VCO, (b) 5-stage VCO and (c) 7-stage VCO.

NAND delay cells. Figures 6(a), 6(b), and 6(c) shows phase noise at 1 MHz offset for three-, five-, and seven-stage VCOs.

In the reported circuits, power consumption is showing upward trend with increase in number of delay stages whereas output frequency is showing downward trend. The number of stages may be decreased or increased depending upon the application and requirement for output frequency range. A comparison with earlier reported circuits in terms of power consumption and output frequency range is given in Table 3. The proposed circuits show superior performance in terms of power consumption and output frequency range than the compared circuits.

4. Conclusions

In the reported work CMOS ring VCO designs have been improved with three-transistor NAND gates. Three-, five- and seven-stage VCOs have been reported with reduced



(a) (b)

(c)

Figure 6: Phase noise for (a) 3-stage VCO, (b) 5-stage VCO, and (c) 7-stage VCO.

power consumption. Three-stage VCO shows frequency variation in the range of 3.2909 GHz to 4.2280 GHz. Five-stage NAND delay based VCO provides output frequency from 1.9406 GHz to 2.5769 GHz. Finally the VCO designed with seven-stage NAND delay cells depicts frequency variation from 1.3984 GHz to 1.8077 GHz. Phase noise performances of proposed circuits also show good agreement with earlier circuits. Three- and five-stage VCOs show phase noise of −80.9461 dBc/Hz and −84.5595 dBc/Hz, respectively with the offset of 1 MHz. Finally the seven-stage VCO shows phase noise of −86.6507 dBc/Hz. The proposed designs have been compared with the previously reported design and our approach shows significant power saving with wide tuning range.

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