Research Article

OTRA Based Voltage Mode Third Order Quadrature Oscillator

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Two topologies of operational transresistance (OTRA) based third order quadrature oscillators (QO) are proposed in this paper. The proposed oscillators are designed using a combination of lossy and lossless integrators. The proposed topologies can be made fully integrated by implementing the resistors using matched transistors operating in linear region, which also facilitates electronic tuning of oscillation frequency. The nonideality analysis of the circuit is also given and for high frequency applications self-compensation can be used. Workability of the proposed QOs is verified through PSPICE simulations using 0.5 μm AGILENT CMOS process parameters. The total harmonic distortion (THD) for both the QO designs is found to be less than 1%.

1. Introduction

Quadrature oscillators (QO) produce outputs having a phase difference of 90°. The phase-locked sine-cosine relationship of QO has useful applications in the field of telecommunications where the modulation scheme utilizes both in-phase and quadrature components, such as single-sideband generators and quadrature mixers [1]. The QOs are also used extensively in the field of instrumentation and power electronics [2]. For these applications low value of total harmonic distortion (THD) is an essential requirement as higher harmonics have detrimental effects on electrical equipment. These higher order harmonics can also interfere with communication transmission lines since they oscillate at the same frequencies as the transmit frequency. If left unchecked, increased temperature and interference can greatly shorten the life of electronic equipment and cause damage to power systems.

It is well known that higher order networks as compared to lower order circuits provide better accuracy, frequency response, and distortion performance [3, 4]. However, it has been observed that higher order QO designs have not been explored much, as only a few third order QOs [1, 3–16] have appeared in literature in recent years. A careful observation suggests that the reported QO designs are based on forming closed loop using (i) two lossy and one lossless integrators [3–5], (ii) one lossy and two lossless integrators [8], (iii) a second order low pass filter followed by an integrator [1, 6, 7, 10–16], and (iv) three low pass filters and gain feedback around the loop [9]. These topologies are designed using second generation current conveyor (CCII) [1, 6], second generation current-controlled conveyor (CCCII) [7–9], differential voltage current conveyor (DVCC) [10], op-amp [5], operational transconductance amplifier (OTA) [3], current difference transconductance amplifier (CDTA) [4, 11], operational transresistance amplifier (OTRA) [12], and current-controlled current difference transconductance amplifier (CCCDTA) [13]. The structure proposed in [15] uses differential difference current conveyor (DDCC) and OTA whereas design of [16] is based on CCCDTA and OTA.

The OTRA is a current input voltage output device [17]. Being a current processing block, it inherits all the advantages of current mode techniques [12] and provides voltage output at low impedance which can readily be used to drive voltage input circuits without increasing component count. An extensive literature review suggests though a large number of OTRA based second order QOs [17–21] are available in literature, yet only a single third order QO topology using...
OTRA \[12\] is reported. This QO design is based on forming a closed loop using a second order low pass filter followed by an integrator.

In this paper two topologies of third order QO based on OTRA have been presented which use the scheme of lossy and lossless integrators. One of the proposed circuits makes use of one inverting lossy and two lossless integrators connected in a feedback forming closed loop whereas the other configuration uses one lossless and two lossy integrators to form closed loop. The proposed structures can be made fully integrated by implementing the resistors using matched transistors operating in linear region and can be tuned electronically.

2. Circuit Description

The OTRA is a high gain, current input voltage output analog building block \[17\]. The input terminals of OTRA are internally grounded, thereby eliminating response limitations due to parasitic capacitances and resistances and hence is a suitable choice for high frequency applications. The circuit symbol of OTRA is shown in Figure 1 and the port characteristics are given by (1), where $R_m$ is transresistance gain of OTRA:

\[
\begin{bmatrix}
V_p \\
V_n \\
V_O
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 \\
0 & 0 & 0 \\
R_m & -R_m & 0
\end{bmatrix}
\begin{bmatrix}
I_p \\
I_n \\
I_O
\end{bmatrix}.
\]  

(1)

For ideal operations the $R_m$ of OTRA approaches infinity and forces the input currents to be equal. Thus OTRA must be used in a negative feedback configuration \[22\].

2.1. Circuit I. The first QO topology is shown in Figure 2. It uses two lossless integrators and a lossy inverting integrator in the feedback forming a closed loop resulting in loop gain of the system as $A(s)\beta(s)$, where $A(s)$ is forward path gain involving OTRA2 and OTRA3 and $\beta(s)$ is feedback gain involving OTRAI.

The criterion for oscillations \[23\] to occur is given by

\[1 - A(s)\beta(s) = 0.\]  

(2)

If this criterion is satisfied, the closed loop system will result in two quadrature phase oscillations, available at nodes 1 and 2. Routine analysis of the circuit of Figure 2 results in the following characteristic equation:

\[s^3C_1C_2C_3R_2R_3 + \frac{s^2C_2C_3R_2R_3}{R_4} + sc_3 \frac{R_3}{R_5} + \frac{1}{R_1} = 0.\]  

(3)

From this characteristic equation the condition of oscillation (CO) and frequency of oscillation (FO) can be found to be

\[\frac{1}{2\pi} \sqrt{\frac{1}{C_1C_2R_2R_3}},\]  

(4)

CO:

\[R_4R_5 = R_1R_3,\]  

(5)

The FO can be adjusted to desired value through $R_2$ and proper selection of resistors $R_1$, $R_3$, and $R_4$ would satisfy the CO.

2.2. Circuit II. The second proposed QO configuration is shown in Figure 3 which makes use of two lossy and one lossless integrators, all in inverting mode.
The characteristic equation of the Circuit II can be deduced as

\[ s^3 C_1 C_2 C_3 R_3 + s^2 \left( \frac{C_2 C_3 R_3}{R_4} + \frac{C_1 C_3 R_3}{R_5} \right) + \frac{s C_3 R_3}{R_4 R_5} + \frac{1}{R_1 R_2} = 0 , \]  

(6)

**FO:**

\[ f = \frac{1}{2\pi} \sqrt{\frac{1}{C_1 C_2 R_4 R_5}} . \]  

(7)

**CO:**

\[ R_1 R_2 R_3 C_3 \left[ R_4 C_1 + R_5 C_2 \right] = R_2^2 R_3^2 C_1 C_2. \]  

(8)

By suitable selection of \( R_4 \) and \( R_5 \) the FO can be adjusted to desired value and proper selection of resistors \( R_1, R_2, \) and \( R_3 \) results in desired CO.

The current differencing property of the OTRA makes it possible to implement the resistors connected to the input terminals of OTRA, using MOS transistors with complete nonlinearity cancellation [17]. Each resistor requires two matched n-MOSFETs connected in a manner as shown in Figure 4 which represents a typical MOS implementation of resistance connected at negative input of OTRA.

Symbols “\( \text{p} \)” and “\( \text{n} \)” represent the noninverting and the inverting terminals of the OTRA. As can be seen from the figure, the voltages at the drain and the source terminals for both MOSFETs are equal. On taking the difference of the currents flowing in the two transistors, the nonlinearity gets cancelled out. The resistor value realized can be expressed as

\[ R = \frac{1}{K_N (V_a - V_b)} , \]  

(9)

where

\[ K_N = \mu C_{OX} \frac{W}{L} . \]  

(10)

\( K_N \) needs to be determined for the transistors being used to implement the resistors and \( \mu, C_{OX}, \) and \( W/L \) represent standard transistor parameters. The MOS based implementations of Circuit I and Circuit II are shown in Figures 5 and 6, respectively.

### 3. Nonideal Analysis

The output of the QO may deviate due to nonideality of OTRA in practice. Ideally the transresistance gain \( R_m \) is assumed to approach infinity. However, practically \( R_m \) is a frequency dependent finite value. Considering a single pole model for the transresistance gain, \( R_m \) can be expressed as

\[ R_m (s) = \left( \frac{R_0}{1 + (s/\omega_0)} \right) , \]  

(11)

where \( R_0 \) is dc transresistance gain. For high frequency applications the transresistance gain \( R_m (s) \) reduces to

\[ R_m (s) = \left( \frac{1}{s C_p} \right) , \]  

(12)
where
\[ C_p = \frac{1}{R_0 \omega_0}. \] (13)

Taking this effect into account (3) modifies to
\[
s^3 \left( c_1 + c_p \right) \left( c_2 + c_p \right) \left( c_3 + c_p \right) R_2 R_3
+ s^2 \left( c_2 + c_p \right) \left( c_3 + c_p \right) \frac{R_2 R_3}{R_4}
+ s \left( c_3 + c_p \right) \frac{R_3}{R_5} + \frac{1}{R_1} = 0. \] (14)

From (14) it is found that FO for Circuit I changes to
\[ f = \frac{1}{2\pi} \sqrt[4]{\frac{1}{(C_1 + C_p)(C_2 + C_p) R_2 R_3}}. \] (15)

Due to nonideality effect of OTRA (6) changes to
\[
s^3 \left( c_1 + c_p \right) \left( c_2 + c_p \right) \left( c_3 + c_p \right) R_3
+ s^2 \left( c_2 + c_p \right) \left( c_3 + c_p \right) \frac{R_3}{R_4} + \left( c_1 + c_p \right) \left( c_3 + c_p \right) \frac{R_3}{R_5}
+ s \left( c_3 + c_p \right) \frac{R_3}{R_4 R_5} + \frac{1}{R_1 R_2} = 0. \] (16)

The characteristic equation represented by (16) results in modified FO for Circuit II and is expressed as
\[ f = \frac{1}{2\pi} \sqrt[4]{\frac{1}{(C_1 + C_p)(C_2 + C_p) R_4 R_5}}. \] (17)

The effect of \( C_p \) can be eliminated by preadjusting the values of capacitors \( C_1, C_2, \) and \( C_3 \), thus achieving self-compensation.

4. Simulation Results

The proposed QO is verified through simulations using the CMOS implementation of the OTRA [22] which is shown in Figure 7. The SPICE simulations are performed using 0.5 μm CMOS process parameters provided by MOSIS (AGILENT). Supply voltages taken are ±1.5 V. Both the QO topologies are designed for an FO of 159 KHz and the simulated value was observed to be 161 KHz for Circuits I and II, respectively. The simulated transient output and corresponding frequency spectrum for Circuit I are showed in Figures 8 and 9, respectively, and those for Circuit II are depicted in Figures 10 and 11. The percentage total harmonic distortion (THD) is 0.57% for QO Circuit I and that for Circuit II is observed to be 0.7%. These values are considerably low as compared to 6.3% THD of QO circuit of [12].

5. Conclusion

Two topologies of third order OTRA based quadrature oscillator are presented in this paper using lossy and lossless integrators. The simulations are performed using PSPICE and it is observed that the results are in close agreement with theoretical propositioned. The simulated value of % THD in both the circuits is quite low as compared to other third order structures available in literature. The effect of nonideal behavior of OTRA and high frequency compensation scheme has also been included in the proposed theory.
Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

References


Figure 10: Transient output of proposed QO Circuit II.

Figure 11: Frequency spectrum of output of QO Circuit II.