Research Article

Design of CDTA and VDTA Based Frequency Agile Filters

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This paper presents frequency agile filters based on current difference transconductance amplifier (CDTA) and voltage difference transconductance amplifier (VDTA). The proposed agile filter configurations employ grounded passive components and hence are suitable for integration. Extensive SPICE simulations using 0.25 μm TSMC CMOS technology model parameters are carried out for functional verification. The proposed configurations are compared in terms of performance parameters such as power dissipation, signal to noise ratio (SNR), and maximum output noise voltage.

1. Introduction

The rapid evolution of wireless services has led to demand for one-fits-all “analog” front end solution. These services use different standards and therefore necessitate development of integrated multistandard transceivers as they result in reduction of size, price, complexity, and power consumption. The parameters of integrated transceiver can be modified in order to be able to adapt to the specifications of each standard [1]. Practically, the designs employ either elements handling various standards in parallel or reconfigurable elements. The frequency agile filter (FAF) [1–10] characterized by adjustment range, reconfigurability, and agility may be used in transceivers. The term shadow filters is sometimes used in literature to refer to FAF [11,12]. The literature survey shows that a limited number of topologies of active FAF are available and are based on op-amp [1] and current mode active block [2,3] and CMOS [4].

There is a wide range of current mode building blocks available in open literature. Among these blocks current difference transconductance amplifier (CDTA) [11] is most suitable for current mode signal processing owing to its low input and high output impedances, respectively. The VDTA is yet another recently introduced building block which works on a principle similar to that of CDTA except that the input current differencing unit is replaced by the voltage differencing circuit. Many applications such as filters and oscillators based on CDTA and VDTA are available and have been reported in the literature [13–27] and references cited therein.

The main intention of this paper is to present CDTA and VDTA based frequency agile filter topologies. The proposed filters are suitable for integration as these employ grounded capacitors and a resistor. The paper is organised as follows. The FAF implementation scheme is briefly reviewed in Section 2. The CDTA based Class 0, Class 1, and Class 2 FAF are presented in Section 3. Section 4 deals with the realization of VDTA based Class 0, Class 1, and Class 2 FAF. In Section 5, nonideal analysis of filters is presented. Simulation results are provided in Section 6 to substantiate the proposed FAF topologies. The performance characteristics of filter topologies are described in Section 7. The paper is concluded in Section 8.

2. Implementation Scheme of FAF

The implementation scheme of frequency agile filter (FAF) [3] is briefly reviewed in this section.

2.1. Class 0 FAF. A classical second order filter with band pass ($I_{BP}$) and low pass ($I_{LP}$) outputs of Figure 1 is designated as
Class 0 FAF [3]. The transfer functions of Class 0 FAF are given by

\[ T_{BP}(s) = \frac{I_{BP}}{I_{IN}} = \frac{ks}{1 + \alpha s + \beta s^2}, \]
\[ T_{LP}(s) = \frac{I_{LP}}{I_{IN}} = \frac{p}{1 + \alpha s + \beta s^2}. \]

The center frequency \( f_0 \) and quality factor \( Q \) of the filter are represented by (2) and (3), respectively:

\[ f_0 = \frac{1}{2\pi \sqrt{\beta}}. \]
\[ Q = \sqrt{\frac{\beta}{\alpha}}. \]

2.2. Class 1 FAF. The basic block diagram of Class 1 FAF is shown in Figure 2 wherein the low pass output of the Class 0 FAF is amplified (with variable gain \( A \)) and fed back to the input. The characteristic frequency \( f_{0A} \) and quality factor \( Q_A \) of Class 1 FAF are given by (4) and (5), respectively:

\[ f_{0A} = f_0 \sqrt{(1 + Ap)}, \]
\[ Q_A = Q \sqrt{(1 + Ap)}. \]

2.3. Class n FAF. The method outlined for Class 1 FAF realization can be extended for Class \( n \) FAF implementation as shown in Figure 3. This requires \( n \) amplifiers each with gain \( A \) (\( A_1 = A_2 = \cdots = A_{n-1} = A_n \)) to be placed in \( n \) feedback paths obtained in the same way as done in Class 1 implementation. The characteristic parameters of Class \( n \) FAF are given by

\[ f_{0n} = f_0 (1 + Ap)^{n/2}, \]
\[ Q_n = Q (1 + Ap)^{n/2}. \]

3. CDTA Based FAF

The CDTA [11–18] consists of a unity-gain current source controlled by the difference of the input currents and a transconductance amplifier providing electronic tunability through its transconductance gain. The CDTA symbol is shown in Figure 4 and its terminal characteristics in matrix form are given by

\[ \begin{bmatrix} V_p \\ V_n \\ I_z \\ I_{x+} \\ I_{x-} \\ V_x^+ \\ V_x^- \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & g & 0 & 0 \\ 0 & 0 & 0 & g & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_z \\ I_{x+} \\ I_{x-} \\ V_x^+ \\ V_x^- \end{bmatrix}, \]

(7)

where \( g \) is transconductance of the CDTA. The CMOS implementation of CDTA [16] is given in Figure 5. The transistor network comprising transistors Mc1–Mc17 performs [16] current differencing operation on the currents entering at \( p \) and \( n \) nodes, which is available at \( Z \) terminal. The voltage at \( z \) terminal drives the source coupled pair (transistors (Mc18–Mc21)) [16] of differential amplifier (Mc18–Mc26) giving a transconductance of \( g \). The value of transconductance \( (g) \) is expressed as

\[ g = \sqrt{2\mu C_{ox} \left( \frac{W}{L} \right)_{19,21} I_{Bias}}, \]

(8)

which can be adjusted by bias current \( I_{Bias} \) of CDTA.
3.1. CDTA Based Class 0 FAF. The CDTA based second order filter employing two CDTA blocks and two grounded capacitors is shown in Figure 6. The second CDTA block uses additional TA block with its current output terminals denoted by $x^+$ and $x^-$. It provides both low pass and band pass responses at high output impedance and can be used as Class 0 FAF. The current flowing through $x^+$ and $x^-$ is controlled through transconductance $g_2$ whereas current flowing through terminals $x^+$ and $x^-$ is controlled through $g_3$. The low pass and band pass transfer functions of CDTA based Class 0 FAF are given by (9) and (10), respectively:

$$I_{LP} = \frac{g_1g_2}{C_1C_2s^2 + sC_1g_3 + g_1g_2}, \quad (9)$$

$$I_{BP} = \frac{sC_2g_1}{C_1C_2s^2 + sC_1g_3 + g_1g_2} \left(1 + Rg_4\right), \quad (10)$$

The center frequency and quality factor of Class 0 FAF are expressed as

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{g_1g_2}{C_1C_2}}, \quad (11)$$

$$Q = \frac{1}{g_3} \sqrt{\frac{g_1g_2C_2}{C_1}}. \quad (12)$$

It may be noted that the $Q$ of the Class 0 FAF can be controlled independent of $f_0$ by varying $g_3$.

3.2. CDTA Based Class 1 FAF. The CDTA based Class 1 FAF is shown in Figure 7. It employs Class 0 FAF of Figure 6 along with an additional TA block (provides an output current which is product of its transconductance and voltage difference between noninverting (+) and inverting (−) terminals) and one grounded resistor. The TA block in the feedback path functions as an amplifier with tunable gain $A$ as given in

$$A = g_4R, \quad (13)$$

where $g_4$ is the transconductance of TA block and is given by $\sqrt{2\mu C_{ox}(W/L)_{19,21}I_{Bias}}$.

The low pass and band pass transfer functions of CDTA based Class 1 FAF are given by (14) and (15), respectively:

$$I_{LP} = \frac{g_1g_2}{C_1C_2s^2 + sC_1g_3 + g_1g_2 \left(1 + Rg_4\right)}, \quad (14)$$

$$I_{BP} = \frac{sg_1C_2}{C_1C_2s^2 + sC_1g_3 + g_1g_2 \left(1 + Rg_4\right)}. \quad (15)$$

The center frequency and quality factor of the CDTA based Class 1 FAF are expressed by (16) and (17), respectively:

$$f_{0A} = \frac{1}{2\pi} \sqrt{\frac{g_1g_2}{C_1C_2} \left(1 + g_4R\right)}, \quad (16)$$

$$Q_A = \frac{1}{g_3} \sqrt{\frac{g_1g_2C_2}{C_1} \left(1 + g_4R\right)}. \quad (17)$$

3.3. CDTA Based Class 2 FAF. The CDTA based Class 2 FAF is shown in Figure 8. It employs two CDTA blocks, two grounded capacitors, three TA blocks, and two grounded resistors. The TA blocks in the feedback path are used as amplifier with tunable gain $A$. The gain $A$ of TA based
Figure 6: CDTA based Class 0 FAF.

Figure 7: CDTA based Class 1 FAF.

Figure 8: CDTA based Class 2 FAF.
4. The VDTA Based FAF

The circuit symbol and the CMOS realization of VDTA [20, 21] are shown in Figures 10 and 11, respectively. The VDTA consists of two transconductance (TC) stages termed as input and output stages. The input differential voltage \( (V_p - V_n) \) is converted to current \( I_x \) through TC gain \( (g_1) \) of input stage and second stage converts the voltage at \( z \) terminal \( (V_z) \) to current \( (I_z) \) through its TC gain \( (g_2) \). The port relations of VDTA can thus be defined by the following matrix:

\[
\begin{bmatrix}
I_z \\
I_{z_c}
\end{bmatrix} =
\begin{bmatrix}
g_1 & -g_1 & 0 \\
0 & g_1 & 0 \\
0 & 0 & g_2 \\
0 & 0 & -g_2
\end{bmatrix}
\begin{bmatrix}
V_p \\
V_n \\
V_z
\end{bmatrix},
\]

(23)

The TC \( g_1 \) and TC \( g_2 \) are expressed by (24) which can be adjusted by bias currents \( I_{Bias1} \) and \( I_{Bias2} \), respectively:

\[
g_1 = \sqrt{\frac{2\mu C_{ox} W_1}{L_1,2}} I_{Bias1},
\]

\[
g_2 = \sqrt{\frac{2\mu C_{ox} W_5,6}{L_5,6}} I_{Bias2}.
\]

(24)

4.1. VDTA Based Class 0 FAF. The VDTA based Class 0 FAF employing single VDTA and two grounded capacitors is shown in Figure 12. This circuit configuration is based on second order filter presented in [21]. However, to allow independent control of quality factor and center frequency an additional TA block with transconductance \( g_1 \) is included in VDTA. The current flowing through \( z \) terminal is controlled by transconductance \( g_1 \) whereas current flowing through \( z_c \) terminal is controlled by \( g_3 \). The terminal characteristics of the modified VDTA block are given by (25). The low pass and band pass transfer functions of VDTA based Class 0 FAF are given by (26) and (27), respectively:

\[
\begin{bmatrix}
I_{LP} \\
I_{BP}
\end{bmatrix} =
\begin{bmatrix}
g_1 & -g_1 & 0 \\
0 & g_1 & 0 \\
0 & 0 & g_3 \\
0 & 0 & -g_3
\end{bmatrix}
\begin{bmatrix}
V_p \\
V_n \\
V_z
\end{bmatrix},
\]

(25)

\[
I_{LP} = \frac{g_1 g_3}{C_1 C_2} \left(1 + g_4 R \right),
\]

\[
I_{BP} = \frac{g_1 g_3}{C_1 C_2} \left(1 + g_4 R \right).
\]

(26)

The center frequency and quality factor of Class 0 FAF are expressed by (28). The center frequency can be controlled by
I_{Bias1} and I_{Bias3} whereas quality factor can be independently controlled by I_{Bias2}:

\[ f_0 = \frac{1}{2\pi} \sqrt{\frac{g_1 g_3}{C_1 C_2}}, \quad (28) \]

\[ Q = \frac{1}{g_2} \sqrt{\frac{g_1 g_3 C_1}{C_2}}, \]

4.2. VDTA Based Class 1 FAF. The VDTA based Class 1 FAF is shown in Figure 13. It employs two VDTA blocks and two grounded capacitors. The second VDTA block is used as amplifier with tunable gain \( A \). The gain \( A \) of VDTA based amplifier is given by

\[ A = \frac{g_4}{g_3}, \quad (29) \]

and can be adjusted by varying \( I_{Bias3} \) and \( I_{Bias4} \).

The low pass and band pass transfer functions of VDTA based Class 1 FAF are given by (30) and (31), respectively:

\[ \frac{I_{LP}}{I_{IN}} = \frac{g_1 g_3}{C_1 C_2 s^2 + s C_2 g_2 + g_1 g_3 (1 + (g_4/g_3))}, \quad (30) \]

\[ \frac{I_{BP}}{I_{IN}} = \frac{sg_1 C_2}{C_1 C_2 s^2 + s C_2 g_2 + g_1 g_3 (1 + (g_4/g_3))}. \quad (31) \]

The center frequency and quality factor of the VDTA based Class 1 FAF are expressed by (32) and (33), respectively. The center frequency can be independently controlled by varying \( I_{Bias2} \) without changing center frequency:

\[ f_{0A} = \frac{1}{2\pi} \sqrt{\frac{g_1 g_3 C_1}{C_2} \left(1 + \frac{g_4}{g_3}\right)}, \quad (32) \]

\[ Q_A = \frac{1}{g_2} \sqrt{\frac{g_1 g_3 C_1}{C_2} \left(1 + \frac{g_4}{g_3}\right)}. \quad (33) \]

4.3. VDTA Based Class 2 FAF. The VDTA based Class 2 FAF is shown in Figure 14 which employs three VDTAs, two grounded capacitors and one grounded resistor. The second VDTA block is used as amplifier with tunable gain \( A \). The gain \( A \) of VDTA based amplifier is given by (34). The proposed filter uses grounded resistor which can easily be implemented using the TA with transconductance equal to \( g_3 \) based structure given in Figure 9. To realize second order filter, \( I_{Bias7} \) is set to value of \( I_{Bias4} \) such that \( g_7 \) is equal to \( g_4 \) and \( I_{Bias6} \) is set to value such that \( g_6 \) is equal to sum of \( g_3 \) and \( g_4 \); that is, \( g_6 = g_3 + g_4 \). Consider

\[ A = \frac{g_4}{g_3}, \quad (34) \]

which can be adjusted by varying \( I_{Bias3} \) and \( I_{Bias4} \), thereby making \( f_{0A} \) tunable.
5. Nonideal Analysis

In this section, nonideal analysis of CDTA and VDTA based Class 0 FAF is presented.

5.1. Nonideal Analysis of Class 0 CDTA Based FAF.

In practice, the transfer functions (9) and (10) modify due to nonidealities which are classified as tracking errors and parasites. The tracking errors cause current transfer from \( p \) and \( n \) ports to \( z \) port to differ from unity value and are represented by \( \alpha_p \) and \( \alpha_n \). There is deviation in transconductance transfer from \( z \) to \( x^+ \) and \( x^- \) ports which is modeled by \( \beta g V_z \). The parasites denoted by resistances \( R_p \) and \( R_n \) are at \( p \) and \( n \) terminals; shunt output impedances \( (R//C) \) are present at terminals \( z \), \( z_c \), \( x^+ \), and \( x^- \), and \( x^+_c \) and \( x^-_c \). The effect of the parasites is highly dependent on the topology. A close inspection of the circuit of Figure 6 shows that the parasitic capacitances

\[
\begin{align*}
I_{LP} &= \frac{g_1 g_3}{C_1 C_2 s^2 + s C_2 g_2 + g_1 g_3 (1 + (g_4/g_3))^2}, \\
I_{BP} &= \frac{s g_1 C_2}{C_1 C_2 s^2 + s C_2 g_2 + g_1 g_3 (1 + (g_4/g_3))^2}. 
\end{align*}
\]

The center frequency and quality factor of the CDTA based Class 1 FAF are expressed by (37) and (38), respectively:

\[
\begin{align*}
f_0 &= \frac{1}{2\pi} g_1 g_3 \frac{1 + (g_4/g_3)}{C_1 C_2}, \\
Q &= \frac{1}{g_2} \frac{g_1 g_3 C_2}{C_2 (1 + (g_4/g_3))}. 
\end{align*}
\]
present at $z$ terminal can be easily accommodated in external capacitances.

Reanalysis of the proposed circuit (Figure 6) yields the following nonideal transfer functions:

\[
\frac{I_{LP}}{I_{IN}} = \frac{\alpha_2^2 \beta^2 g_1 g_2 Q_1}{D_n(s)}, \quad (39a)
\]

\[
\frac{I_{BP}}{I_{IN}} = \frac{\alpha_2^2 \beta g_1 \left(sC_{2eq} + G_x\right) Q_1}{D_n(s)}, \quad (39b)
\]

where

\[
D_n(s) = P_1 Q_1 \left(sC_{1eq} + G_x\right) \left(sC_{2eq} + G_x\right) + \alpha_p \beta g_1 P_1 \left(sC_{1eq} + G_x\right) + \alpha_p \sigma_n \beta^2 g_1 g_2,
\]

\[
P_1 = \left(1 + G_x R_n + sC_X R_n\right);
\]

\[
Q_1 = \left(1 + G_x R_p + sC_X R_p\right);
\]

\[
C_{1eq} = C_1 + C_z; \quad C_{2eq} = C_2 + C_z;
\]

\[
G_x = \frac{1}{R_X}; \quad G_z = \frac{1}{R_z};
\]

Choosing operating frequencies below \(\min(1/C_X R_p, 1/C_X R_n)\) (as \(G_X R_n \ll 1\) and \(G_X R_p \ll 1\)) the terms \(P_1\) and \(Q_1\) would not affect the transfer function. For frequencies below \(\min(G_Z/C_{1eq} G_Z/C_{2eq})\), (39c) modifies to

\[
D_n(s) = s^2 C_{1eq} C_{2eq} + \alpha_p \beta g_3 s C_{1eq} + \alpha_p \sigma_n \beta^2 g_1 g_2, \quad (39d)
\]

and transfer functions (39b) and (39c) change to

\[
\frac{I_{LP}}{I_{IN}} = \frac{\alpha_2^2 \beta^2 g_1 g_2}{D_n(s)}, \quad (40a)
\]

\[
\frac{I_{BP}}{I_{IN}} = \frac{\alpha_2^2 \beta g_1 sC_{2eq}}{D_n(s)}. \quad (40b)
\]
The center frequency, quality factor of Class 0 FAF can be expressed as

$$f_0 = \frac{1}{2\pi} \left[ \frac{\alpha_p \alpha_p \beta^2 g_1 g_2}{C_{1eq} C_{2eq}} \right]$$

$$Q = \frac{1}{g_3} \left[ \frac{\alpha_p \alpha_p g_1 g_2 C_{2eq}}{C_{1eq}} \right]$$

(41a)

(41b)

It is clear that the transfer functions and filter parameters ((40a), (40b) and (41a), (41b)) deviate from the ideal value in presence of nonidealities. The change can, however, be accommodated by adjusting bias currents.

5.2. Nonideal Analysis of Class 0 VDTA Based FAF. Considering the nonideal characteristics of the VDTA, the port relations of current and voltage in (25) can be rewritten as

$$\begin{bmatrix}
I_x \\
I_y \\
I^f_x \\
I^f_y \\
I^s_x \\
I^s_y
\end{bmatrix} =
\begin{bmatrix}
\beta g_3 & -\beta g_1 & 0 \\
-\beta g_1 & -\beta g_2 & 0 \\
-\beta g_2 & -\beta g_3 & 0 \\
0 & 0 & -\beta g_3
\end{bmatrix}
\begin{bmatrix}
V_p \\
V_y \\
V^f_y \\
V^s_y
\end{bmatrix},$$

(42)

where $\beta$ represents the tracking error. Apart from tracking error, the parasites appear as shunt impedances ($R/C$) at
ports $p$, $n$, $z$, $z_c$, and $x^+$ denoted by ($R_p$/$C_p$), ($R_n$/$C_n$), ($R_z$/$C_z$), ($R_{z_c}$/$C_{z_c}$), and ($R_x$/$C_x$), respectively. The parasitic capacitances present at $p$, $z$, $z_c$, and $x$ terminal can be easily accommodated in external capacitances.

Reanalysis of the proposed circuit in Figure 12 yields the following nonideal transfer functions of Class 0 VDTA based FAF.

Then

$$\frac{I_{LP}}{I_{IN}} = \frac{g_1 g_3 \beta^2}{D_{n2}(s)}, \quad (43a)$$

$$\frac{I_{BP}}{I_{IN}} = \frac{\beta g_1 \left(sC_{1eq} + G_z\right)}{D_{n2}(s)}, \quad (43b)$$

where

$$D_{n2}(s) = \left(sC_{2eq} + G_z\right) \left(sC_{1eq} + G_x + G_z + G_p + \beta g_2\right) + \beta^2 g_1 g_3,$$

$$C_{1eq} = C_1 + C_x + C_z + C_p; \quad C_{2eq} = C_2 + C_z;$$

$$G_z = \frac{1}{R_Z}; \quad G_x = \frac{1}{R_X};$$

$$G_p = \frac{1}{R_p}.$$  \hspace{1cm} (43c)

As $G_z + G_p + \beta g_2 \ll \beta g_2$, (43c) modifies to

$$D_{n2}(s) = \left(sC_{2eq} + G_z\right) \left(sC_{1eq} + \beta g_2\right) + \beta^2 g_1 g_3.$$ \hspace{2.5cm} (44)

Choosing operating frequencies below $\min (G_z/C_{1eq}, G_z/C_{2eq})$ (44) reduces to

$$D_{n2}(s) = s^2C_{1eq}C_{2eq} + sC_{2eq} \beta g_2 + \beta^2 g_1 g_3.$$ \hspace{2.5cm} (45)

and the transfer function (43b) simplifies to

$$\frac{I_{LP}}{I_{IN}} = \frac{g_1 g_3 \beta^2}{D_{n2}(s)}, \quad (46a)$$

$$\frac{I_{BP}}{I_{IN}} = \frac{\beta g_1 sC_{2eq}}{D_{n2}(s)}.$$  \hspace{1cm} (46b)
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6. Simulation Results

In this section, the functionality of the proposed filters has been verified. The SPICE simulations results for CDTA and VDTA based filters have been presented using TSMC 0.25 μm CMOS process model parameters and supply voltages of $V_{DD} = -V_{SS} = 1.8$ V.

6.1. Simulation of CDTA Based FAF. The CMOS schematic of Figure 5 is used for verifying CDTA based FAF and the aspect ratios of the MOS transistors are given in Table 1. The additional TA blocks in CDTA providing current ports ($x^+_C$, $x^-_C$, $x'^+_C$, and $x'^-_C$) use aspect ratios same as that for $x^+$ and $x^-$. The capacitors $C_1$ and $C_2$ are chosen as 50 pF each.

And the filter parameters are calculated as

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{g_2^2 g_3}{C_{1eq} C_{2eq}}}, \quad (47a)$$

$$Q = \frac{1}{g_2} \sqrt{\frac{g_1 g_3 C_{2eq}}{C_{1eq}}}, \quad (47b)$$

It is clear that the transfer functions and filter parameters ((46a), (46b) and (47a), (47b)) deviate from the ideal value in presence of nonidealities. The change can, however, be accommodated by adjusting bias currents.

![Figure 26: (a) and (c) Input and its frequency spectrum. (b) and (d) Output and its frequency spectrum for Class 0 FAF.](image1)

![Figure 27: SNR of CDTA based FAF.](image2)

![Figure 28: SNR of VDTA based FAF.](image3)
The grounded resistor of Figure 7 is realized using TA block. The bias current is set as 0.85 $\mu$A to realize a resistor of value 10 kΩ. The frequency responses of CD T A based Class 0, Class 1, and Class 2 FAF topologies are depicted in Figures 15, 16, and 17, respectively. The responses are obtained by varying bias currents $I_{Bias1}$ and $I_{Bias2}$ ($I_{Bias1} = I_{Bias2} = I_{Bias3}$) to 1 $\mu$A, 10 $\mu$A, 30 $\mu$A, and 60 $\mu$A while keeping $I_{Bias3}$ and $I_{Bias4}$, respectively, at 0.5 $\mu$A and 10 $\mu$A. It can be clearly noticed that center frequency $f_0$ increases on increasing the bias current.

The electronic tunability of quality factor and center frequency for proposed Class 0, Class 1, and Class 2 FAF topologies are shown in Figure 24 for different values of $I_{Bias2}$. While setting $I_{Bias1}$ and $I_{Bias3}$ to 30 $\mu$A in Class 0, the responses for Class 1 FAF are obtained by setting $I_{Bias1}$ and $I_{Bias2}$ to 30 $\mu$A and setting $I_{Bias3}$ and $I_{Bias4}$ to 0.5 $\mu$A, respectively. To plot responses for Class 1 FAF, the grounded resistor is implemented at 0.5 $\mu$A and 10 $\mu$A. The input and output waveforms along with their frequency spectrum for CD T A based Class 0 FAF. It may clearly be noted that the CD T A based Class 0 FAF allows only 1 MHz signal to pass and significantly attenuates signals of frequencies 100 kHz, 500 kHz, and 10 MHz. Similar responses for Class 1 and Class 2 FAF were also obtained.

### 6.2. Simulation of VDT A Based FAF

The CMOS schematic of Figure 12 is used for verifying VDT A based FAF and the aspect ratios of the MOS transistors are given in Table 2. The capacitors $C_1$ and $C_2$ are taken as 50 pF each. In the realization of Class 2 FAF, the grounded resistor is implemented by TA block. The frequency responses of VDT A based Class 0, Class 1, and Class 2 FAF topologies are shown in Figures 21, 22, and 23, respectively. The responses are obtained by keeping $I_{Bias3}$ to 5 $\mu$A and setting bias currents $I_{Bias1}$ and $I_{Bias3}$ ($I_{Bias1} = I_{Bias3} = I_{Bias4}$) to 5 $\mu$A, 10 $\mu$A, 30 $\mu$A, and 60 $\mu$A. In realization of Class 1 FAF, $I_{Bias4}$ is set to obtain $g_4 = g_3 = 3$ while keeping $I_{Bias5}$ equal to $I_{Bias1}$. In realization of Class 2 FAF, $I_{Bias6}$ is selected such that $g_6 = g_3 + g_4$ while $I_{Bias7}$ is equal to $I_{Bias1}$.

The electronic tunability of quality factor and center frequency for proposed Class 0, Class 1, and Class 2 VDT A based FAF is plotted in Figures 24 and 25, respectively. The analytical and simulated responses describing variation of quality factor are shown in Figure 24 for different values of $I_{Bias1}$, while setting $I_{Bias1}$ and $I_{Bias3}$ to 0.5 $\mu$A. To plot responses for Class 1, $I_{Bias3}$ is set to obtain $g_4 = g_3 + g_4$ while $I_{Bias5}$ is set equal to $I_{Bias1}$. Class 2 FAF responses are plotted by selecting $I_{Bias6}$ to obtain $g_6 = g_3 + g_4$ while $I_{Bias7}$ is equal to $I_{Bias4}$. Figure 25 depicts the analytical and simulated responses for Class 1 FAF. The responses for Class 1, $I_{Bias1}$ is set to a value in such a manner that $g_4 = g_3 = 3$ whereas $I_{Bias5}$ is set equal to $I_{Bias1}$. The Class 2 FAF responses are plotted by setting $I_{Bias6}$ to value such that $g_6 = g_3 + g_4$ whereas $I_{Bias7}$ is equal to $I_{Bias4}$.

The transient behaviour of proposed agile filter is also studied by applying input signals of frequencies 100 kHz, 500 kHz, 1 MHz, and 10 MHz, each having an amplitude of 10 $\mu$A. The responses for Class 0 FAF are obtained by setting bias currents $I_{Bias1}$ and $I_{Bias2}$ each to 10 $\mu$A and $I_{Bias3}$ to 0.5 $\mu$A. Figure 20 shows the input and output waveforms along with their frequency spectrum for CD T A based Class 0 FAF. It may clearly be noted that the CD T A based Class 0 FAF allows only 1 MHz signal to pass, partially attenuates signal of frequency 500 kHz, and significantly attenuates signals of frequencies 100 kHz and 10 MHz. Similar responses for Class 1 and Class 2 FAF are also obtained.

### 7. Performance Evaluation

The performance of proposed CD T A and VDT A based FAF circuits is studied in terms of power dissipation, output noise voltage, and SNR. The overall performance characteristics are summarized in Table 3. Figures 27 and 28 depict the signal to noise ratio (SNR) for the proposed CD T A and VDT A based filter topologies for Class 0, Class 1, and Class 2, respectively. The VDT A based FAF proved to be optimum concerning the power dissipation and signal to noise ratio. The maximum output noise voltage is better in VDT A based FAF.

### 8. Conclusion

In this paper CD T A and VDT A based frequency agile filters are presented. The proposed FAF configurations employ...
Table 3: Performance characteristics of CDTA and VDTA based Class 0, Class 1, and Class 2 FAF.

<table>
<thead>
<tr>
<th>Performance characteristics</th>
<th>Type of FAF</th>
<th>$I_{\text{bias}} = 1\mu\text{A}$</th>
<th></th>
<th>$I_{\text{bias}} = 10\mu\text{A}$</th>
<th></th>
<th>$I_{\text{bias}} = 30\mu\text{A}$</th>
<th></th>
<th>$I_{\text{bias}} = 60\mu\text{A}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CDTA</td>
<td>Class 0</td>
<td>Class 1</td>
<td>Class 2</td>
<td>Class 0</td>
<td>Class 1</td>
<td>Class 2</td>
<td>Class 0</td>
</tr>
<tr>
<td>Power dissipation (mW)</td>
<td>0.359</td>
<td>0.997</td>
<td>1.63</td>
<td>3.34</td>
<td>3.99</td>
<td>4.63</td>
<td>9.98</td>
<td>10.7</td>
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<tr>
<td></td>
<td>0.089</td>
<td>0.177</td>
<td>0.405</td>
<td>0.32</td>
<td>1.19</td>
<td>3.45</td>
<td>0.835</td>
<td>3.34</td>
</tr>
<tr>
<td>SNR (dB)</td>
<td>CDTA</td>
<td>124.9</td>
<td>122.1</td>
<td>119.2</td>
<td>135.5</td>
<td>134.2</td>
<td>131.3</td>
<td>140.2</td>
</tr>
<tr>
<td></td>
<td>VDTA</td>
<td>175.82</td>
<td>170.4</td>
<td>165.0</td>
<td>181.7</td>
<td>180.5</td>
<td>170.96</td>
<td>182.0</td>
</tr>
<tr>
<td>Max. output noise voltage (nV)</td>
<td>CDTA</td>
<td>79.37</td>
<td>74.92</td>
<td>75.49</td>
<td>155.02</td>
<td>82.99</td>
<td>58.97</td>
<td>210.46</td>
</tr>
<tr>
<td></td>
<td>VDTA</td>
<td>28.5</td>
<td>28.85</td>
<td>28.1</td>
<td>38.92</td>
<td>37.43</td>
<td>51.3</td>
<td>46.10</td>
</tr>
</tbody>
</table>
grounded passive components and are suitable for integration. The filter configurations are designed in such a way that quality factor can be independently controlled without changing the center frequency. The simulation results are included to demonstrate the workability of the circuits. The performance of the proposed FAF is evaluated in terms of power dissipation, SNR, and noise performance. The VDTA based FAF proved to be optimum concerning the power dissipation and signal to noise ratio.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

References


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