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Research Article

Low Voltage Floating Gate MOS Transistor Based Differential Voltage Squarer

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This paper presents novel floating gate MOSFET (FGMOS) based differential voltage squarer using FGMOS characteristics in saturation region. The proposed squarer is constructed by a simple FGMOS based squarer and linear differential voltage attenuator. The squarer part of the proposed circuit uses one of the inputs of two-input FGMOS transistor for threshold voltage cancellation so as to implement a perfect squarer function, and the differential voltage attenuator part acts as input stage so as to generate the differential signals. The proposed circuit provides a current output proportional to the square of the difference of two input voltages. The second order effect caused by parasitic capacitance and mobility degradation is discussed. The circuit has advantages such as low supply voltage, low power consumption, and low transistor count. Performance of the circuit is verified at ±0.75 V in TSMC 0.18 μm CMOS, BSIM3, and Level 49 technology by using Cadence Spectre simulator.

1. Introduction

Technology scaling and growing demand of portable electronic equipments have motivated the researchers towards the design of low voltage and low power analog signal processing circuits. Low supply voltage increases the battery lifetime and hence reduces the power consumption of the portable equipment. Various low-voltage lowpower design techniques reported in literatures include subthreshold MOSFETs, level shifters, self-cascode, bulk-driven, and FGMOS techniques [1–10]. Among these, FGMOS concept has gained prime importance due to its ability to reduce or remove the threshold voltage requirement of the circuit. Scaling of transistor dimensions has motivated the designers towards the design of low voltage nonlinear CMOS circuits. Voltage squarer is one of the most versatile nonlinear blocks that find application in several fields like neural and image signal processing [11–18]. It can be used to implement various nonlinear circuits such as multipliers, balanced modulators, and phase comparators. Analog hardware implementation of these blocks offers advantage of reduced silicon area and low power consumption. CMOS squarer circuit based on cross-coupled differential pair has been proposed in [11] but the circuit is complex and has large supply voltage requirement. Squarer with low supply voltage and high rejection of common-mode variations has been proposed in [12] and [13], respectively, but again these circuits require large number of transistors. Recently, the squarer topology using NMOS transistor has been proposed in [16] but it requires positive and negative bias voltage generator for threshold voltage cancellation and can process only single ended input signal. This paper presents very simple and new FGMOS based differential squarer which is the combination of the FGMOS based squarer proposed in [17] and differential voltage attenuator proposed in [18]. The proposed squarer can process differential signals and has low supply voltage, low power consumption, and low circuit complexity.

The operation of FGMOS transistor is described in Section 2. FGMOS based differential squarer is proposed and analyzed in Section 3. In Section 4, the simulation results are given to verify theoretical results and to demonstrate the effectiveness of the proposed circuit. Finally, the conclusions are drawn in the last section.

2. FGMOS Transistor

FGMOS is a multiple-input floating gate transistor whose threshold voltage can be controlled and tuned by the values

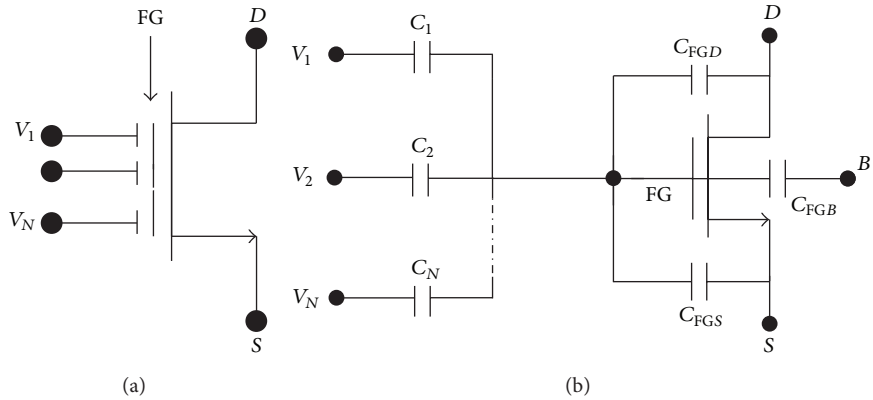

Figure 1: (a) Symbol of FMGOS; (b) FGMOS equivalent circuit.

of capacitors and bias voltage applied. The symbol of n-input FGMOS transistor and its equivalent circuit are shown in Figures 1(a) and 1(b), respectively. The voltage on floating gate (FG) V_{FG} is given by [10]

$$V_{\mathrm{FG}} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i + \frac{C_{\mathrm{GS}}}{C_T} V_S + \frac{C_{\mathrm{GD}}}{C_T} V_D + \frac{Q_{\mathrm{FG}}}{C_T}, \tag{1}$$

where C_i is the set of capacitors associated with effective inputs and the floating gate.

$C_T = C_1 + C_2 + C_{\mathrm{FGS}} + C_{\mathrm{FG}D} + C_{\mathrm{FG}B}$ is the total floating gate capacitance. $C_{\mathrm{FG}D}$, C_{FGS}, and $C_{\mathrm{FG}B}$ are the overlap capacitances of floating gate with drain, source, and bulk, respectively, V_D is the drain voltage, V_S is the source voltage, V_B is the bulk voltage, and Q_{FG} is the residual charge trapped in the oxide-silicon interface during fabrication process. The trapped residual charges give rise to the problem of offset in threshold voltage of the device. The removal of the residual charge can be done by using the method suggested in [19, 20], in which the first polysilicon layer is connected to the metal-k (where k represents number of metals available in the technology). By this contact, the floating gate is not connected to any part of the circuit so it will not affect the operation of FGMOS transistor. Therefore, neglecting the residual charge (1) can be modified as

$$V_{\mathrm{FGS}} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_{iS} + \frac{C_{\mathrm{FG}D}}{C_T} V_{\mathrm{DS}} + \frac{C_{\mathrm{FG}B}}{C_T} V_{\mathrm{BS}}. \tag{2}$$

The drain current (I_D) of the FGMOS transistor operating in saturation region is given by [10]

$$I_D = \frac{\mu_0 \mathrm{Cox}}{2} \frac{W}{L} \left(V_{\mathrm{FGS}} - V_T\right)^2 \tag{3}$$

Assuming $C_i \gg C_{\mathrm{FG}D}, C_{\mathrm{FG}B}$ [10, 21], the drain current of FGMOS transistor in saturation region can be expressed as

$$I_D = \frac{\beta}{2} \left(\sum_{i=1}^{N} k_i V_{iS} - V_T \right)^2, \tag{4}$$

where $k_i = C_i/C_T$, β is the transconductance, and V_T stands for the threshold voltage. In (4), it can be seen that by choosing proper values of multiple input voltages along with capacitance ratio the threshold voltage term can be cancelled so as to get the perfect squarer equation. The proposed circuit utilizes this property of FGMOS transistor to implement the squarer function.

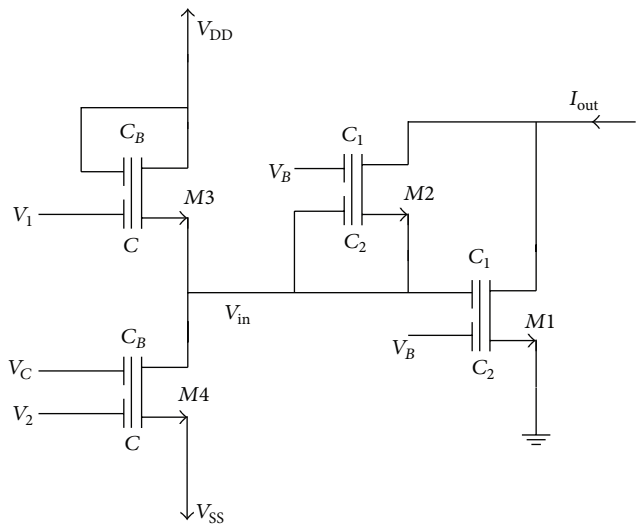

Figure 2: Proposed differential squarer.

Table 1: Aspect ratios of the transistor of the proposed circuit.

Transistor	W (μm)	L (μm)
M1-M2	4.4	0.18
M3-M4	0.54	0.18

3. Proposed FGMOS Based Differential Squarer

The proposed differential squarer is shown in Figure 2. It is constructed by FGMOS based squarer (M1, M2) and linear voltage attenuator (M3, M4). The squarer function is obtained by taking the advantage of FGMOS square law characteristics in saturation region. V_B and V_{in} are bias and signal voltages

Table 2: Comparison of various conventional and proposed squarers.

Parameters	[12]	[13]	Proposed
Technology (μm)	1.2	0.5	0.18
Supply voltage (V)	1.5	±2.5	±0.75
Number of transistors	11 MOS	6 MOS	4 FGMOS
Power dissipated (μW)	NA	NA	15
Input signal range (V_{PP})	0.26	1.5	0.75
Attenuation factor (α)	NA	NA	1/4
FGMOS capacitances (fF)	NA	NA	$C_B = 432, C = 144$ $C_1 = C_2 = 100$
Bias voltages (V)	NA	NA	$V_C = -0.25$ $V_B = 0.75$

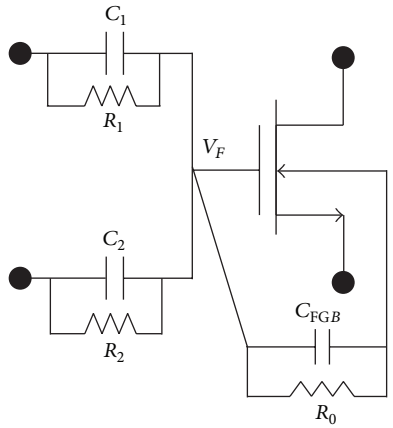

Figure 3: Simulation model of FGMOS.

applied at the two inputs of FGMOS transistor M1 and M2. If the input voltage V_{in} is positive, M2 is off while M1 operates in saturation region and if the input voltage V_{in} is negative, M1 is off while M2 operates in saturation region.

The output current of the squarer (neglecting the parasitic capacitances, channel-length modulation, mobility degradation, and the body effect) is given by

$$I_{out} = \frac{\beta_1}{2}\left(k_1 V_{inS1} + k_2 V_{BS1} - V_{T1}\right)^2, \quad \text{if } V_{in} > 0 \tag{5}$$

$$I_{out} = \frac{\beta_2}{2}\left(k_1 V_{BS2} + k_2 V_{inS2} - V_{T2}\right)^2, \quad \text{if } V_{in} < 0. \tag{6}$$

If $\beta_1 = \beta_2 = \beta$, $V_{T1} = V_{T2} = V_T$, $k_1 = k_2 = k$, and $kV_B = V_T$, then the output current of the squarer can be approximated as

$$I_{out} = \frac{\beta}{2}\left(kV_{in}\right)^2. \tag{7}$$

The input voltage V_{in} of the squarer is generated by voltage attenuator formed by FGMOS transistor M3 and M4. The output voltage of the attenuator is given by [18]

$$V_{in} = \alpha\left(V_1 - V_2\right) + \frac{kV_{SS} - k_B V_C}{k + k_B}, \tag{8}$$

where $k = C/(C + C_B)$, $k_B = C_B/(C + C_B)$ are the capacitive coupling ratio and $\alpha = k/(k + k_B)$ is the attenuation factor which can be adjusted by choosing proper values of k and k_B. From (8), it can be seen that the offset voltage term $(kV_{SS} - k_B V_C)/(k + k_B)$ can be cancelled by choosing proper value of bias voltage V_B. For zero output offset, the bias voltage V_C must be equal to

$$V_C = \frac{k}{k_B} V_{SS}. \tag{9}$$

Assuming zero-output offset for the voltage attenuator and combining (7) and (8), the output current of the squarer is modified as

$$I_{out} = \frac{\beta}{2}\left\{k\alpha\left(V_1 - V_2\right)\right\}^2. \tag{10}$$

If $k\alpha = k_{eq}$, then (10) can be written as

$$I_{out} = \frac{\beta}{2}\left\{k_{eq}\left(V_1 - V_2\right)\right\}^2. \tag{11}$$

From the above equation, it can be seen that the proposed squarer gives the output current proportional to the difference of input voltages V_1 and V_2 and The voltage range of input signals can be determined by the factor k_{eq}.

3.1. Second Order Effects. The operation of squarer has been analyzed by neglecting the deviations from ideal square-law characteristics due to parasitic capacitance and mobility degradation. These nonideal effects are the basic source of discrepancy between the ideal and simulated output currents of the proposed squarer.

3.1.1. Parasitic Capacitance. Parasitic capacitances have a minor effect on the squarer operation. The modified current equation after considering the parasitics is given by

$$I_{out} = \frac{\beta}{2}\left(k_{eq}\left(V_1 - V_2\right) + \frac{C_{GD}}{C_T} V_{DS} + \frac{C_{GB}}{C_T} V_{BS}\right)^2. \tag{12}$$

The ratios C_{GD}/C_T and C_{GB}/C_T can be neglected if the transistors are operating in saturation mode [21]. Therefore, the parasitic capacitances do not contribute significantly to the squarer operation and have only a small effect on the input range.

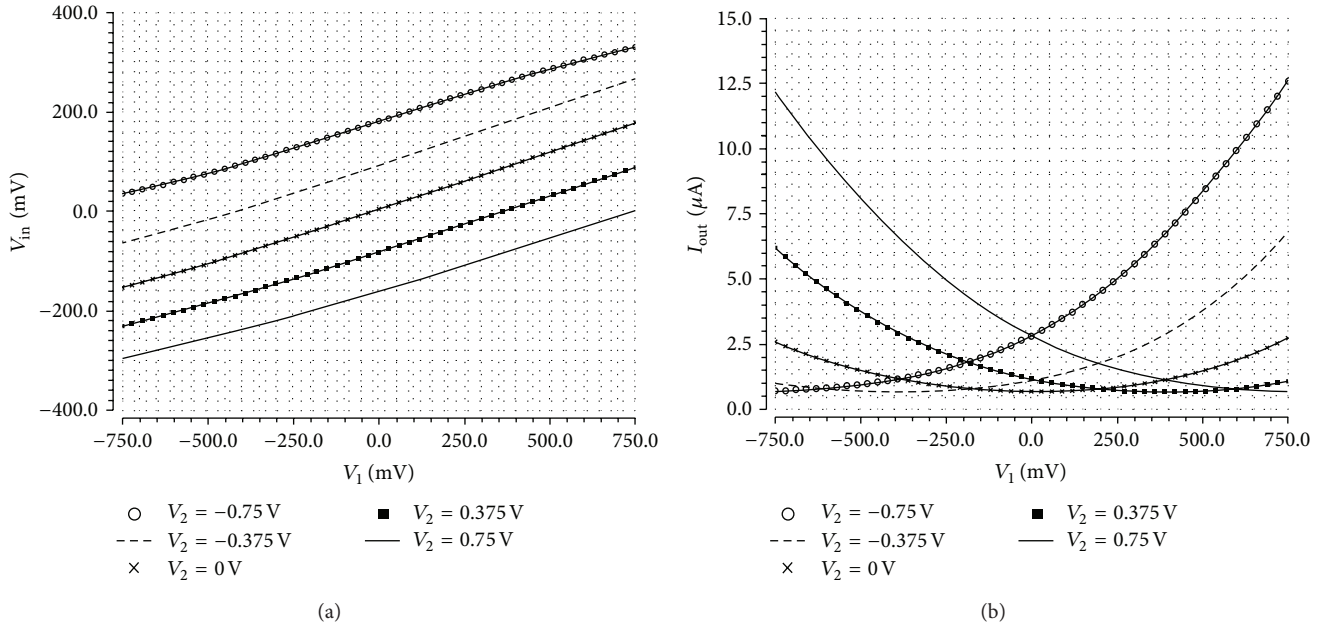

Figure 4: (a) DC response of the attenuator; (b) DC response of the proposed squarer.

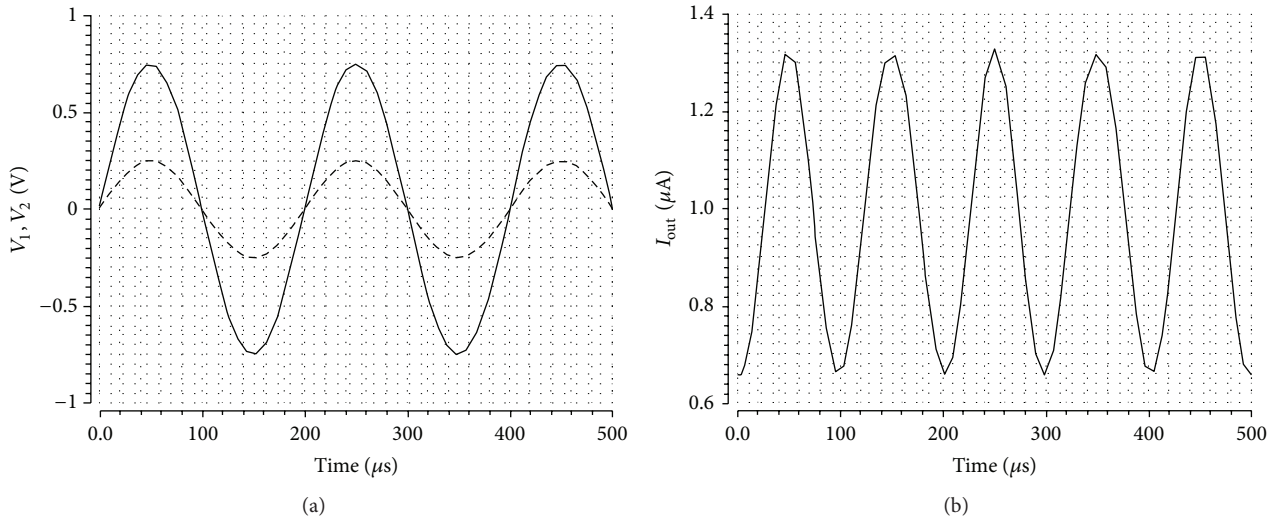

Figure 5: (a) Waveform of input signals V_1 and V_2; (b) transient response.

3.1.2. Mobility Degradation. Considering the mobility degradation effect, the I-V characteristic of NMOS transistor can be modelled by

$$I_D = \frac{(\beta/2)(V_{GS} - V_T)^2}{1 + \theta(V_{GS} - V_T)}, \tag{13}$$

where θ is mobility degradation parameter which has a value of about 0.1~0.001 V^{-1}. According to the above equation, the output current of the squarer can be modified as

$$I_{out} = \frac{\beta}{2}\{k_{eq}(V_1 - V_2)\}^2 \left[1 - \theta\{k_{eq}(V_1 - V_2)\} + \theta^2\{k_{eq}(V_1 - V_2)\}^2\right] \tag{14}$$

$$I_{out} = \frac{\beta}{2}\{k_{eq}(V_1 - V_2)\}^2 + \varepsilon, \tag{15}$$

where the output current error of the squarer can be given by

$$\varepsilon = -\frac{\beta}{2}\theta\{k_{eq}(V_1 - V_2)\}^3 \left[1 - \theta\{k_{eq}(V_1 - V_2)\}\right]. \tag{16}$$

From the above equation, it can be seen that total harmonic distortion due to mobility degradation will be negligible because of small value of mobility degradation parameter.

4. Simulation Results

The designed circuits are simulated using Cadence Spectre simulator in TSMC 0.18 μm CMOS technology using ±0.75 V

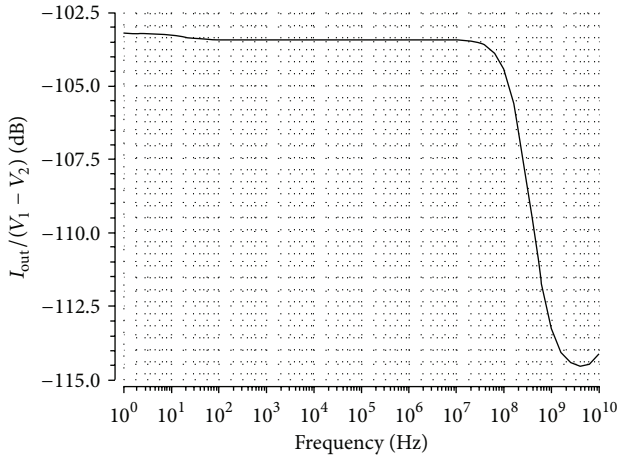

Figure 6: Frequency response of the proposed squarer.

power supply. The aspects ratios of the transistors of the proposed circuits are given in Table 1. Since the floating gate (FG) of FGMOS does not have any connection to ground, the simulator cannot understand the floating gate and reports dc convergence problem during simulation. To avoid dc convergence error during simulation model suggested in [10] has been used in this work. This model is based on connecting large value resistors in parallel with the input capacitors as shown in Figure 3. In this model, the relation between resistances and capacitances can be given as follows: $R_i = 1/kC_i = 1000\,\text{G}\Omega$.

The DC response of the attenuator and squarer against V_1 with V_2 varying from −0.75 V to 0.75 V is shown in Figures 4(a) and 4(b), respectively. It can be seen from the curves that the output voltage of attenuator varies from −320 mV to 320 mV and the maximum value of the output current of the squarer is approximately 12 μA. The proposed squarer operates at low supply voltage with total power consumption of 15 μW only. The transient response of the squarer is shown in Figure 5. Figure 5(a) shows that V_1 and V_2 are the two input sinusoidal signals with amplitude 0.75 V and 0.25 V peak-to-peak, respectively, and frequency 5 kHz and the output current is shown in Figure 5(b). The frequency response of the proposed squarer with V_1 = 1 mV is shown in Figure 6. It can be seen from the figure that the proposed squarer exhibits the bandwidth of 199.426 MHz. The performance parameters of the proposed circuit and various conventional circuits are compared in Table 2. It can be seen that the proposed configuration has the lowest transistor count, operates at low supply voltage, and also has low DC power consumption.

5. Conclusions

In this paper, novel differential voltage squarer based on simple FGMOS squarer and voltage attenuator has been proposed. The proposed circuit operates at ±0.75 V with maximum power consumption of 15 μW and bandwidth of 199.426 MHz. The circuit can process differential signal and hence it can be useful in various low voltage lowpower analog signal processing/generating applications.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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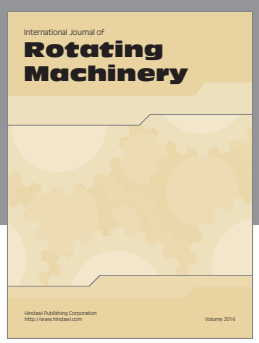

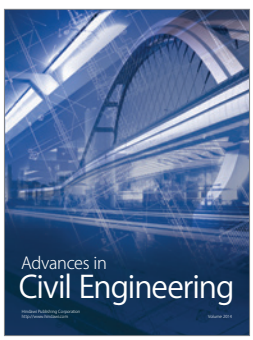

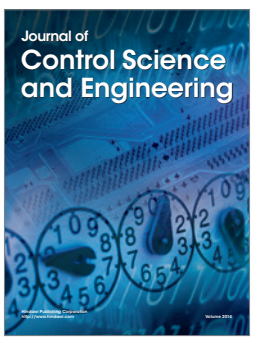

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