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Research Article

Multiobjective Genetic Algorithms Program for the Optimization of an OTA for Front-End Electronics

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The design of an interface to a specific sensor induces costs and design time mainly related to the analog part. So to reduce these costs, it should have been standardized like digital electronics. The aim of the present work is the elaboration of a method based on multiobjectives genetic algorithms (MOGAs) to allow automated synthesis of analog and mixed systems. This proposed methodology is used to find the optimal dimensional transistor parameters (length and width) in order to obtain operational amplifier performances for analog and mixed CMOS-(complementary metal oxide semiconductor-) based circuit applications. Six performances are considered in this study, direct current (DC) gain, unity-gain bandwidth (GBW), phase margin (PM), power consumption (P), area (A), and slew rate (SR). We used the Matlab optimization toolbox to implement the program. Also, by using variables obtained from genetic algorithms, the operational transconductance amplifier (OTA) is simulated by using Cadence Virtuoso Spectre circuit simulator in standard TSMC (Taiwan Semiconductor Manufacturing Company) RF 0.18 μm CMOS technology. A good agreement is observed between the program optimization and electric simulation.

1. Introduction

Microelectronics industry is distinguished by the raising level of integration and complexity. It aims at decreasing exponentially the minimum feature sizes used to design integrated circuits [1]. The cost in time of design is a great problem to the continuation of this evolution. Senior designer's knowledge and skills are required to ensure a good analog integrated circuit design. To fulfill the given requirements, the designer must choose the suitable circuit architecture, although different tools which partially automated the topology synthesis appeared in the past [2, 3].

Therefore, the use of multiple-objective optimization algorithms is of a great importance to the automatic design of operational amplifier. Accuracy, ease of use, generality, robustness, and reasonable run-time are necessary for a circuit synthesis solution to gain acceptance by using optimization methods [4–9].

This method uses a program based on multiobjective optimization using a genetic algorithm to calculate the optimal transistors dimensions, length, and width of an operational amplifier (Figure 1) which is used as part of an electronic front-end for signal shaping stage. The method which handles a wide variety of specifications and constraints is extremely fast and results in globally optimal designs.

The aim of this work is to design and optimize an operational amplifier circuit in sight of a front-end electronics of the semiconductor tracker (SCT) detector in ATLAS (A Toroidal LHC Apparatus) experiment. ATLAS is a particle physics experiment at the Large Hadron Collider at CERN (the European Organization for Nuclear Research) in Switzerland.

This paper is organized as follows. The amplifier structure is analyzed in Sections 2 and 3. Section 4 describes the optimization approach proposed in this work. Section 5 presents

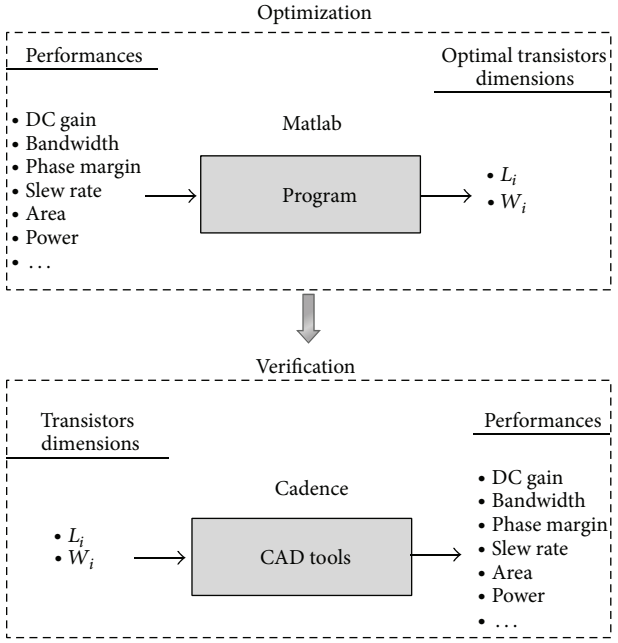

Figure 1: Operational amplifier design flow.

the obtained results, and there is a section for the comparison of our work with other optimization approaches. Finally some concluding remarks are provided after evaluating our study towards other works.

2. Design Methodology

Optimal design of analog circuits consists of finding a variable set $x = \{x_1, x_2, \ldots, x_n\}$ that optimizes performance functions, such as gain, offset, signal to noise ratio, and maximum operating frequency, while meeting imposed specifications and/or inherent constraints, for example, saturation conditions of transistors, technology limits, and impedance matching. Vector x may encompass biases, lengths (L), and widths (W) of MOS transistors, component values, and so forth [5].

3. Specifications

We concentrate on one operational amplifier topology and the two-stage operational amplifier shown in Figure 2. The main electrical parameters of the circuit are low frequency voltage gain (A_v), gain-bandwidth product (GBW), slew-rate (SR), dissipated power (P_{diss}), phase margin (PM), and area (A), among others. The design variables are the size of transistor (width and length), the value of the passive components (capacitors and resistors), and the value of bias currents and bias voltages. For this particular two-stage operational amplifier, there are fourteen design variables.

3.1. Open-Loop DC Gain. For the two-stage op-amp, the open-loop voltage gain is given by [3]

$$A_v = \frac{g_{m1}}{g_{ds2} + g_{ds4}} \cdot \frac{g_{m6}}{g_{ds7} + g_{ds6}}, \tag{1}$$

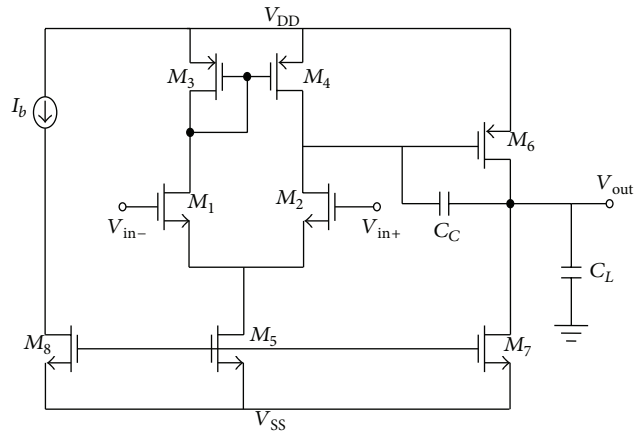

Figure 2: The two-stage operational amplifier architecture used in this study is composed of eight CMOS transistors.

where g_m (g_{m1} g_{m6}) is the transconductance of transistors (M_1 and M_6) and g_{ds} is the output conductance.

3.2. Unity-Gain Bandwidth. The unity-gain bandwidth is given by the expression [1]

$$\text{GBW} = \frac{g_{m1}}{C_C}, \tag{2}$$

where C_C is the compensation capacitance.

3.3. Phase Margin. The phase margin of operational amplifier depends on the sum of phase shifts, at the unity-gain frequency, contributed by the nondominant poles ($p1$ and $p2$) and zeros (z):

$$\begin{aligned}\text{PM} = \pm 180 - \tan^{-1}\left(\frac{\text{GBW}}{p1}\right) \\ - \tan^{-1}\left(\frac{\text{GBW}}{p2}\right) - \tan^{-1}\left(\frac{\text{GBW}}{z}\right).\end{aligned} \tag{3}$$

3.4. Slew Rate. For this operational amplifier, the slew rate is given by

$$\text{SR} = \frac{I_5}{C_C}, \tag{4}$$

where I_5 is the current that flows through transistor M_5.

3.5. Power Consumption. For the two-stage operational amplifier, the power consumption has the form [10]

$$P = (V_{\text{DD}} - V_{\text{SS}})(I_5 + 2I_7). \tag{5}$$

3.6. Area. The area A of the operational amplifier is given by the sum of transistors and capacitors areas:

$$\text{Area} = \sum_{i=1}^{k} W_i \cdot L_i. \tag{6}$$

4. Optimization

To make the system power level, it is obviously important to size the different constituent blocks. At this level, the performance of each unit becomes constraints to be respected. The performances are bound by a set of equations which depends on the considered characteristics (gain, SR, etc.). The set of equations is nonlinear, and there is no systematic analytical method to solve it. In addition, the solution is not unique. For this reason, the best way is to use an optimizer that will help automate the resolution of equations (synthesis of analog circuits). It is important to note that, in the design of analog circuits, compromises are made because there are many performance parameters used to describe them. Nonlinear relationships between them make them a more delicate design.

Optimal design of analog circuits is to find a set of variables $x = \{x_1, x_2, \ldots, x_n\}$ that optimizes performance, such as gain, offset, and signal to noise ratio, while respecting the imposed specifications and/or constraints [6].

In the program, every individual is presented by a binary code string. From Figure 2, we can see that there are 8 transistors and a biasing current to be adjusted. As a total, there are 10 parameters to be adjusted and each gene of the chromosome stands for one parameter. Thus, the parameter vector is compressed to [8] [W_1, L_1, W_3, L_3, W_5, L_5, W_7, L_7, W_8, L_8].

Genetic algorithms start with an initial population of randomly generated individuals. Each individual in the population represents a possible solution to the problem of the study. Individuals evolve through successive iterations, called generations. In every generation, each individual in the population is evaluated using a measure of fitness. Then, the population of the next generation is created by genetic operators. The procedure continues until the stop condition is satisfied (Figure 3).

A weighted approach is used to optimize operational amplifiers. It uses adaptive weights along the optimization process to determine the overall fitness of an individual [7]:

$$F = \sum_{i=1}^{n} \omega_i \cdot f_i, \tag{7}$$

where ω_i is the weight coefficient of every subobjective, f_i is the overall fitness of every performance considered, and i is the number of the performances considered.

We used the Matlab optimization toolbox to implement optimization by MOGA. It starts by generating a random population of individuals. To pass from one generation k to generation $k + 1$, the following operations are performed. At first, the population is reproduced by good selection where individuals with the best evaluations tend to reproduce more often than those with bad evaluations. This population is applied to cross pairs of individuals (parents) of a certain proportion of the population (probability P_c, usually around 0.6) to produce new children. A mutation operator is applied to a certain proportion of the population (probability P_m, the P_c generally much lower). Finally, the new individuals are evaluated and incorporated into the population of the next generation and several stopping criteria of the algorithm are possible: the number of generations can be fixed a priori (time constant) or the algorithm can be stopped when the population does not evolve fast enough.

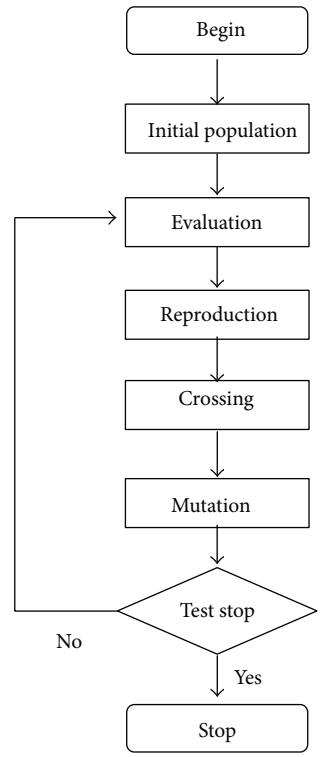

Figure 3: Basic procedures of genetic algorithms.

5. Results

Six performances are considered in this program. They are the DC gain, bandwidth of unity-gain, phase margin, power consumption, area, and slew rate. The optimization process optimizes the individual to improve its fitness score. This process will continue until the total number of generations is reached.

Also, by using variables obtained from GA, the OTA circuit is simulated by using Cadence Virtuoso Spectre in TSMC 0.18 μm CMOS process and simulation results are shown in Table 2 and Figure 4.

Table 2 shows the performance of the design obtained by Matlab optimization tools. The objective was to maximize the unity-gain bandwidth and minimize power consumption subject to the other given constraints. The simulation results confirm the efficiency of GA in determining the device sizes in an analog circuit.

According to the simulation results, the performance of the operational amplifier optimized by the proposed method represents a good method to optimize an analog circuit.

After introducing the transistors dimensions (Table 1) in Spectre and making the different simulations, we pass to the layout of the circuit which is represented in Figure 5 and the

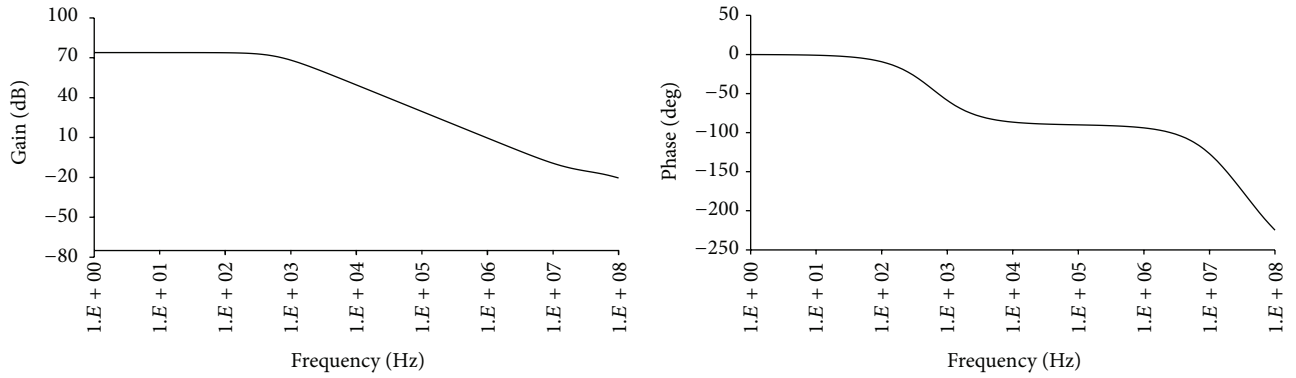

Figure 4: Gain and phase simulation of the obtained transistors dimensions.

Table 1: Optimal transistors dimensions.

Variable	Value (μm)
$W_1 = W_2$	1.34
$L_1 = L_2$	1.5
$W_3 = W_4$	8.5
$L_3 = L_4$	1.11
W_5	1.4
L_5	0.44
W_6	48
L_6	0.92
W_7	6
L_7	0.8
W_8	23.5
L_8	0.68

Table 2: Simulation results in Matlab and Spectre.

Performances	Specifications	MOGA program	Spectre
DC gain (dB)	≥70	76	75
Unity gain (MHz)	Max	1.5	1.11
Phase margin (°)	≥60	70	64
Slew rate (V/μs)	Max	2.25	2.19
Area (μm^2)	Min	559	678
Power (mW)	≤0.5	0.047	0.051

postlayout simulations. Figure 4 represents the simulation of gain and phase of the circuit.

The results given in the two Tables 1 and 2, respectively, represent the dimensions and performance operational amplifiers obtained for different constraints and conditions. With constraints on the optimizer, the satisfactory results (GWB aspects gain and PM) are obtained. However, the program happens to minimize power consumption and layout area.

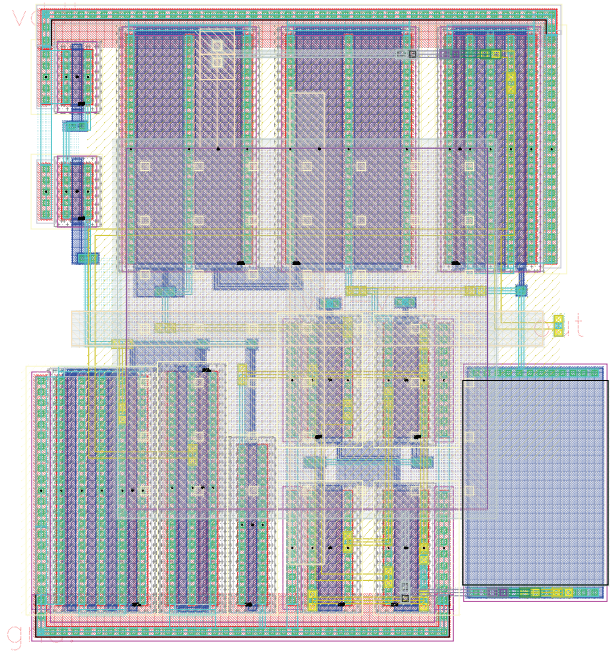

Figure 5: Layout of the operational amplifier.

6. Comparison

The lack of detail necessary to compare the results (such as limits of design variables, the supply voltage, bias current, capacitive load time, and circuit optimization) makes the comparison of our work with other optimization approaches presented a difficult task [11].

Kubar and Jakovenko [11] present comparisons with works using Miller two-stage OTA design example. These works [10, 12] are using particle swarm optimization.

The differences between the work [9] and our case are that transistors of the current mirror ($M3$ and $M4$) do not have the same size. Table 3 presents results in comparison with our design.

Table 3

Variable	Lower bound	Upper bound	Our result	Result [9]
W_1 (μm)	5	100	1.34	87.1
L_1 (μm)	0.18	2	1.5	0.55
W_2 (μm)	5	100	1.34	87.1
L_2 (μm)	0.18	2	1.5	0.55
W_3 (μm)	3	200	8.5	400
L_3 (μm)	0.18	2	1.11	8.4
W_4 (μm)	7	100	8.5	400
L_4 (μm)	0.18	2	1.11	8.4
W_5 (μm)	3	60	1.4	62.5
L_5 (μm)	0.18	2	0.44	0.55
W_6 (μm)	3	60	48	331.8
L_6 (μm)	0.18	2	0.92	0.4
W_7 (μm)	3	60	6	62.5
L_7 (μm)	0.18	2	0.8	0.55
W_8 (μm)	3	60	23.5	62.5
L_8 (μm)	0.18	2	0.68	0.55

7. Conclusion

This work demonstrates the utility of an evolutionary algorithm for automating electronic design using algorithms called MOGAs, which have the ability to deal with a problem of multiobjective optimization with two or more goals and taking the constraints also into account.

In this paper, a program based on multiobjective genetic algorithm has been developed for analog integrated circuits design. The genetic algorithm and equation-based optimization are combined to produce an accurate tool in order to determine the device sizes in an analog circuit. A MOGAs-based approach is proposed to optimize the performances of two-stage OTAs.

The results prove the effectiveness of the approach in the analog design where the design space is too complicated to be done with the classical methods within a short time. It can be concluded that the proposed MOGAs-based approach is efficient and gives promising results for circuits design and optimization problems.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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