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Research Article

Design Multipurpose Circuits with Minimum Garbage Outputs Using CMVMIN Gate

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Quantum-dot cellular automata (QCA) suggest an emerging computing paradigm for nanotechnology. The QCA offers novel approach in electronics for information processing and communication. QCA have recently become the focus of interest in the field of low power nanocomputing and nanotechnology. The fundamental logic elements of this technology are the majority voter (MV) and the inverter (INV). This paper presents a novel design with less garbage output and minimum quantum cost in nanotechnology. In the paper we show how to create multipurpose reversible gates. By development of suitable gates in logic circuits as an example, we can combine MFA and HS in one design using CMVMIN gate. We offer CMVMIN gate implementations to be used in multipurpose circuit. We can produce concurrent half adder/subtractor and one bit comparator in one design using reversible logic gates and CMVMIN gates. Also, a 2×4 decoder from recent architecture has been shown independently. We investigate the result of the proposed design using truth table. A significant improvement in quality of the calculated parameters and variety of required outputs has been achieved.

1. Introduction

This heat dissipation extremely reduces the performance and lifetime of the circuits. The solution is to use revolutionary technology which enables extremely low power consumption and heat waste in computing [1]. Reversible logic gates are extensively known to be compatible with future computing technologies which approximately dissipate zero heat [2]. Reversible are the circuits or the gates that have the same number of inputs and outputs and have one-to-one mappings between vectors of inputs and outputs; thus, the vector of the input states can be uniquely reconstructed from the vector of the output states [3].

The QCA (Quantum-dot cellular automata) are considered to be the promising technology for future generation ICs that overcome the limitations of CMOS. The fundamental unit of QCA based design is the 3-input majority gate (majority voter, MV) and the inverter. The wide acceptance of QCA in logic design attracts researchers to explore new universal gate structures targeting cost effective realization [4]. Existing synthesis tools do not make efficient use of MV in technology mapping for synthesis of logic designs. Even for arithmetic circuits, in which there should be perfect matches for the MV, the synthesis tools rarely find any matches [5].

This satisfies the requirement of optimum logic gates as well as minimum number of garbage outputs in an energy efficient design [6]. We illustrate CMVMIN gate with the target to reduce the number of logic gates and garbage outputs. In this work, we propose the use of CMVMIN gate as a basic of multipurpose circuit. We can construct other multipurpose circuits similarly.

2. Fundamental Reversible Gates

Because of their easiness and quantum realization cost there are design approaches and tools that incorporate them separately or in combination with each other. The quantum cost of a reversible circuit is the number of primary quantum gates required to implement a circuit [7]. Any reversible gate performs the permutation of its input patterns only and realizes the functions that are reversible. If a reversible gate has k inputs, and therefore k outputs, then we call it a $k * k$ reversible gate [8]. We demonstrate the application of the reversible gate to design multipurpose circuit. Firstly, in order

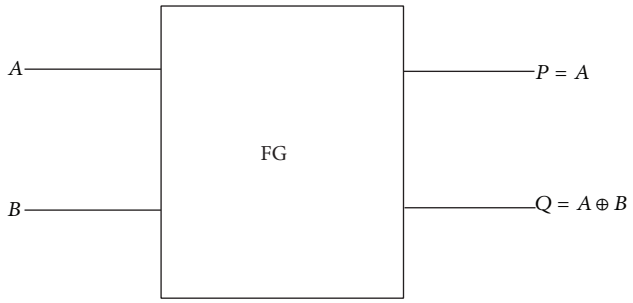

Figure 1: Feynman gate (FG).

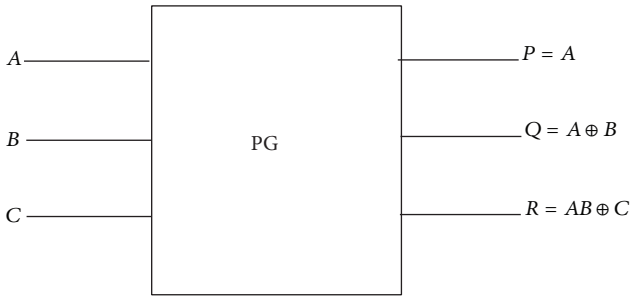

Figure 2: Peres gate (PG).

to derive the results we review the characterization of FG and PG gates. In Feynman gate, one of the input bits act as control signal (A). That is, if $A = 0$ then the output Q follows the input B. If $A = 1$ then the input B is flipped at the output Q. Because of this, it is called controlled NOT (1-NOT) and also called quantum XOR because of its popularity in the field of quantum computing [9]. Feynman gate (CNOT gate) is shown in Figure 1.

A $3 * 3$ one through reversible gate called Peres gate (PG) is introduced. Figure 2 shows the Peres gate as the reversible gate.

Also, the block diagram of RUG is shown in Figure 3. Since use of this universal function helps the realization of XNOR/XOR easily, the RUG can enable low cost realization of many other complex Boolean functions [6]. Another reversible gate, namely, IG gate, is presented in Figure 4 [8]. The application of these gates is described in the following sections.

3. The QCA Basics

The QCA (Quantum-dot cellular automata) are considered to be a promising technology to meet such a design target [6]. QCA have significant advantages in terms of power dissipation as they do not have to dissipate all their signal energy, hence, considered one of the promising technologies to achieve the thermodynamic limit of computation [10]. A QCA cell consists of two electrons positioned at opposite corners owing to coulombic repulsion, so the polarization states of $P = -1$ and $P = +1$ can be represented by two stable configurations of a pair of electrons; the corresponding logic values of "0" and "1" also are represented in Figure 5.

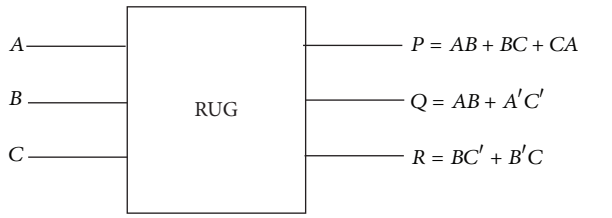

Figure 3: The reversible universal gate (RUG).

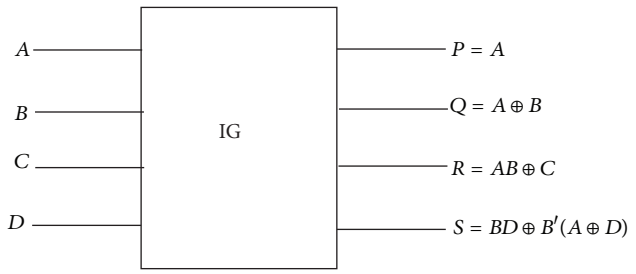

Figure 4: $4 * 4$ reversible gate (IG).

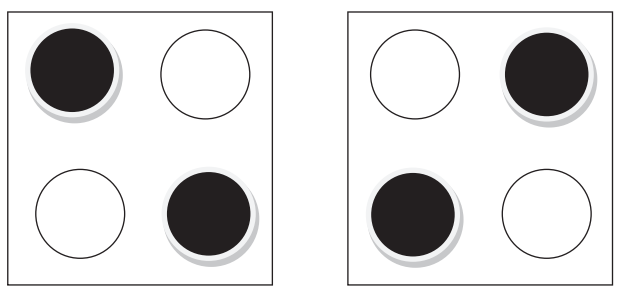

Figure 5: Quantum cellular automata [9].

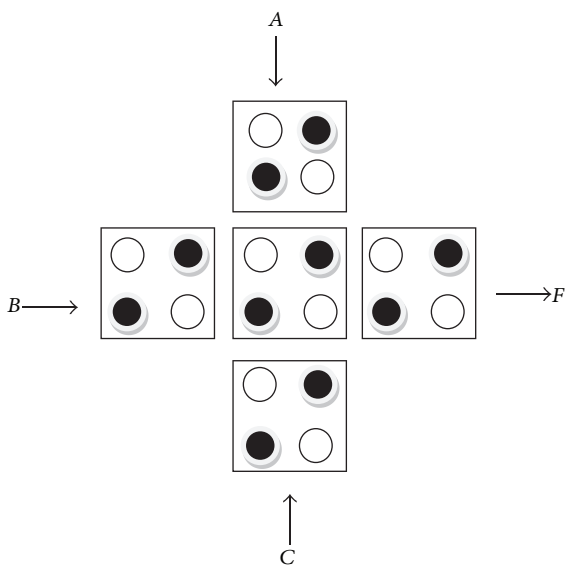

Figure 6: QCA majority gate [12].

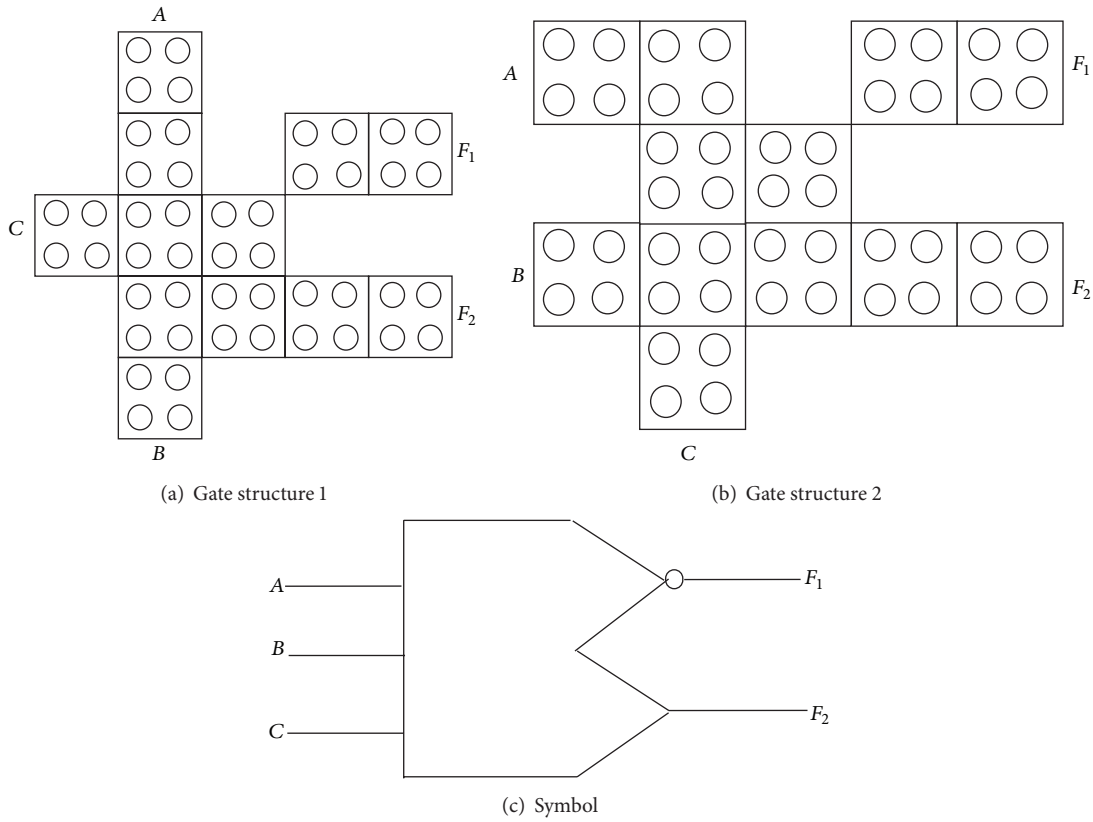

Figure 7: Gate structures and symbol of CMVMIN gate [12].

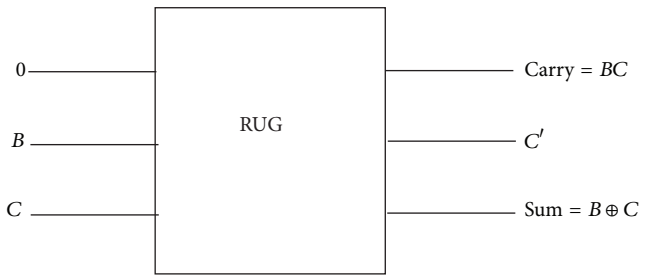

Figure 8: RUG as half adder.

Table 1: Truth table of CMVMIN gate.

A	B	C	F_1	F_2
0	0	0	1	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1

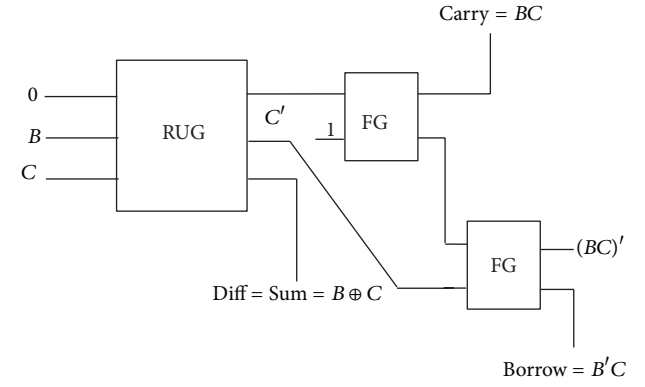

Figure 9: Concurrent half adder/subtractor circuit using RUG and FG.

A majority gate with the logic function of MV $(A, B, C) = AB + AC + BC$ is composed of five cells. By setting one of the inputs of this gate permanently to 0 or 1, AND and OR functions will be formed in QCA [11]. We review NNI gate as the basic logic element for QCA based designs. This 3-input gate realizes the function $F = \text{NNI}(A, B, C) = \text{maj}(A', B, C') = A'B + BC' + C'A'$.

A QCA circuit can be efficiently built using majority gates and inverters. QCA majority gate is shown in Figure 6.

4. Coupled Majority-Minority Gate

In QCA, coplanar wire crossings are one of the very elegant features of this new low power computing paradigm.

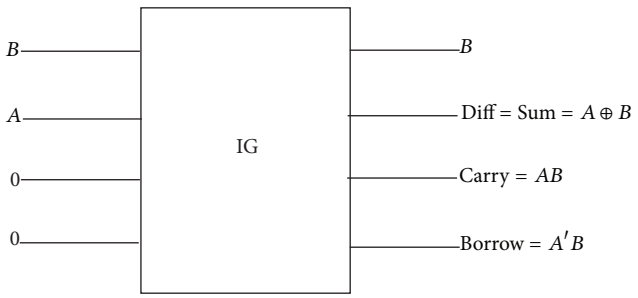

Figure 10: Concurrent half adder/subtractor circuit using IG.

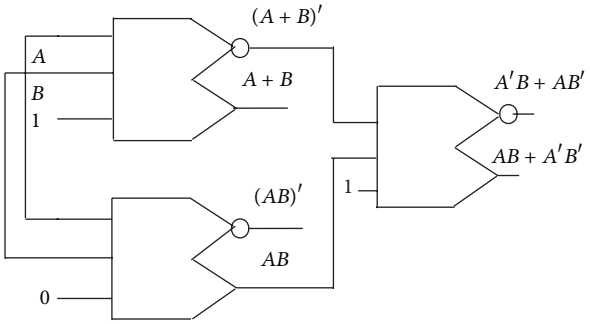

Figure 11: Generating 6 symmetric functions using CMVMIN gate.

However, these need two types of cells and are known to be neither easy to fabricate nor very robust. In QCA based logic design, the utmost necessity is to ensure least number of wire crossings due to its single layer restriction [11].

The coupled majority-minority (CMVMIN) QCA gate structure simultaneously realizes 3-input minority logic (MIN) and majority voter (MV) in its 2 outputs F_1 and F_2 (Figure 7). The $F_1 = A'B' + B'C' + C'A'$ is the complement of $F_2 = AB + BC + CA$. This gate is also realizable with a 3×3 tile structure. The truth table of CMVMIN gate is shown in Table 1. This gate can function as an AND-NAND gate ($F_2 = AB$ and $F_1 = (AB)'$) when input C is set to logic 0. Similarly, it can simultaneously realize OR ($F_2 = A + B$) and NOR ($F_1 = (A + B)'$) functions when C is set to 1.

Two structures are shown in Figures 7(a) and 7(b). The symbol of this gate is illustrated in Figure 7(c) [12].

5. Design Multipurpose Circuit

The major consideration in implementing the proposed multipurpose circuit is to enhance its speed as much as possible [13]. We could achieve some other various states configurations of logic circuits in quantum information and quantum computation [14].

Firstly, the design capability of RUG will be evaluated in implementing multipurpose circuits. If $A = 0$, then the outputs will be achieved according to Figure 8. One and three outputs represent the carry and sum of a half adder, respectively. Results of RUG are shown in Figure 8.

Now, we propose half adder/subtractor architecture in one design using RUG and two Feynman gates. The design

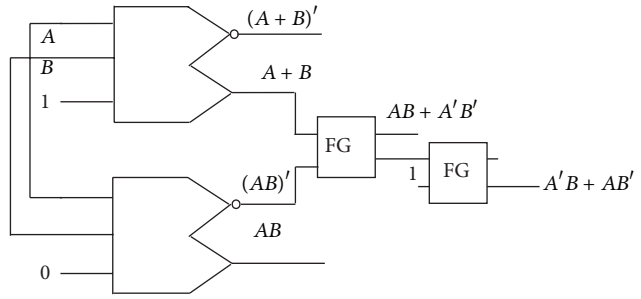

Figure 12: Generating 6 symmetric functions using CMVMIN and Feynman gate.

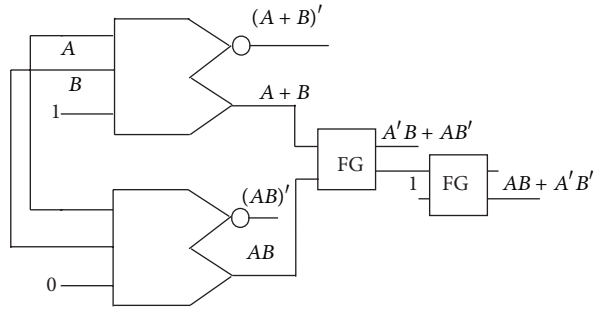

Figure 13: Generating 6 symmetric functions using CMVMIN and Feynman gate.

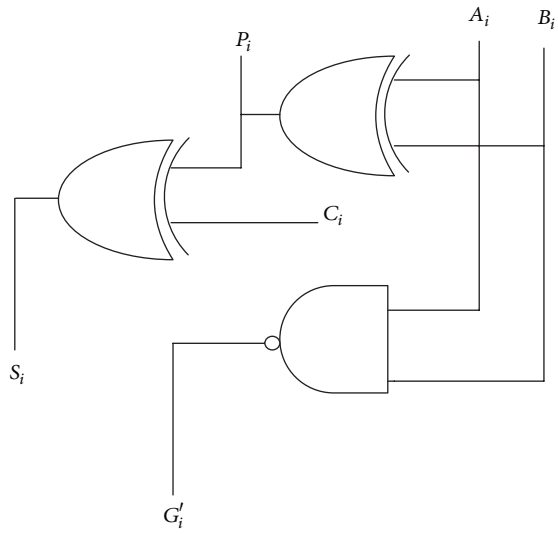

Figure 14: MFA (modified full adder) [15].

Table 2: Evaluation of the proposed circuit.

	No. of gates	Garbage outputs
Proposed circuit	3	1

of a mentioned circuit is presented which is implemented with minimum gates and garbage outputs. Results are shown in Figure 9. Table 2 shows the evaluation of the mentioned circuit.

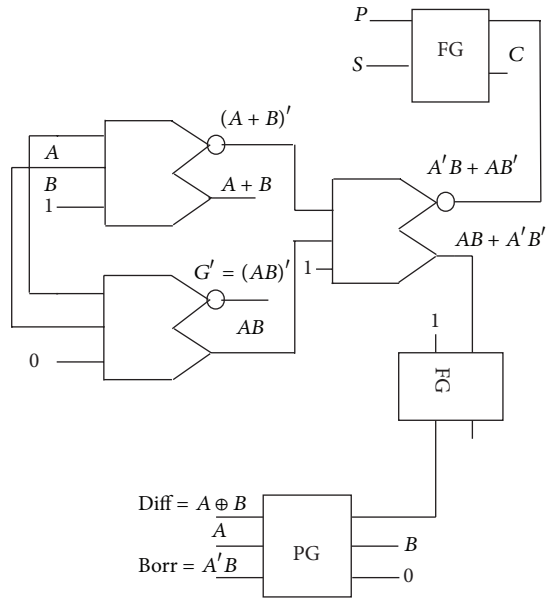

Figure 15: Multipurpose circuit (MFA and HS).

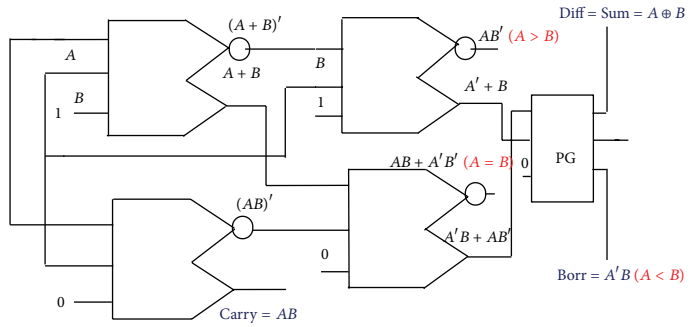

Figure 16: Multipurpose circuit using CMVMIN gate and Peres gate (HS, HA, and OBC).

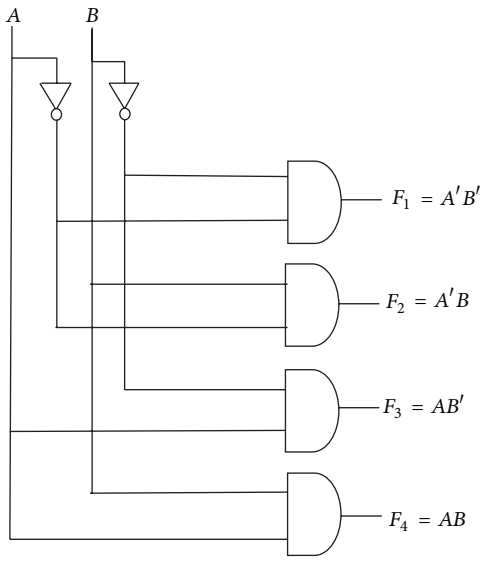

Figure 17: 2 × 4 decoder.

Table 3: Evaluation of the proposed circuit.

	No. of gates	Garbage outputs
Proposed circuit	1	1

On the other hand, we can demonstrate our goal with IG gate that its obtained result has better performance than previous structure. If inputs C and D are equal to zero, then the circuit will be depicted as follows. Hence, the mentioned circuit requires one reversible gate (IG gate) and produces one garbage output. The architecture of this gate is demonstrated in Figure 10. Table 3 shows the evaluation of the mentioned circuit.

Now, let us consider a function of conventional gates investigated by truth table. We realized the EXOR and EXNOR gates with the following equations. Table 4 shows the operation of the logic circuit topics. We have

$$F_1 \oplus F_3 = F_2 \oplus F_4 = \text{EXOR},$$
$$F_1 \oplus F_2 = F_3 \oplus F_4 = \text{EXNOR}. \quad (1)$$

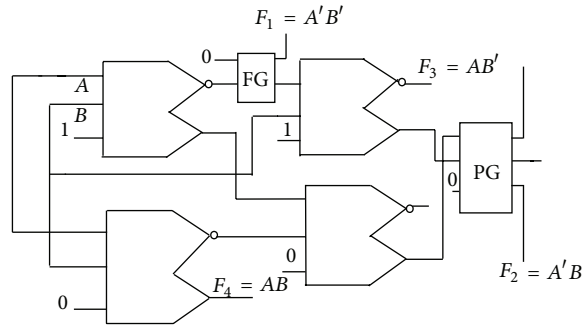

Figure 18: Comprehensive multipurpose circuit using CMVMIN gate and Peres gate (HS, HA, OBC, and 2 × 4 decoder).

Table 4: Truth table of conventional gate.

A	B	F_1 = AND	F_2 = NOR	F_3 = OR	F_4 = NAND
0	0	0	1	0	1
0	1	0	0	1	1
1	0	0	0	1	1
1	1	1	0	1	0

Table 5: Evaluation of the proposed circuit.

	No. of gates	Garbage outputs
Proposed circuit	6	3

A symmetric function means a Boolean function invariant to the permutation of any of its input variables [3]. Figure 11 points to the fact that only three CMVMIN gates are needed to realize all such 6 symmetric functions.

According to Table 4, by combining CMVMIN gate and Feynman gate, we can generate EXOR and EXNOR gates. Figures 12 and 13 show a combination of CMVMIN gates and FG gates.

Adder is profoundly used in the generic computer because it is very noticeable for adding data in the processor. The MCLA [15] uses the modified full adder (MFA) as shown in Figure 14. The major consideration in implementing the proposed multipurpose circuit is to enhance its speed as much as possible. On the other hand, the equations of borrow and difference for half subtractor are as follows:

$$\text{Borr} = A'B, \qquad \text{Diff} = A \oplus B. \tag{2}$$

Figure 15 is obtained by combining the two mentioned circuits. Table 5 shows the evaluation of the proposed design.

We can produce half subtractor, half adder, and one bit comparator in one design using Peres gate and CMVMIN gates. The proposed circuit of Figure 16 is evaluated in terms of number of reversible gates used and garbage outputs produced.

Table 6 shows the evaluation of the proposed design.

The following circuit has another application that is as a 2 × 4 decoder. Decoder is significant component and it is utilized in many logical and functional circuits. A decoder is a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. Figure 17 shows a 2 × 4 decoder. The behaviour of mentioned conventional circuit is defined as follows:

$$F_1 = A'B', \qquad F_2 = A'B,$$
$$F_3 = AB', \qquad F_4 = AB. \tag{3}$$

Hence, another proposed circuit implementation using additional Feynman gate is presented in Figure 18.

Figure 18 has been utilized to implement new aspect from available circuit. Table 7 shows the evaluation of the proposed design.

We see that the mentioned circuit performs significantly appropriate in terms of the number of gates and the number of garbage outputs. As we have seen, this multipurpose circuit produces only one garbage output. Therefore, we can infer that the proposed structure will successfully implement mentioned multipurpose circuit.

Table 6: Evaluation of the proposed circuit.

	No. of gates	Garbage outputs
Proposed circuit	5	1

Table 7: Evaluation of the comprehensive multipurpose circuit.

	No. of gates	Garbage outputs
Proposed circuit	6	1

6. Conclusion

Reversible logic has had promising interest in the recent past due to its less heat dissipating characteristics. An important purpose in our designs was to ensure that the designs are practical and usable. We present a novel design for concurrent half adder/subtractor scheme using RUG and two Feynman gates. However, these fundamental results motivate realizations of the same circuit using IG gate with better performance. One aim of this paper is to evaluate the CMVMIN gate in the available logic circuits with capable versatility and minimum garbage outputs susceptibility. Also, results are verified by the truth table. In addition, the last design is proposed for the multipurpose circuits in terms of garbage

output and gate count that was not ever seen. It clearly shows the capabilities and characteristics of CMVMIN gate for designing circuits. Also, we can generalize this concept to the other families of reversible gates. The experimental results illustrate that reversible logic is less likely to exhibit redundant logic than irreversible logic.

Conflict of Interests

The author declares that there is no conflict of interests regarding the publication of this paper.

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